15 MOS Model 11, level 1102

15.1 Introduction

General Remarks

MOS Model 11 (MM11, level 1102) is a new compact MOSFET model, intended for digital, analogue and RF circuit simulation in modern and future CMOS technologies [1] - [3]. MM11 is the successor of MOS Model 9, it was especially developed to give not only an accurate description of currents and charges and their first-order derivatives (i.e. transconductance, conductance, capacitances), but also of the higher-order derivatives, resulting in an accurate description of electrical distortion behaviour [3]. The latter is especially important for analog and RF circuit design. The model furthermore gives an accurate description of the noise behaviour of MOSFETs.
MOS Model 11 gives a complete description of all transistor-action related quantities: nodal currents, nodal charges and noise-power spectral densities. The equations describing these quantities are based on surface-potential formulations, resulting in equations valid over all operation regions (i.e. accumulation, depletion and inversion). Additionally, in order for the model to be valid for modern and future MOS devices, several important physical effects have been included in the model: mobility reduction, bias-dependent series-resistance, velocity saturation, drain-induced barrier lowering, static feedback, channel length modulation, self-heating, weak-avalanche (or impact ionization), gate current due to tunnelling, poly-depletion, quantum-mechanical effects on charges and bias-dependent overlap capacitances.

MOS Model 11 only provides a model for the intrinsic transistor and the gate/source- and gate/drain overlap regions. Junction charges, junction leakage currents and interconnect capacitances are not included. They are covered by separate models, which are not part of this documentation.

MOS Model 11, Level 1102, is an updated version of Level 1101 [2]. It uses slightly different equations than Level 1101.

The surface potential generally is implicitly related to the terminal voltages and has to be calculated iteratively. Since the iterative procedure was assumed to be time consuming, the surface potential has been approximated by an explicit expression [4] in previous levels of MM11[1]-[3]. In the Level 1102, the surface potential is calculated iteratively using a second-order Newton-Raphson procedure, resulting in a much more accurate description of surface potential which is obtained within 3 iterations. Owing to the increased accuracy, some of the basic equations used in Level 1101 can be simplified, and as a result Level 1102 is computationally as fast as Level 1101. In addition, a more physical and simpler velocity saturation expression is used, and as a consequence the saturation voltage expression has changed slightly as well. This all results in a more accurate description of transconductance in saturation.

The temperature scaling and geometrical scaling of parameters in MM11, Level 1102 is the same as in Level 1101. This implies that Level 1102 includes two types of geometrical scaling rules: physical rules and binning rules. It should be noted that using the source code of the Modelkit on the Philips' website (which can be found at http://www.semiconductors.philips.com/Philips_Models).

1. the physical geometry scaling rules can be selected by using Level 11020, while
2. the binning geometry scaling rules can be selected by using Level 11021.

Structural Elements of MOS Model 11

The structure of MOS Model 11 is the same as the structure of MOS Model 9[5]. The model is separable into a number of relatively independent parts, namely:

- **Model embedding**

It is convenient to use one single model for both *n*- and *p*-channel devices. For this reason, any *p*-channel device and its bias conditions are mapped onto those of an equivalent *n*-channel transistor. This mapping comprises a number of sign changes. Also, the model describes a symmetrical device, i.e. the source and drain nodes can be interchanged without changing the electrical properties. The assignment of source and drain to the channel nodes is based on the voltages of these nodes: for an *n*-channel transistor the node at the highest potential is called drain. In a circuit simulator the nodes are denoted by their network numbers, based on the circuit configuration. Again, a transformation is necessary involving a number of sign changes, including the directional noise-current sources.

- **Preprocessing**

The complete set of all the parameters, as they occur in the equations for the various electrical quantities, is denoted as the set of actual parameters, usually called the "miniset". In MM11, Level 1102, the temperature scaling parameters are included in the "miniset". Each of these actual parameters can be determined by purely electrical measurements. Since most of these parameters scale with geometry the process as a whole is characterized by an enlarged set of parameters, which is denoted as the set of scaling parameters, usually called the "maxiset". This set of parameters contains most of the actual parameters for an infinitely long and broad device and a large set of sensitivity coefficients. From this, the actual parameters for an arbitrary transistor are obtained by applying a set of transformation rules. The transformation rules describe the dependencies of the actual parameters on the length, width, and temperature. This procedure is called preprocessing, as it is normally done only once, prior to the actual electrical simulation.

In MM11, Level 1102, parameter binning has been facilitated by adding a second, separate set of geometry scaling rules. Consequently, besides the *physical* geometrical scaling rules

there is also a set of *binning* geometrical scaling rules. The physical geometry scaling rules of Level 1102 have been developed to give a good description over the whole geometry range of CMOS technologies. For processes under development, however, it is sometimes useful to have more flexible scaling relations. In this case one could opt for a binning strategy, where the accuracy with geometry is mostly determined by the number of bins used. The physical scaling rules of Level 1102 are not straightforwardly applicable to binning strategies, since they may result in discontinuities in parameter values at the bin boundaries. Consequently, special geometrical binning scaling relations have been developed, which guarantee continuity in the model parameters at the bin boundaries.

- **Clipping**

For very uncommon geometries or temperatures, the preprocessing rules may generate parameters that are outside a physically realistic range or that may create difficulties in the numerical evaluation of the model, for example division by zero. In order to prevent this, all parameters are limited to a pre-specified range directly after the preprocessing. This procedure is called clipping.

- **Current equations**

These are all expressions needed to obtain the DC nodal currents as a function of the bias conditions. They are segmentable in equations for the channel current, the gate tunnelling current and the avalanche current.

- **Charge equations**

These are all the equations that are used to calculate both the intrinsic and extrinsic charge quantities, which are assigned to the nodes.

- **Noise equations**

The total noise output of a transistor consists of a thermal- and a flicker noise part. which create fluctuations in the channel current. Owing to the capacitive coupling between gate and channel region, current fluctuations in the gate current are induced as well, which is referred to as induced gate noise.

15.2 Physics

15.2.1 Comments and Physical Background

In this section some physical background on the current, charge and noise description of MOS Model 11, Level 1102 will be given. For the full details of the physical background of the drain-source channel current equations the reader is referred to [3], [4], [6]-[9]. The gate current, charge and noise equations have been newly developed and their physical background will be discussed in a future report. All equations referred to are to be found in section 15.2.3.

Comments on Current Equations

Conventional MOS models such as MOS Model 9 and BSIM4 are threshold-voltage-based models, which make use of approximate expressions of the drain-source channel current I_{DS} in the weak-inversion region (i.e. subthreshold) and in the strong-inversion region (i.e. well above threshold). These approximate equations are tied together using a mathematical smoothing function, resulting in neither a physical nor an accurate description of I_{DS} in the moderate inversion region (i.e. around threshold). With the constant downscaling of supply voltage the moderate inversion region becomes more and more important, and an accurate description of this region is thus essential.

A more accurate type of model is the surface-potential-based model, where the channel current I_{DS} is split up in a drift (I_{drift}) and a diffusion (I_{diff}) component, which are a function of the gate bias V_{GB} and the surface potential at the source (ψ_{s_0}) and the drain (ψ_{s_L}) side. In this way I_{DS} can be accurately described using one equation for all operating regions (i.e. weak, moderate and strong-inversion). MOS Model 1102 is a surface-potential-based model.

Surface Potential

The surface potential ψ_s is defined as the electrostatic potential at the gate oxide/ substrate interface with respect to the neutral bulk (due to the band bending, see Figure 1a). For an n-MOS transistor with uniform doping concentration it can be calculated from the following implicit relation:

$$\left(\frac{V_{GB}-V_{FB}-\psi_p-\psi_s}{k_0}\right)^2 = \psi_s + \phi_T \cdot \left[\exp\left(-\frac{\psi_s}{\phi_T}\right)-1\right]$$

$$+\phi_T \cdot \exp\left(-\frac{\phi_B+V}{m_{\phi T}}\right)\cdot\left[\exp\left(\frac{\psi_s}{m_{\phi T}}\right)-\frac{\psi_s}{m_{\phi T}}-1\right]$$

where V is the quasi-Fermi potential, which ranges from V_{SB} at the source side to V_{DB} at the drain side. The parameter m_0 has been added to model the non-ideal subthreshold behaviour of short-channel transistors[1], and ψ_p is the potential drop in the polysilicon gate material due to the poly-depletion effect. The latter is given by[2]:

$$\psi_p = \begin{cases} 0 & \text{for: } V_{GB} \le V_{FB} \\ \left(\sqrt{V_{GB}-V_{FB}-\psi_s+\frac{k_p^2}{4}}-\frac{k_p}{2}\right)^2 & \text{for: } V_{GB} > V_{FB} \end{cases}$$

In Figure 1b the surface potential is shown as a function of gate bias for a typical n-type MOS device. The surface potential ψ_s is implicitly related to the gate bias V_{GB} and the quasi-Fermi potential V , and cannot be calculated analytically. It can only be calculated using an iterative solution, which in general is computation-time consuming. As a consequence, an explicit approximation of the surface potential was used in previous levels of MM11. In order to increase the accuracy of the calculated ψ_s, however, in MM11, Level 1102, the surface potential is calculated using a second-order Newton-Raphson iterative procedure . In this way, ψ_s is calculated with an accuracy of about $2.5 \cdot 10^{-12}$ and this accuracy is reached within 3 iterations. Owing to the increased accuracy some of the basic equations used in Level 1101 can be simplified, and as a result Level 1102 is computationally as fast as Level 1101. A more complete overview of the iterative calculation of ψ_s can be found in Section 15.5 on the implemented model equations.

1. Parameter $m_0 = 0$ for the ideal long-channel case.

2. For $V_{GB} < V_{FB}$ an accumulation layer is formed in both the substrate silicon and the gate polysilicon, in this case ψ_p is slightly negative and weakly dependent on V_{GB}. This effect has been neglected.

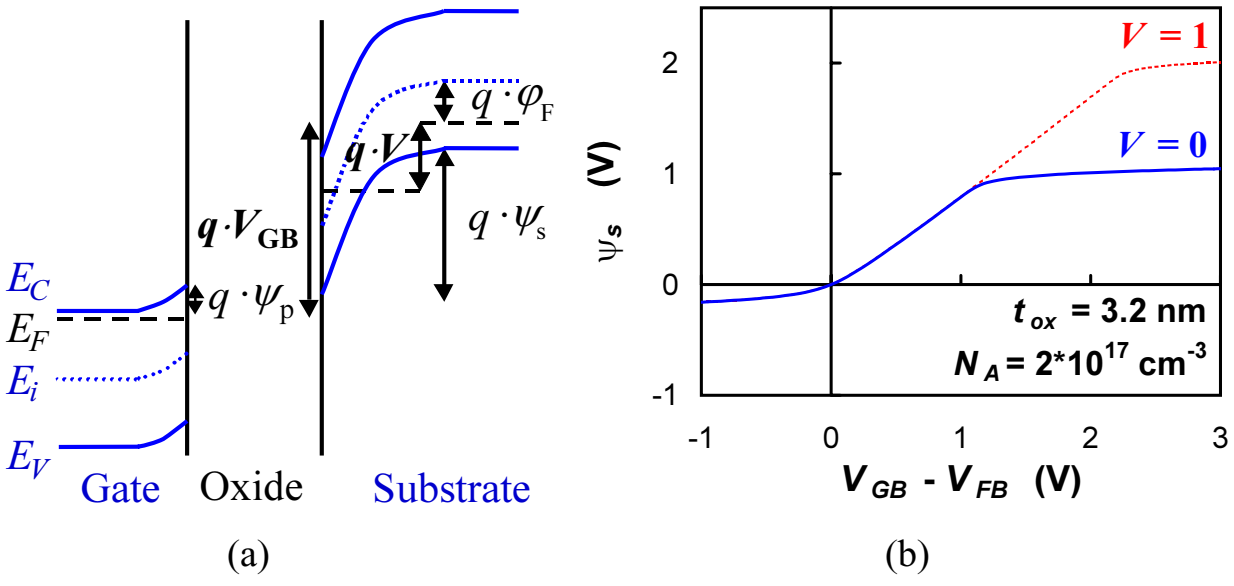


Figure 1: Left figure (a): The energy band diagram of an n-type MOS transistor in inversion ($V_{GB} > V_{FB}$), where ψ_s is the surface potential, ψ_p is the potential drop in the gate due to the poly-depletion effect, V is the quasi-Fermi potential and ϕ_F is the intrinsic Fermi-potential ($\phi_B = 2 \cdot \phi_F$). Right figure (b): The surface potential as a function of gate bias for different values of quasi-Fermi potential V ($m_0 = 0$).

A surface-potential-based model automatically incorporates the pinch-off condition at the drain side, and as a result it gives a description of both the linear (or ohmic) region and the saturation region for the ideal long-channel case. In this case the saturation voltage V_{DSAT} (i.e. the drain-source voltage above which saturation occurs) corresponds to Eq. (15.28). For short-channel devices, however, no real pinch-off occurs and the saturation voltage is affected by velocity saturation and series-resistance. In this case the saturation voltage V_{DSAT} is calculated using eqs. (15.28)-(15.33). The transition from linear to saturation region is no longer automatically described by the surface-potential-based model. This has been solved in the same way as in [11] by introducing an effective drain-source bias V_{DS_x} which changes smoothly from V_{DS} in the linear region to V_{DSAT} in the saturation region, see Eq. (15.34).

A surface-potential-based model makes no use of threshold voltage V_T. Circuit designers, however, are used to think in terms of threshold voltage, and as a consequence it would be useful to have a description of V_T in the framework of a surface-potential-model. It has been found that an accurate expression of threshold voltage is simply given by:

$$V_T = V_{FB} + \left(1 + \frac{k_0^2}{k_p^2}\right) \cdot (V_{SB} + \phi_B + 2 \cdot \phi_T) - V_{SB} + k_0 \cdot \sqrt{V_{SB} + \phi_B + 2 \cdot \phi_T}$$

The threshold voltage and other important parameters for circuit design are part of the operating point output as given in Section 15.7.1.

Channel Current

Neglecting the influence of gate and bulk current, the channel current can be written as: $I_{DS} = I_{drift} + I_{diff}$ where ideally the drift component I_{drift} can be approximated by (for $V_{GB} > V_{FB}$):

$$I_{drift} = -\beta \cdot \frac{Q_{inv_0} + Q_{inv_L}}{2 \cdot C_{ox}} \cdot (\psi_{s_L} - \psi_{s_0})$$

and the diffusion component I_{diff} can be approximated by (for $V_{GB} > V_{FB}$):

$$I_{diff} = \beta \cdot \phi_T \cdot \frac{(Q_{inv_L} - Q_{inv_0})}{C_{ox}}$$

Here, C_{ox} is given by ε_{ox}/t_{ox}, and Q_{inv_0} and Q_{inv_L} denote the inversion-layer charge density at the source and drain side, respectively, which are given by eqs. (15.42)-(15.44) (where $Q_{inv} = -\varepsilon_{ox}/t_{ox} \cdot V_{inv}$).

In the non-ideal case the channel current is affected by several physical effects, such as drain-induced barrier lowering, static feedback, mobility reduction, series-resistance, velocity saturation, channel length modulation and self-heating, which have to be taken into account in the channel current expression:

- In threshold-voltage-based models drain-induced barrier lowering and static feedback are traditionally implemented as a decrease in threshold voltage with drain bias. Here these effects have been implemented as an increase in effective gate bias ΔV_G given by eqs. (15.20)-(15.25). An effective drain-source voltage $V_{DS_{eff}}$ has been used to preserve non-singular behaviour in the higher-order derivatives of I_{DS} at $V_{DS} = 0$ V.

- The effects of mobility reduction and series-resistance on channel current have been described in [7], and have consequently been implemented using eqs. (15.53) and (15.57), respectively. For MOS Model 11, level 1102.3 and higher, the effect of the of Coulomb scat-

tering has been included in the mobility of the model. The equations for this have been adopted from the PSP model [8]

- The effect of velocity saturation has been modelled using the following electron velocity saturation expression [9]:

$$v = \frac{\mu \cdot E_{\parallel}}{\sqrt{1 + (\mu / v_{sat} \cdot E_{\parallel})^2}}$$

where $E_{\parallel}$ is the lateral electric field $E_{\parallel}$. Using the expression above in the calculation of channel current I_{DS} results in the velocity saturation expression (15.56), where θ_{sat} is theoretically equal to $\mu_0 / (v_{sat} \cdot L)$. For holes, the expression is slightly different.

- The effect of channel length modulation and self-heating on channel current have been described in [9], and have consequently been implemented using eqs. (15.54) and (15.58), respectively.

All the above effects can be incorporated into the channel current expression using Eq. (15.59) and Eq. (15.62).

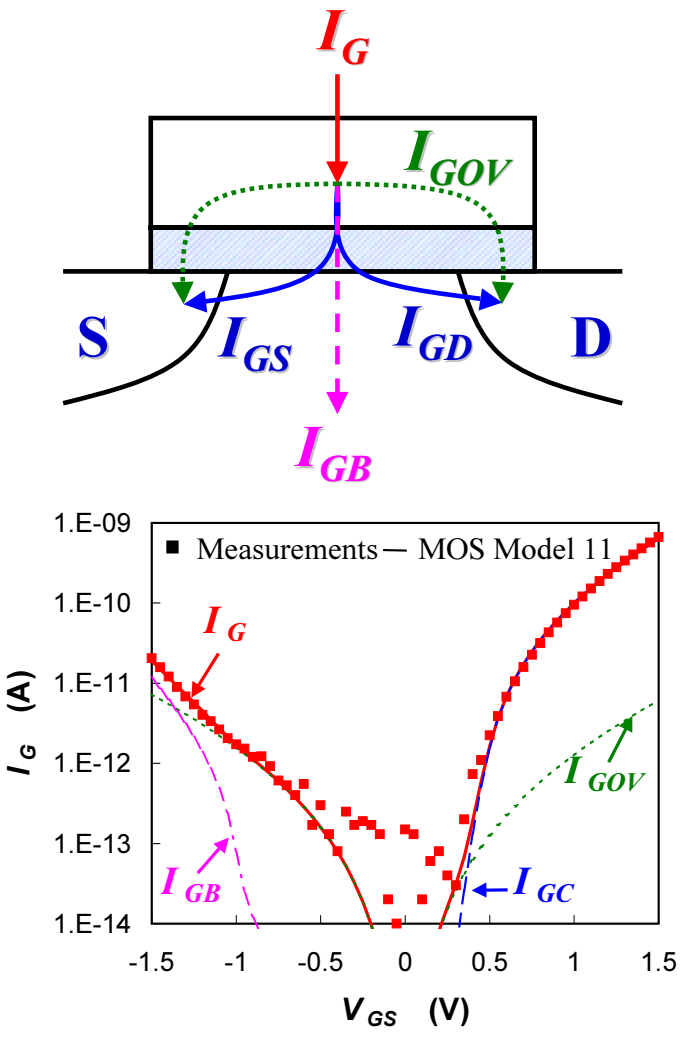


Figure 2: Upper figure (a): The different gate current components in a MOS transistor. One can distinguish the intrinsic components, i.e. the gate-to-channel current $I_{GC}(= I_{GS} + I_{GD})$ and the gate-to-bulk current I_{GB} , and the extrinsic, i.e. the gate/source and gate/drain overlap components $I_{G_{ov}}$.
Lower figure (b): Measured and modelled gate current as a function of gate bias V_{GS} at $V_{DS} = V_{SB} = 0\,V$, the different gate current components are also shown. NMOS-transistor, $W/L = 10/0.6\mu\,m$ and $t_{ox} = 2\,nm$.

Weak-Avalanche Current

At high drain bias, owing to the weak-avalanche effect (or impact ionization), a current I_{avl} will flow between drain and bulk[1]. The description of the weak-avalanche current has been

1.In reality, part of the generated avalanche current will also flow from drain to source [3], this has been neglected.

taken from MOS Model 9 [5], and is given by Eq. (15.63). With the down-scaling of supply voltage for modern CMOS technologies, weak-avalanche becomes less and less important.

Gate Tunnelling Current

With CMOS technology scaling the gate oxide thickness is reduced and, due to the direct-tunnelling of carriers through the oxide, the gate current is no longer negligible, and has to be taken into account. Several gate current components can be distinguished, three components (I_{GS}, I_{GD} and I_{GB}) due to the intrinsic MOS channel, and two components (I_{Gov_0} and I_{Gov_L}) due to gate/source and gate/drain overlap region, see Figure 2(a).

For an n-type MOS transistor operating in inversion, the intrinsic gate current density J_G consists of electrons tunnelling from the inversion layer to the gate, the so-called conductance band tunnelling, which in general can be written as [12] (for $V_{GB} > V_{FB}$):

$$J_G \propto -V_{ox} \cdot Q_{inv} \cdot P_{tun}\{V_{ox}, \chi_B, B\}$$

where V_{ox} is the oxide voltage given by $V_{ox} = V_{GB} - V_{FB} - \psi_p - \psi_s$. The carrier tunnelling probability P_{tun} is a function of the oxide voltage V_{ox}, the oxide energy barrier χ_B as observed by the inversion-layer carriers, and a parameter B. This probability is given by Eq. (15.71), where both direct-tunnelling for $V_{ox} < \chi_B$ and Fowler-Nordheim tunnelling for $V_{ox} > \chi_B$ have been taken into account.

Owing to quantum-mechanical energy quantization in the potential well at the SiO_2-surface, the electrons in the inversion layer are not situated at the bottom of the conduction band, but in the lowest energy subband which lies $\Delta\chi_B$ above the conduction band. Assuming that only the lowest energy subband is occupied by electrons, the value of $\Delta\chi_B$ can be given by Eq. (15.78) [13]. As a result the oxide barrier $\chi_{B_{eff}}$ has to be lowered by an amount of $\Delta\chi_B$, see Eq. (15.79).

In inversion the total intrinsic gate current consists of electrons tunnelling from inversion layer to gate, the so-called gate-to-channel current I_{GC}. These electrons are supplied by both source (I_{GS}) and drain (I_{GD}). The gate-to-channel current I_{GC} can be calculated from:

$$I_{GC} = W \cdot \int_0^L J_G \cdot dx$$

where x is the coordinate along the channel. Using a first-order perturbation approximation, i.e. assuming the gate current is small enough so that it does not change the distribution of surface potential along the channel, I_{GC} can be calculated by eqs. (15.78)-(15.87). In the same way the partitioning of I_{GC} into I_{GS} and I_{GD} can be calculated using:

$$I_{GS} = W \cdot \int_0^L \left(1 - \frac{x}{L}\right) \cdot J_G \cdot dx$$

$$I_{GD} = W \cdot \int_0^L \frac{x}{L} \cdot J_G \cdot dx$$

which results in expressions for I_{GS} and I_{GD} as given by eqs. (15.88)-(15.90). The gate-to-channel current I_{GC} can be seen in Figure 2(b) as a function of gate bias for a typical n-MOS transistor at $V_{DS} = 0$ (i.e. $I_{GS} = I_{GD} = 1/2 \cdot I_{GC}$).

For an n-type MOS transistor operating in accumulation, an accumulation layer of holes is formed in the p-type substrate and an accumulation layer of electrons is formed in the n^+-type polysilicon gate. Since the oxide energy barrier for electrons χ_{B_N} is considerably lower than that for holes χ_{B_P}, the gate current will mainly consist of electrons tunnelling from the gate to the bulk silicon, where they are swept to the bulk terminal. In this case the (intrinsic) gate current density J_G can be written as [12] (for $V_{GB} < V_{FB}$):

$$J_G \propto -V_{ox} \cdot Q_{acc} \cdot P_{tun}\{-V_{ox}, \chi_B, B\}$$

where Q_{acc} is the accumulation charge density in the gate given by $\varepsilon_{ox}/t_{ox} \cdot V_{ox}$. In order to limit calculation time the quantum-mechanical oxide barrier lowering in this case is neglected, and the resulting expression for I_{GB} is given by eqs. (15.76)-(15.77). The gate-to-bulk current I_{GB} can be seen in Figure 2(b) as a function of gate bias for a typical n-MOS transistor at $V_{DS} = 0$.

Apart from the intrinsic components I_{GC} and I_{GB}, considerable gate current can be generated in the gate/source- and gate/drain-overlap regions. Concentrating on the gate/source[1]-overlap region, in order to calculate the overlap gate current, the overlap region is treated as an n^+-gate/oxide/n^+-bulk MOS capacitance where the source acts as bulk. Although the impurity doping concentration in the n^+-source extension region is non-uniform in both lat-

1. In the following derivation, the same can be done for the gate/drain-overlap region by replacing the source by the drain.

eral and transversal direction, it is assumed that an effective flat-band voltage V_{FBov} and body-factor k_{ov} can be defined for this structure. Furthermore, assuming that only accumulation and depletion occur in the n^+-source region[1] , a surface potential $\psi_{s_{ov}}$ can be calculated using:

$$\left(\frac{V_{GS} - V_{FBov} - \psi_{p_{ov}} - \psi_{ov}}{k_{ov}}\right)^2 = -\psi_{ov} + \phi_T \cdot \left[\exp\left(\frac{\psi_{S_{OV}}}{\phi_T}\right) - 1\right]$$

where the potential drop in the polysilicon gate material due to the poly-depletion effect $\psi_{p_{ov}}$ is given by:

$$\psi_{p_{ov}} = \begin{cases} 0 & \text{for: } V_{GS} \leq V_{GBov} \\ \left(\sqrt{V_{GS} - V_{FBov} - \psi_{ov} + \frac{k_p^2}{4}} - \frac{k_p}{2}\right)^2 & \text{for: } V_{GS} > V_{FBov} \end{cases}$$

Again, the surface potential $\psi_{p_{ov}}$ is calculated a second-order Newton-Raphson iterative procedure, see eqs. (15.64)-(15.70). A more complete overview of the iterative calculation of $\psi_{p_{ov}}$ can be found in Section 15.5 on the implemented model equations.

For $V_{GS} > V_{FBov}$ a negatively charged accumulation layer is formed in the overlapped n^+-source extension and a positively charged depletion layer is formed in the overlapping gate. In this case the overlap gate current will mostly consist of electrons tunnelling from the source accumulation layer to the gate, it is given by:

$$I_{G_{ov}} \propto -V_{ov} \cdot Q_{ov} \cdot P_{tun}\{V_{ov}, \chi_B, B\}$$

where V_{ov} is the oxide voltage for the gate/source-overlap ($= V_{GS} - V_{FBov} - \psi_{p_{ov}} - \psi_{s_{ov}}$), given by eqs. (15.65)-(15.70), and Q_{ov} is the total charge density in the n^+-source region ($= \varepsilon_{ox}/t_{ox} \cdot V_{ov}$). For $V_{GS} < V_{FBov}$ the situation is reversed, a positively charged depletion layer is formed in the overlapped n^+-source extension and a negatively charged accumulation layer is formed in the overlapping gate. In this case the overlap gate current will mostly consist of electrons tunnelling from the gate accumulation layer to the source, it is given by:

$$I_{G_{ov}} \alpha \cdot V_{ov} \cdot Q_{ov} \cdot P_{tun}\{-V_{ov}, \chi_B, B\}$$

1.Since the source extension has a very high doping concentration, an inversion layer in the gate/source overlap will only be formed at very negative gate-source bias values. This effect has been neglected.

The overlap gate current components can now be given by eqs. (15.72)-(15.75). In Figure 2(b) the gate overlap current $I_{G_{ov}}$ is shown as a function of gate bias for a typical n-MOS transistor at $V_{DS} = 0$ (i.e. $I_{Gov_L} = I_{Gov_0}$). For n-type and p-type MOS transistors the gate current behaviour is different due to the type of carriers that constitute the different gate current components[1] . The difference is summarized in Table 17.

Table 17: The type of carriers that contribute to the gate tunnelling current in the various operation regions for the intrinsic MOSFET, the gate/drain- and gate/source-overlap regions. The type of carriers determine the value of oxide energy barrier χ_B that has to be used (χ_{B_N} for electrons, χ_{B_P} for holes). In the last row the direction of gate current is indicated.

Type	Intrinsic MOSFET		Overlap Regions
	Accumulation	Inversion	
NMOS	electrons	electrons	electrons
PMOS	electrons	holes	holes
	I_{GB}	I_{GS}/I_{GD}	I_{GS}/I_{GD}

Comments on Charge Equations

In a typical MOS structure we can distinguish intrinsic and extrinsic charges. The latter are due to the gate/source and gate/drain overlap regions. The drain/source junctions also contribute to the capacitance behaviour of a MOSFET, but this is not taken into account in MOS Model 11; it is described by a separate junction diode model.

Intrinsic Charges

In the intrinsic MOS transistor charges can be attributed to the four terminals. The gate charge Q_G can be simply calculated from:

1. It is assumed here that the gate current is only determined by conductance band tunnelling. For high values of gate bias (i.e. $q \cdot V_{ox} > E_g$) electrons in the bulk valence band may also tunnel through the oxide to the gate conduction band. This mechanism is referred to as valence band tunnelling, and it has not been taken into account in MOS Model 1101.

$$Q_G = -W \cdot \int_0^L Q_{tot} \cdot dx$$

where Q_{tot} is the total charge density in the silicon bulk ($Q_{tot} = -\varepsilon_{ox}/t_{ox} \cdot V_{ox}$). The total inversion-layer charge Q_{inv} is split up in a source Q_S and a drain Q_D charge, they can be calculated using the Ward-Dutton charge partitioning scheme [14]:

$$Q_S = W \cdot \int_0^L \left(1 - \frac{x}{L}\right) \cdot Q_{inv} \cdot dx$$

$$Q_D = W \cdot \int_0^L \frac{x}{L} \cdot Q_{inv} \cdot dx$$

Since charge neutrality holds for the complete transistor, the gate charge is simply given by:

$$Q_B = -Q_S - Q_D - Q_G$$

These equations have been solved, and the charges are given by eqs. (15.97)-(15.102). In these equations $C_{ox_{eff}}$ is the effective oxide capacitance, which is smaller than the ideal oxide capacitance C_{ox} due to quantum-mechanical effects: Quantum-mechanically, the inversion/accumulation charge concentration is not maximum at the Si-SiO_2-interface (as it would be in the classical case), but reaches a maximum at a distance Δz from the interface [13]. This quantum-mechanical effect can be taken into account by an effective oxide thickness $t_{ox} + \varepsilon_{ox}/\varepsilon_{si} \cdot \Delta z$, where Δz is dependent on the effective electric field E_{eff} [13], [15]($E_{eff} = -\varepsilon_{ox}/\varepsilon_{si} \cdot V_{eff}/t_{ox}$). The effective oxide thickness results in an effective oxide capacitance $C_{ox_{eff}}$, see Eq. (15.97).

It should be noted that the above charge model is quasi-static. A phase-shift between drain channel current and gate voltage is not taken into account. This implies that for a few applications at high frequencies approaching the cut-off frequency, errors have to be expected due to non-quasi-static effects. Nevertheless non-quasi-effects can be taken into account using a segmentation model as described in [16].

Extrinsic Charges

The gate/source- and gate/drain-overlap regions act as bias-dependent capaci-tances. In order to take this bias-dependence into account the overlap regions are treated as an n^+-gate/oxide/n^+-bulk MOS capacitance along the same lines as was done for the overlap gate

current, see the section titled *Comments on Current Equations*. The charge in the overlap regions can simply be given by eqs. (15.95)-(15.96). The quantum-mechanical effect on oxide thickness has been neglected here in order to reduce calculation time.

Comments on Noise Equations

In a MOS transistor generally three different types of noise can be observed: $1/f$-noise, thermal noise and induced gate noise. The gate tunnel current and the bulk avalanche current will also exhibit noisy behaviour (due to shot noise), however this has been neglected in MOS Model 11.

$1/f$ -Noise

At low frequencies flicker (or $1/f$) noise becomes dominant in MOSFETs. In the past this type of noise has been interpreted either in terms of trapping and detrapping of charge carriers in the gate oxide or in terms of mobility fluctuations. Over the past years, a general model for $1/f$-noise which combines both of the above physical origins [20], [21], has found wide acceptance in the field of MOS modelling. The model assumes that the carrier number in the channel fluctuates due to trapping/detrapping in the gate oxide, and that these number fluctuations also affect the carrier mobility resulting in (correlated) mobility fluctuations.

The same model is part of MOS Model 9 [22], and has been used to calculate the $1/f$-noise for MOS Model 11. The calculations have been performed in such a way that the resulting expression for spectral density is valid for all operation regions (i.e. both in subthreshold and above threshold), it is given by eqs. (15.118)-(15.122).

Thermal Noise

Since the MOSFET channel can be considered as a non linear resistor, the channel current is subject to thermal noise. For an ideal MOSFET, where the mobility is position independent, the thermal noise is given by the so-called Klaassen-Prins equation [10]. Let thermal noise current sources be parallel connected to each infinitesimal short element of the channel, it can be shown that the noise spectral density, which is defined by [10]:

$$\langle \Delta i_{th}^2 \rangle = \int_0^\infty s_{th}(f)\,df$$

is given by a generalized Nyquist relation:

$$S_{th} = \frac{N_T}{L^2} \cdot \int_0^L g(x)\,dx$$

where N_T is equal to $4 \cdot k_B \cdot T$ and $g(x)$ is the local specific channel conductance:

$$g(x) = -\mu(x) \cdot W \cdot Q_{inv}(x)$$

In reality, however, the mobility $\mu(x)$ is position dependent mainly due to the effect of velocity saturation. In this case, the conventional Klaassen-Prins approach does not hold, and an improved Klaassen-Prins approach has been derived [10]. This improved approach results in the spectral density given by eqs. (15.104)-(15.112). Again continuity of the noise model is assured along all modes of operation. The above thermal noise model has been found to accurately describe exper-imental results for various CMOS technologies without having to invoke carrier heating effects [10].

Induced Gate Noise

Owing to capacitive coupling between gate and channel, the fluctuating channel current induces noise in the gate terminal at high frequencies. Using the previously mentioned improved Klaassen-Prins approach [10], we can derive eqn. (15.113) for the induced gate current noise. In addition, since S_{th} and S_{ig} have the same physical origin, both spectral densities are correlated. Using the approach described, this can be expressed by eqn. (15.114):

The induced gate noise S_{ig} is a so-called non-quasi static (NQS) effect. Since the use of the channel current noise description in an NQS segmentation model [16] would automatically result in a correct description of induced gate noise, S_{ig} can be made equal to zero by using parameter GATENOISE, see Eq. (15.113).

15.2.2 Calculation of Temperature-Dependent Parameters

In this section, the temperature scaling rules for the parameters of the electrical model will be given. In contrast to the geometry scaling rules, as treated in Section 15.4, the temperature scaling is the same for both level 11020 and 11021.

3 Note

Note the addition of the voltage V_{dT} of the thermal node in order to include self-heating, see Section 15.6.

Calculation of Transistor Temperature

$$T_{KR} = T_0 + T_R \tag{15.1}$$

$$T_{amb} = T_0 + T_A + \Delta T_A \tag{15.2}$$

$$T_{KD} = T_0 + T_A + \Delta T_A + V_{dT} \tag{15.3}$$

Calculation of Threshold-Voltage Parameters

$$\phi_T = \frac{k_B \cdot T_{KD}}{q} \tag{15.4}$$

$$V_{FB_T} = V_{FB} + (T_{KD} - T_{KR}) \cdot S_{T;V_{FB}} \tag{15.5}$$

$$\phi_{B_T} = \phi_B + (T_{KD} - T_{KR}) \cdot S_{T;\phi_B} \tag{15.6}$$

Calculation of Mobility/Series-Resistance Parameters

$$\beta_T = \beta \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta\beta} \tag{15.7}$$

$$\theta_{sr_T} = \theta_{sr} \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta sr} \tag{15.8}$$

$$\theta_{ph_T} = \theta_{ph} \cdot \left(\frac{T_{KD}}{T_{KR}}\right)^{\eta_{ph}} \tag{15.9}$$

$$\eta_{mob_T} = \eta_{mob} \cdot [1 + (T_{KD} - T_{KR}) \cdot S_{T;\eta_{mob}}] \tag{15.10}$$

$$v_T = 1 + (v - 1) \cdot (T_{KR}/T_{KD})^{v_{\exp}} \tag{15.11}$$

$$C_{s_T} = C_s \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta_{C_s}} \tag{15.12}$$

$$\theta_{R_T} = \theta_R \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta_R} \tag{15.13}$$

$$\theta_{sat_T} = \theta_{sat} \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta sat} \tag{15.14}$$

Calculation of Conductance Parameters

$$\theta_{Th_T} = \theta_{Th} \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta\beta} \tag{15.15}$$

Calculation of Weak-Avalanche Parameters

$$a_{1_T} = a_1 \cdot [1 + (T_{KD} - T_{KR}) \cdot S_{T;a_1}] \tag{15.16}$$

Calculation of Gate-Induced Drain Leakage Parameters

$$B_{GIDL_T} = B_{GIDL} \cdot [1 + (T_{KD} - T_{KR}) \cdot S_{T;B_{GIDL}}] \tag{15.17}$$

Calculation of Noise Parameters

$$N_{T_T} = \frac{T_{KD}}{T_{KR}} \cdot N_T \tag{15.18}$$

Calculation of Thermal Resistance

$$R_{Th_T} = R_{Th} \cdot \left(\frac{T_{amb}}{T_{KR}} \right)^{A_{Th}} \tag{15.19}$$

15.2.3 Basic Equations

The equations listed in the following sections, are the basic equations of MOS model 11 without any adaptation necessary for numerical reasons. As such they form the base for parameter extraction. In the following, a function is denoted by *F*{*variable*, ...}, where *F* denotes the function name and the function variables are enclosed by braces {}.

Internal Parameters

$$\varepsilon_1 = 1 \cdot 10^{-2}$$

$$\varepsilon_2 = 4 \cdot 10^{-2}$$

$$\varepsilon_3 = 1 \cdot 10^{-4}$$

$$\varepsilon_4 = 1 \cdot 10^{-14}$$

$$P_D = 1 + (k_0 / k_p)^2$$

$$V_{limit} = 4 \cdot \phi_T$$

$$\theta_{R_{eff}} = \frac{1}{2} \cdot \theta_{R_T} \cdot \left(1 + \frac{\theta_{R1}}{1/2 + \theta_{R2}}\right)$$

$$m_{\phi T} = (1 + m_0) \cdot \phi_T$$

$$Acc = \left.\frac{\partial \psi_s}{\partial V_{GB}}\right|_{V_{GB} = V_{FB_T}} = \frac{1}{1 + k_0 / \sqrt{2 \cdot \phi_T}}$$

$$Acc_{ov} = \left.\frac{\partial \psi_{sov}}{\partial V_{GB}}\right|_{V_{GB} = V_{FBov}} = \frac{1}{1 + k_{ov} / \sqrt{2 \cdot \phi_T}}$$

$$QM_{\psi} = \begin{cases} QM_N \cdot (\varepsilon_{ox}/t_{ox})^{2/3} & \text{for NMOS} \\ QM_N \cdot (\varepsilon_{ox}/t_{ox})^{2/3} & \text{for PMOS} \end{cases}$$

$$QM_{tox} = \frac{2}{5} \cdot QM_{\psi}$$

$$\chi_{B_{inv}} = \begin{cases} \chi_{B_N} & \text{for NMOS} \\ \chi_{B_P} & \text{for PMOS} \end{cases}$$

$$\chi_{B_{acc}} = \chi_{B_N}$$

Basic Current Equations

Drain induced barrier lowering and Static Feedback:

$$V_{GB_{eff}} = \begin{cases} 0 & \textit{for:} \quad V_{GS} + V_{SB} - V_{FB_T} \le 0 \\ V_{GS} + V_{SB} - V_{FB} & \textit{for:} \quad V_{GS} + V_{SB} - V_{FB_T} > 0 \end{cases} \tag{15.20}$$

$$\psi_{sat_0} = \left(\frac{\sqrt{P_D \cdot V_{GB_{eff}} + k_0^2/4} - k_0/2}{P_D} \right)^2 \tag{15.21}$$

$$D_{dibl} = \sigma_{dibl} \cdot \sqrt{V_{SB} + \phi_{B_T}} \tag{15.22}$$

$$D_{sf} = \begin{cases} 0 & \textit{for:} \quad \psi_{sat_0} - V_{SB} - \phi_{B_T} \le 0 \\ \sigma_{sf} \cdot \sqrt{\psi_{sat_0} - V_{SB} - \phi_{B_T}} & \textit{for:} \quad \psi_{sat_0} - V_{SB} - \phi_{B_T} > 0 \end{cases} \tag{15.23}$$

$$V_{DS_{eff}} = \frac{V_{DS}^{4}}{(V_{limit}^{2} + V_{DS}^{2})^{3/2}} \tag{15.24}$$

$$\Delta V_G = \sqrt{D_{dibl}^{2} + D_{sf}^{2}} \cdot V_{DS_{eff}} \tag{15.25}$$

Effective Gate-Bulk Voltage:

$$V_{GB}^{*} = V_{GS} + V_{SB} + \Delta V_G - V_{FB_T} \tag{15.26}$$

Drain Saturation Voltage:

$$\Psi_{SAT_1} = \begin{cases} 0 & \text{for: } V_{GB}^{*} \leq 0 \\ ([\sqrt{P_D \cdot V_{GB}^{*} + k_0^{2}/4} - k_0/2]/P_D)^{2} & \text{for: } V_{GB}^{*} > 0 \end{cases} \tag{15.27}$$

$$V_{DSAT_{long}} = \Psi_{sat_1} - V_{SB} - \phi_{B_T} \tag{15.28}$$

$$T_{sat} = \begin{cases} \theta_{sat_T} & \text{for NMOS} \\ \dfrac{\theta_{sat_T}}{(1 + \theta_{sat_T}^{2} \cdot V_{DSAT_{longX}}^{2})^{1/4}} & \text{for PMOS} \end{cases} \tag{15.29}$$

$$V_{DSAT_{longX}} = \sqrt{(V_{DSAT_{long}}^{2} + \varepsilon_1)}, \text{ where } \varepsilon_1 = 0.01 \tag{15.30}$$

$$\Delta_{SAT} = \frac{(T_{sat} - \theta_{R_{eff}}) \cdot V_{DSAT_{long}}}{\frac{1}{2} \cdot \left(\sqrt{2} + \sqrt{2 + 2 \cdot {T_{sat}}^2 \cdot {V_{DSAT_{longX}}}^2} \right) + \theta_{R_{eff}} \cdot V_{DSAT_{long}}} \quad (15.31)$$

$$V_{DSAT_{short}} = V_{DSAT_{long}} \cdot \left[1 - \frac{44/45 \cdot \Delta_{SAT}}{1 + \sqrt{1 - \frac{(\sqrt{2} - 1) \cdot T_{sat} - \theta_{R_{eff}}}{T_{sat} - \theta_{R_{eff}}} \cdot {\Delta_{SAT}}^2}} \right] \quad (15.32)$$

$$V_{DSAT} = \begin{cases} V_{limit} & for: \quad V_{DSAT_{short}} \leq V_{limit} \\ V_{DSAT_{short}} & for: \quad V_{DSAT_{short}} > V_{limit} \end{cases} \quad (15.33)$$

$$V_{DS_x} = \frac{V_{DS}}{[1 + (V_{DS}/V_{DSAT})^{2 \cdot m}]^{\frac{1}{2 \cdot m}}} \quad (15.34)$$

Surface Potential:

The surface potential ψ_s is given by the following implicit relation:

$$F\{\psi_{s,}\theta\} = -V_{OX}\{\psi_s\}^2 + {k_0}^2 \cdot d\{\psi_{s,}\phi\} = 0 \quad (15.35)$$

where ϕ can be either $V_{SB} + \phi_{B_T}$ or $V_{DS_x} + V_{SB} + \phi_{B_T,}$ and:

$$V_{OX}\{\psi_S\} = \begin{cases} V^*_{GB} - \psi_s & \text{for: } V^*_{GB} - \psi_s \le 0 \\ \dfrac{2 \cdot (V^*_{GB} - \psi_S)}{1 + \sqrt{1 + 4/k_p{}^2 \cdot (V^*_{GB} - \psi_s)}} & \text{for: } V^*_{GB} - \psi_s > 0 \end{cases} \tag{15.36}$$

$$d\{\psi_s, \phi\} = \psi_s + \phi_T \cdot \left[\exp\left(-\frac{\psi_s}{\phi_T}\right) - 1 \right] + \phi_T \cdot \exp\left(-\frac{\phi}{m_{\phi T}}\right) \cdot \left[\exp\left(\frac{\psi_s}{m_{\phi T}}\right) - \frac{\psi_s}{m_{\phi T}} - 1 \right] \tag{15.37}$$

The surface potential is iteratively calculated using a second-order Newton Raphson procedure. The surface potential at the source ψ_{S_0} and at the drain ψ_{S_L} are calculated iteratively using a second-order Newton Raphson procedure from the following implicit relations:

$$F\{\psi_{S_0}, V_{SB} + \phi_{B_T}\} = 0 \tag{15.38}$$

$$F\{\psi_{S_L}, V_{DS_X} + V_{SB} + \phi_{B_T}\} = 0 \tag{15.39}$$

Auxiliary Variables:

$$\Delta\psi = \psi_{s_L} - \psi_{s_0} \tag{15.40}$$

$$\overline{\psi} = \frac{\psi_{s_L} + \psi_{s_0}}{2} \tag{15.41}$$

Inversion-Layer Charge ($Q_{inv} = -\varepsilon_{ox}/t_{ox} \cdot V_{inv}$):

$$V_{inv}\{\psi,\phi\} = \begin{cases} 0 & \text{for: } V^*_{GB} - \psi_s \le 0 \\ \dfrac{k_0 \cdot \phi_T \cdot \exp(-\phi/m_{\phi_T}) \cdot [\exp(\psi_s/m_{\phi_T}) - \psi_S/m_{\phi_T} - 1]}{\sqrt{d\{\phi,\psi_s\}} + \sqrt{\psi_s + \phi_T \cdot [\exp(-\psi_s/\phi_T) - 1]}} & \text{for: } V^*_{GB} - \psi_s > 0 \end{cases} \tag{15.42}$$

$$V_{inv_0} = V_{inv}\{\psi_{s_0}, V_{SB} + \phi_{B_T}\} \tag{15.43}$$

$$V_{inv_L} = V_{inv}\{\psi_{s_L}, V_{DS_x} + V_{SB} + \phi_{B_T}\} \tag{15.44}$$

$$\overline{V}_{inv} = \frac{V_{inv_0} + V_{inv_L}}{2} \tag{15.45}$$

$$\overline{V}_{ox} = \frac{V_{ox}\{\psi_{s_0}\} + V_{ox}\{\psi_{s_L}\}}{2} \tag{15.46}$$

$$V_{eff} = \overline{V}_{inv} + \eta_{mob_T} \cdot (\overline{V}_{ox} - \overline{V}_{inv}) \tag{15.47}$$

$$\xi_{OX}\{\psi_S\} = -\phi_T \frac{\dot{V}_{\partial V_{ox}}}{\partial \psi_s} = \begin{cases} \phi_T & \text{for: } V^*_{GB} - \psi_s \le 0 \\ \dfrac{\phi_T}{\sqrt{1 + 4/k_p{}^2 \cdot (V^*_{GB} - \psi_s)}} & \text{for: } V^*_{GB} - \psi_s > 0 \end{cases} \tag{15.48}$$

$$\overline{\xi}_{ox} = \frac{\xi_{ox}\{\psi_{s_0}\} + \xi_{ox}\{\psi_{s_L}\}}{2} \tag{15.49}$$

$$\xi\{\psi_s\} = -\phi_T \frac{\partial V_{inv}}{\partial \psi_s} = \begin{cases} \xi_{ox}\{\psi_s\} + \phi_T \cdot \left[\frac{1}{Acc} - 1\right] & \text{for: } V_{GB}^* - \psi_s \le 0 \\ \xi_{ox}\{\psi_s\} + \phi_T \cdot \frac{k_0 \cdot [1 - \exp(-\psi_s/\phi_T)]}{2 \cdot \sqrt{\psi_s + \phi_T \cdot [\exp(-\psi_s/\phi_T) - 1]}} & \text{for: } V_{GB}^* - \psi_s > 0 \end{cases} \quad (15.50)$$

$$\bar{\xi} = \frac{\xi\{\psi_{s_0}\} + \xi\{\psi_{s_L}\}}{2} \quad (15.51)$$

$$\bar{V}_{inv}^* = \bar{V}_{inv} + \{1 + m_0\} - \bar{\xi} \quad (15.52)$$

Second-Order Effects

Mobility Degradation:

$$G_{mob} = \frac{\mu_0}{\mu} = \begin{cases} 1 + \left[(\theta_{ph_T} \cdot V_{eff})^{\nu_T/3} + (\theta_{sr_T} \cdot V_{eff})^{2 \cdot \nu_T}\right]^{1/\nu_T} + C_{s_T} \cdot \left(\frac{\bar{V}_{dep}}{\bar{V}_{dep} + \bar{V}_{inv}}\right)^2 & \text{for NMOS} \\ \left[1 + (\theta_{ph_T} \cdot V_{eff})^{\nu_T/3} + (\theta_{sr_T} \cdot V_{eff})^{\nu_T}\right]^{1/\nu_T} + C_{s_T} \cdot \left(\frac{\bar{V}_{dep}}{\bar{V}_{dep} + \bar{V}_{inv}}\right)^2 & \text{for PMOS} \end{cases} \quad (15.53)$$

Channel Length Modulation:

$$G_{\Delta L} = 1 - \frac{\Delta L}{L} = 1 - \alpha \cdot \ln\left[\frac{V_{DS} - V_{DS_x} + \sqrt{(V_{DS} - V_{DS_x})^2 + V_p^2}}{V_P}\right] \quad (15.54)$$

Velocity Saturation:

$$x_{sat} = \begin{cases} \dfrac{\theta_{sat_T} \cdot \Delta\psi}{G_{mob}} & \text{for NMOS} \\ \dfrac{\theta_{sat_T}}{G_{mob}} \cdot \dfrac{\Delta\psi}{[1 + (\theta_{sat_T} \cdot \Delta\psi / G_{mob})^2]^{1/4}} & \text{for PMOS} \end{cases} \quad (15.55)$$

$$G_{vsat} = \frac{G_{mob}}{2} \cdot [1 + \sqrt{1 + 2 \cdot x_{sat}{}^2}] \quad (15.56)$$

Series Resistance and Self-Heating:

$$G_R = \theta_{R_T} \cdot \left(1 + \frac{\theta_{R1}}{\theta_{R2} + \overline{V}_{inv}}\right) \cdot \overline{V}^*_{inv} \quad (15.57)$$

$$G_{Th} = \theta_{Th_T} \cdot V_{DS} \cdot \Delta\psi \cdot \overline{V}^*_{inv} \quad (15.58)$$

$$G_{tot} = G_{Th} + \frac{G_{vsat} \cdot G_{\Delta L} + G_R}{2} + \sqrt{\frac{(G_{vsat} \cdot G_{\Delta L} + G_R)^2}{4} - \frac{G_R}{G_{mob}} \cdot \frac{x_{sat}{}^2}{\sqrt{1 + 2 \cdot x_{sat}{}^2}}} \quad (15.59)$$

Drain-Source Channel Current

$$I_{drift} = \beta_T \cdot \overline{V}_{inv} \cdot \Delta\psi \quad (15.60)$$

$$I_{diff} = \beta_T \cdot m_{\phi_T} \cdot (V_{inv_0} - V_{inv_L}) \quad (15.61)$$

$$I_{DS} = \frac{I_{drift} + I_{diff}}{G_{tot}} \tag{15.62}$$

Weak-Avalanche

$$I_{avl} = \begin{cases} 0 & \text{for: } V_{DS} \leq a_3 \cdot V_{DSAT} \\ a_{1_T} \cdot I_{DS} \cdot \exp\left(-\frac{a_2}{V_{DS} - a_3 \cdot V_{DSAT}}\right) & \text{for: } V_{DS} > a_3 \cdot V_{DSAT} \end{cases} \tag{15.63}$$

Surface Potential in Gate Overlap Regions

The surface potential in the overlap region ψ_{ov} is given by the following implicit relation:

$$F_{ov}\{V_{GX}, \psi_{ov}\} = -V_{ov}\{V_{GX}, \psi_{ov}\}^2 + k_{ov}{}^2 \cdot d_{ov}\{\psi_{ov}\} = 0 \tag{15.64}$$

where V_{GX} can be either V_{GS} or V_{GD}, and:

$$V_{ov}\{V_{GX}, \psi_{ov}\} = \begin{cases} V_{GX} - V_{FBov} - \psi_{ov} & \text{for: } V_{GX} - \psi_{ov} \leq V_{FBov} \\ \frac{V_{GX} - V_{FBov} - \psi_{ov}}{1 + \sqrt{1 + 4/k_p{}^2 \cdot (V_{GX} - V_{FBov} - \psi_{ov})}} & \text{for: } V_{GX} - \psi_{ov} > V_{FBov} \end{cases} \tag{15.65}$$

$$d_{ov}\{\psi_{ov}\} = -\psi_{ov} + \phi_T \cdot \left[\exp\left(\frac{\psi_{ov}}{\phi_T}\right) - 1\right] \tag{15.66}$$

The surface potentials in the gate/source overlap ψ_{ov_0} and in the gate/drain ψ_{ov_L} are calculated iteratively using a second-order Newton Raphson procedure from the following implicit relations:

$$F_{ov}\{V_{GS}, \psi_{ov_0}\} = 0 \tag{15.67}$$

$$F_{ov}\{V_{GS}-V_{DS},\psi_{ov_L}\}=0 \tag{15.68}$$

The oxide voltages in the gate/source overlap V_{ov_0} and the gate/drain overlap V_{ov_L} are given by:

$$V_{ov_0}=V_{ov}\{V_{GS},\psi_{ov_0}\} \tag{15.69}$$

$$V_{ov_L}=V_{ov}\{V_{GS}-V_{DS},\psi_{ov_L}\} \tag{15.70}$$

Gate Current Equations

The tunnelling probability is given by:

$$P_{tun}\{V_{ox},\chi_B,B\}=\begin{cases}\exp\left(-B\cdot\dfrac{[1-(1-V_{ox}/\chi_B)^{3/2}]}{V_{ox}}\right) & \textit{for:}\quad V_{ox}<\chi_B\\ \exp(-B/V_{ox}) & \textit{for:}\quad V_{ox}\geq\chi_B\end{cases} \tag{15.71}$$

Source/Drain Gate Overlap Current:

The gate tunnelling currents in both gate/source and gate/drain overlap are given by:

$$P_{ov}\{V_{ov}\}=P_{tun}\{V_{ov},\chi_{B_{inv}},B_{inv}\} \tag{15.72}$$

$$I_{Gov}\{V_{GX},V_{ov}\}=I_{GOV}\cdot V_{GX}\cdot V_{ov}\cdot[P_{ov}\{V_{ov}\}-P_{ov}\{-V_{ov}\}] \tag{15.73}$$

$$I_{Gov_0}=I_{Gov}\{V_{GS},V_{ov_0}\} \tag{15.74}$$

$$I_{Gov_L} = I_{Gov}\{V_{GS} - V_{DS}\,,\ V_{ov_L}\} \tag{15.75}$$

Intrinsic Gate Current

The gate tunnelling current in accumulation:

$$P_{acc} = P_{tun}\{-\overline{V}_{ov}, \chi_{B_{acc}}, B_{acc}\} \tag{15.76}$$

$$I_{GB} = \begin{cases} -I_{GACC} \cdot (V_{GS} + V_{SB}) \cdot \overline{V}_{ox} \cdot P_{acc} & \textit{for:}\quad \overline{V}_{ox} \le 0 \\ 0 & \textit{for:}\quad \overline{V}_{ox} > 0 \end{cases} \tag{15.77}$$

The tunnelling current in inversion (i.e., $V^*_{GB} > 0$), including quantum-mechanical barrier lowering $\Delta\chi_B$:

$$\Delta\chi_B = QM_{\psi} \cdot (\overline{V}_{inv}/3 + \overline{V}_{ox} - \overline{V}_{inv})^{2/3} \tag{15.78}$$

$$\chi_{B_{eff}} = \chi_{B_{inv}} - \Delta\chi_B \tag{15.79}$$

$$B_{eff} = B_{inv} \cdot (\chi_{B_{eff}}/\chi_{B_{inv}})^{3/2} \tag{15.80}$$

$$P_{inv} = P_{tun}\{\overline{V}_{ox}, \chi_{B_{eff}}, B_{eff}\} \tag{15.81}$$

$$r_B = \frac{3}{8} \cdot \frac{B_{eff}}{\chi_{B_{eff}}{}^2} \cdot \frac{\overline{\xi}_{ox}}{\phi_T} \tag{15.82}$$

$$r^* = \frac{\bar{\xi}}{\phi_T \cdot \bar{V}^*_{inv}} \tag{15.83}$$

$$r_{ox} = \frac{\bar{\xi}_{ox}}{\phi_T \cdot \bar{V}_{ox}} \tag{15.84}$$

$$P_{GC} = 1 + \frac{r_B{}^2 + 4 \cdot r_B \cdot r^* + 2 \cdot r_B \cdot r_{ox} + 2 \cdot r^{*2} + 4 \cdot r_{ox} \cdot r^*}{24} \cdot \Delta\psi^2 \tag{15.85}$$

$$\bar{I}_{GC} = I_{GINV} \cdot G_{\Delta L} \cdot \left(V_{GS} - \frac{1}{2} V_{DS_x} \right) \cdot P_{inv} \tag{15.86}$$

The total intrinsic gate current I_{GC} :

$$I_{GC} = \bar{I}_{GC} \cdot \bar{V}_{inv} \cdot P_{GC} \tag{15.87}$$

$$P_{GS} = [r_B + r_{ox}] \cdot \frac{\Delta\psi}{12} \tag{15.88}$$

$$I_{GS} = \frac{1}{2} \cdot I_{GC} + \left(P_{GS} \cdot \bar{V}_{inv} + \frac{V_{inv_0} - V_{inv_L}}{12} \right) \cdot \bar{I}_{GC} + I_{Gov_0} \tag{15.89}$$

$$I_{GD} = I_{GC} - I_{GS} + I_{Gov_0} + I_{Gov_L} \tag{15.90}$$

Gate-Induced Drain/Source Leakage Current:

$$V_{tov}\{V_{ov}, V\} = \sqrt{V_{ov}{}^2 + C_{GIDL}{}^2 \cdot V^2} \tag{15.91}$$

$$I_{gixl}\{V_{ov}, V\} = A_{GIDL} \cdot V \cdot V_{tov}\{V_{ov}, V\}^{2} \cdot \exp\left(-\frac{B_{GIDL_T}}{V_{tov}\{V_{ov}, V\}}\right) \quad (15.92)$$

$$I_{gisl} = I_{gixl}\{V_{ov_0}, V_{SB}\} \quad (15.93)$$

$$I_{gidl} = I_{gixl}\{V_{ov_L}, V_{DS} + V_{SB}\} \quad (15.94)$$

Basic Charge Equations

Bias-Dependent Overlap Capacitance:

$$Q_{ov_0} = C_{GSO} \cdot V_{ov_0} \quad (15.95)$$

$$Q_{ov_L} = C_{GDO} \cdot V_{ov_L} \quad (15.96)$$

Intrinsic Charges:

$$C_{OX_{eff}} = \frac{C_{OX} \cdot G_{\Delta L}}{1 + QM_{t_{ox}} \cdot \left[\frac{V_{eff}}{\eta_{mob_T}}\right]^{-1/3}} \quad (15.97)$$

$$\Delta V_{inv} = (V_{inv_0} - V_{inv_L}) \cdot \left(1 - \frac{G_R}{G_{tot}}\right) \quad (15.98)$$

$$F_j = \frac{1}{2} \cdot \frac{\Delta V_{inv}}{\overline{V}^{*}_{inv}} \quad (15.99)$$

$$Q_S = -\frac{C_{OX_{eff}}}{2} \cdot \left[\overline{V}_{inv} + \frac{\Delta V_{inv}}{6} \cdot \left(F_j - \frac{F_j^2}{5} + 1 \right) \right] \tag{15.100}$$

$$Q_D = -\frac{C_{OX_{eff}}}{2} \cdot \left[\overline{V}_{inv} + \frac{\Delta V_{inv}}{6} \cdot \left(F_j + \frac{F_j^2}{5} - 1 \right) \right] \tag{15.101}$$

$$Q_G = C_{OX_{eff}} \cdot \left[\overline{V}_{ox} + \frac{\Delta V_{inv}}{6} \cdot F_j \cdot \frac{\overline{\xi}_{ox}}{\overline{\xi}} \right] \tag{15.102}$$

$$Q_B = -[Q_S + Q_D + Q_G] \tag{15.103}$$

Noise Equations

In these equations f represents the operation frequency of the transistor.

$$G_{eff} = 1 - \frac{G_R}{G_{tot}} \tag{15.104}$$

$$x_{sat}^{\ 2} = \begin{cases} \theta_{sat_T}^{\ 2} \cdot \Delta\psi^2 \cdot G_{eff}^{\ 2} & \text{for NMOS} \\ \dfrac{\theta_{sat_T}^{\ 2} \cdot \Delta\psi^2 \cdot G_{eff}^{\ 2}}{\sqrt{1 + \theta_{sat_T}^{\ 2} \cdot \Delta\psi^2 \cdot G_{eff}^{\ 2}}} & \text{for PMOS} \end{cases} \tag{15.105}$$

$$G_{vsat_R} = \frac{G_{mob} + \sqrt{G_{mob}^{\ 2} + 2 \cdot x_{sat}^{\ 2}}}{2} \tag{15.106}$$

$$t_1 = \frac{\overline{V}_{inv}}{\overline{V}^*_{inv}} \tag{15.107}$$

$$t_2 = \frac{F_j^{\,2}}{36} \tag{15.108}$$

$$t_{sat} = \frac{x_{sat}^{\,2}}{G_{vsat_R}^{\,2}} \tag{15.109}$$

$$g_{ideal} = \frac{\beta_T \cdot \overline{V}^*_{inv}}{G_{vsat_R} \cdot G_{\Delta L}} \tag{15.110}$$

$$S_{th} = N_{T_T} \cdot G_{eff}^{\,2} \cdot g_{ideal} \cdot max\{t_1 + 12 \cdot t_2 \cdot (1 - 2 \cdot t_{sat} - 2 \cdot t_{sat}^{\,2}), 0\} \tag{15.111}$$

$$C_{G_{eff}} = C_{OX_{eff}} \cdot \frac{\bar{\xi}_{ox}}{\phi_T} \cdot \frac{G_{vsat_R} \cdot G_{\Delta L}}{G_{mob}} \tag{15.112}$$

$$\begin{aligned} m_{ig} = \frac{1}{g_{ideal}} \cdot \Bigg[& \frac{t_1}{12} - t_1 \cdot t_2 - \frac{t_2}{5} + 12 \cdot t_2^{\,2} \\ & + t_{sat} \cdot \left(\frac{t_1}{12} + 3 \cdot t_1 \cdot t_2 - \frac{9 \cdot t_2}{5} - 36 \cdot t_2^{\,2} \right) \\ & + t_{sat}^{\,2} \cdot \left(\frac{t_1}{12} + 4 \cdot t_1 \cdot t_2 - \frac{17 \cdot t_2}{5} - 24 \cdot t_2^{\,2} \right) \Bigg] \end{aligned} \tag{15.113}$$

$$m_{igh} = G_{eff} \cdot \sqrt{t_2} \cdot \left[1 - 12 \cdot t_2 + t_{sat} \cdot \left(\frac{1}{2} - t_1 + 30 \cdot t_2 \right) + t_{sat}^{\,2} \cdot \left(\frac{3}{8} - \frac{3 \cdot t_1}{2} + \frac{51 \cdot t_2}{2} \right) \right] \tag{15.114}$$

$$S_{ig} = N_{T_T} \cdot (2 \cdot \pi \cdot f \cdot C_{G_{eff}})^2 \cdot m_{ig} \tag{15.115}$$

$$S_{igth} = j \cdot N_{T_T} \cdot 2 \cdot \pi \cdot f \cdot C_{G_{eff}} \cdot m_{igth} \tag{15.116}$$

$$\textit{for GATENOISE=1:} \quad \begin{cases} g_{ideal} = \dfrac{\beta_T \cdot \overline{V}_{inv}}{G_{mob} \cdot G_{\Delta L}} \\ S_{th} = N_{T_T} \cdot G_{eff}^{\,2} \cdot g_{ideal} / \sqrt{1 + t_{sat} + t_{sat}^{\,2}} \\ S_{ig} = 0 \\ S_{igth} = 0 \end{cases} \tag{15.117}$$

$$N_0 = \frac{\varepsilon_{ox}}{q \cdot t_{ox}} \cdot \left(\overline{V}_{inv} + \frac{\Delta V_{inv}}{2} \right) \tag{15.118}$$

$$N_L = \frac{\varepsilon_{ox}}{q \cdot t_{ox}} \cdot \left(\overline{V}_{inv} + \frac{\Delta V_{inv}}{2} \right) \tag{15.119}$$

$$N^* = \frac{\varepsilon_{ox}}{q \cdot t_{ox}} \cdot \bar{\xi} \tag{15.120}$$

$$S_{fl} = \frac{q \cdot \phi_T{}^2 \cdot t_{ox} \cdot \beta_T \cdot I_{DS}}{f \cdot \varepsilon_{ox} \cdot G_{vsat} \cdot N^*} \cdot \left[(N_{FA} - N^* \cdot N_{FB} + N^{*2} \cdot N_{FC}) \cdot \ln\left(\frac{N_0 + N^*}{N_L + N^*}\right) \right.$$

$$\left. + (N_{FB} - N^* \cdot N_{FC}) \cdot (N_0 - N_L) + \frac{N_{FC}}{2} \cdot (N_0{}^2 - N_L{}^2) \right]$$

$$+ \frac{\phi_T \cdot I_{DS}{}^2}{f} \cdot (1 - G_{\Delta L}) \cdot \left[\frac{N_{FA} + N_{FB} \cdot N_L + N_{FC} \cdot N_L{}^2}{(N_L + N^{*2})} \right]$$

15.3 Symbols, parameters and constants

The symbolic representation and the recommended programming names of the quantities listed in the following sections, have been chosen in such a way to express their purpose and relations to other quantities and to preclude ambiguity and inconsistency.

15.3.1 Glossary of used symbols

All parameters which refer to the reference transistor and/or the reference temperature have a symbol with the subscript R and a programming name ending with R. All characters 0 (zero) in subscripts of parameters are represented by the capital letter O in the programming name, because they are often distinguishable with great difficulty! Scaling parameters are indicated by *S* with a subscript where the variables on which the parameter depends, preceed a semicolon whereas the parameter succeeds it, e.g. $S_{T;\theta sr}$.

Note that since the list of parameters for an individual transistor (i.e. the so-called miniset parameters) and the list of physical constants can be found in sections titled *Parameters of the electrical model on page 94* and *Model constants on page 105*, respectively, they will not be repeated here.

List of numerical constants

No.	Constant	Prog. Name	Value
1	A	LN_MINDOUBLE	-800

List of circuit simulator variables

No.	Symbol	Prog. Name	Units	Description
1	L	L	m	Drawn channel length in the lay-out of the actual transistor
2	W	W	m	Drawn channel width in the lay-out of the actual transistor
3	T_A	TA	°C	Ambient circuit temperature
4	f	F	s^{-1}	Operation frequency

External Electrical Variables

The definitions of the external electrical variables are illustrated in Figure 69.

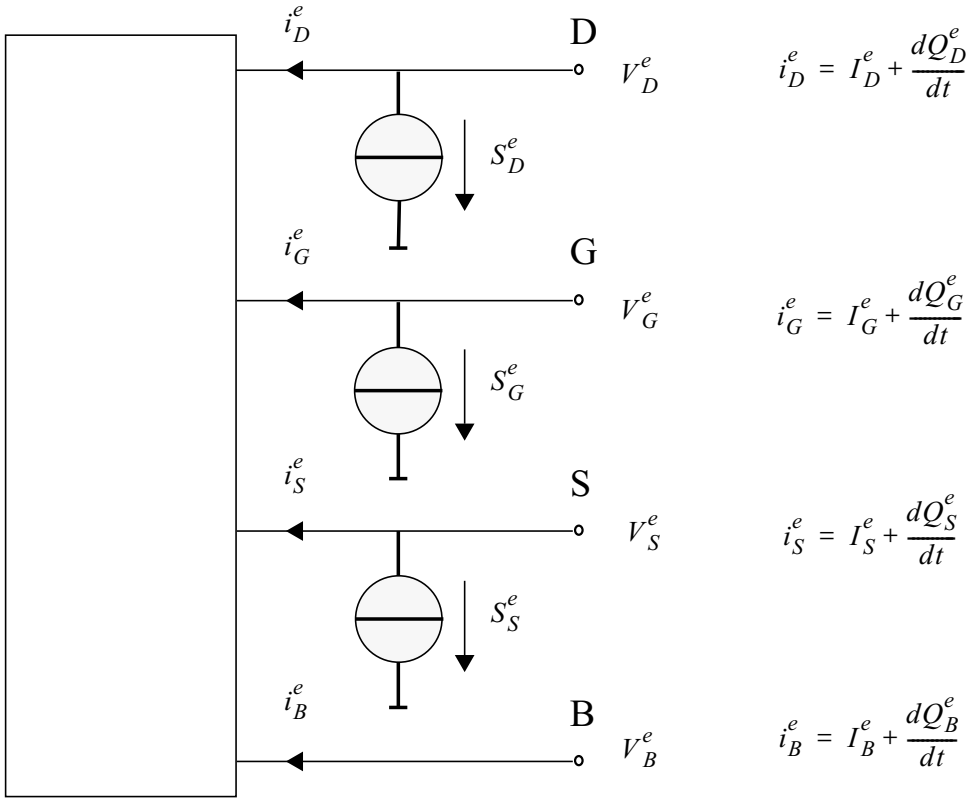


Figure 69: Definition of the external electrical quantities and variables.

No.	Variable	Prog. Name	Units	Description
1	V_D^e	VDE	V	Potential applied to the drain node
2	V_G^e	VGE	V	Potential applied to the gate node
3	V_S^e	VSE	V	Potential applied to the source node
4	V_B^e	VBE	V	Potential applied to the bulk node

No.	Variable	Prog. Name	Units	Description
5	I_D^e	IDE	A	DC current into the drain
6	I_G^e	IGE	A	DC current into the gate
7	I_S^e	ISE	A	DC current into the source
8	I_B^e	IBE	A	DC current into the bulk
9	Q_D^e	QDE	C	Charge in the device attributed to the drain node
10	Q_G^e	QGE	C	Charge in the device attributed to the gate node
11	Q_S^e	QSE	C	Charge in the device attributed to the source node
12	Q_B^e	QBE	C	Charge in the device attributed to the bulk node
13	S_D^e	SDE	A^2s	Spectral density of the noise current into the drain
14	S_G^e	SGE	A^2s	Spectral density of the noise current into the gate
15	S_S^e	SSE	A^2s	Spectral density of the noise current into the source
16	S_{DG}^e	SDGE	A^2s	Cross spectral density between the drain and the gate noise currents
17	S_{GS}^e	SGSE	A^2s	Cross spectral density between the gate and the source noise currents
18	S_{SD}^e	SSDE	A^2s	Cross spectral density between the source and the drain noise currents

Internal Electrical Variables

No.	Variable	Progr. Name	Units	Description
1	V_{DS}	VDS	V	Drain-to-source voltage applied to the equivalent n-MOST
2	V_{GS}	VGS	V	Gate-to-source voltage applied to the equivalent n-MOST
3	V_{SB}	VSB	V	Source-to-bulk voltage applied to the equivalent n-MOST
4	I_{DS}	IDS	A	DC current through the channel flowing from drain to source
5	I_{AVL}	IAVL	A	DC current flowing from drain to bulk due to the weak-avalanche effect
6	I_{GS}	IGS	A	DC current flowing from gate to source due to the direct tunnelling effect
7	I_{GD}	IGD	A	DC current flowing from gate to drain due to the direct tunnelling effect
8	I_{GB}	IGB	A	DC current flowing from gate to bulk due to the direct tunnelling effect
9	I_{GISL}	IGISL	A	DC current flowing from source to bulk due to the gate-induced source leakage effect
10	I_{GIDL}	IGIDL	A	DC current flowing from drain to bulk due to the gate-induced source leakage effect
11	Q_D	QD	C	Charge in the equivalent n-MOST attributed to the drain node
12	Q_G	QG	C	Charge in the equivalent n-MOST attributed to the gate node
13	Q_S	QS	C	Charge in the equivalent n-MOST attributed to the source node
14	Q_B	QB	C	Charge in the equivalent n-MOST attributed to the bulk node
15	Q_{ov0}	QOVO	C	Extrinsic charge in the equivalent n-MOST attributed to the gate-source overlap

16	Q_{ovL}	QOVL	C	Extrinsic charge in the equivalent n-MOST attributed to the gate-drain overlap
17	S_{th}	STH	A^2s	Spectral density of the thermal-noise current of the channel
18	S_{fl}	SFL	A^2s	Spectral density of the flicker-noise current of the channel
19	S_{ig}	SIG	A^2s	Spectral density of the noise current induced in the gate
20	S_{igth}	SIGTH	A^2s	Cross spectral density of the noise current induced in the gate and the thermal-noise current of the channel

15.3.2 Parameters

In MOS Model 11, level 1102, parameter binning has been facilitated by adding a second, separate set of geometry scaling rules. Consequently, besides the physical geometrical scaling rules there is also a set of binning geometrical scaling rules. The physical geometry scaling rules of Level 1102 (see the sections titled *Parameters for physical geometry scaling on page 43* and *Calculation of Geometry-Dependent Parameters using the Physical Scaling Rules on page 110*), have been developed to give a good description over the whole geometry range of CMOS technologies. For processes under development, however, it is sometimes useful to have more flexible scaling relations. In this case one could opt for a binning strategy, where the accuracy with geometry is mostly determined by the number of bins used. The physical scaling rules of Level 1102 are not straightforwardly applicable to binning strategies, since they may result in discontinuities in parameter values at the bin boundaries. Consequently, special binning geometrical scaling relations have been developed (see the sections titled *Parameters for Binning Geometrical Scaling on page 61* and *Calculation of Geometry-Dependent Parameters using the Binning Scaling Rules on page 115*), which guarantee continuity in the model parameters at the bin boundaries. It should be noted that using the source code of the Modelkit on the Philips' website (which can be found at http://www.semiconductors.philips.com/Philips_Models)

1. the physical geometry scaling rules can be selected by using Level 11020, while
2. the binning geometry scaling rules can be selected by using Level 11021.

Parameters for physical geometry scaling

- These parameters correspond to the geometrical model (MN, MP, MOS 11020)**.**

Symbol	Progr. Name	Units	Description
	LEVEL	-	Must be 11020
ΔL_{PS}	LVAR	m	Difference between the actual and the programmed poly-silicon gate length
$\Delta L_{overlap}$	LAP	m	Effective channel length reduction per side due to the lateral diffusion of the source/drain dopant ions
ΔW_{OD}	WVAR	m	Difference between the actual and the programmed field-oxide opening
ΔW_{narrow}	WOT	m	Effective reduction of the channel width per side due to the lateral diffusion of the channel-stop dopant ions

Symbol	Progr. Name	Units	Description
T_R	TR	°C	Reference temperature
V_{FB}	VFB	V	Flat-band voltage at the reference temperature
$S_{T;V_{FB}}$	STVFB	VK^{-1}	Coefficient of the temperature dependence of V_{FB}
k_{0R}	KOR	$V^{1/2}$	Body-effect factor for an infinite square transistor
$S_{L;k_0}$	SLKO	-	Coefficient of the length dependence of k_0
$S_{L2;k_0}$	SL2KO	-	Second coefficient of the length dependence of k_0
$S_{L3;k_0}$	SL3KO	-	Third coefficient of the length dependence of k_0
	SL3KOEXP	-	Exponent belonging to the third coefficient of the length dependence of k_0
$S_{W;k_0}$	SWKO	-	Coefficient of the width dependence of k_0
$1/k_p$	KPINV	$V^{-1/2}$	Inverse of body-effect factor of the polysilicon gate
ϕ_{BR}	PHIBR	V	Surface potential at the onset of strong inversion at the reference temperature
$S_{T;\phi_B}$	STPHIB	VK^{-1}	Coefficient of the temperature dependence of ϕ_B
$S_{L;\phi_B}$	SLPHIB	-	Coefficient of the length dependence of ϕ_B
$S_{L2;\phi_B}$	SL2PHIB	-	Second coefficient of the length dependence of ϕ_B
$S_{W;\phi_B}$	SWPHIB	-	Coefficient of the width dependence of ϕ_B
β_{sq}	BETSQ	AV^{-2}	Gain factor for an infinite square transistor at the reference temperature
$\eta_{\beta R}$	ETABETR	-	Exponent of the temperature dependence of the gain factor of an infinite square transistor

Symbol	Progr. Name	Units	Description
$S_{L;\eta_\beta}$	SLETABET	-	Coefficient of the length dependence of $\eta_{\beta R}$
$f_{\beta,1}$	FBET1	-	Relative mobility decrease due to first lateral profile
$L_{P,1}$	LP1	m	Characteristic length of first lateral profile
$f_{\beta,2}$	FBET2	-	Relative mobility decrease due to second lateral profile
$L_{P,2}$	LP2	m	Characteristic length of second lateral profile
θ_{srR}	THESRR	V^{-1}	Coefficient of the mobility reduction due to surface roughness scattering for an infinite square transistor at the reference temperature
η_{sr}	ETASR	-	Exponent of the temperature dependence of θ_{sr}
$S_{W;\theta_{sr}}$	SWTHESR	-	Coefficient of the width dependence of θ_{sr}
θ_{phR}	THEPHR	V^{-1}	Coefficient of the mobility reduction due to phonon scattering for an infinite square transistor at the reference temperature
η_{ph}	ETAPH	-	Exponent of the temperature dependence of θ_{ph} for the reference transistor
$S_{W;\theta_{ph}}$	SWTHEPH	-	Coefficient of the width dependence of θ_{ph}
η_{mobR}	ETAMOBR	-	Effective field parameter for dependence on depletion/ inversion charge for an infinite square transistor
$S_{T;\eta_{mob}}$	STETAMOB	K^{-1}	Coefficient of the temperature dependence of η_{mob}
$S_{W;\eta_{mob}}$	SWETAMOB	-	Coefficient of the width dependence of η_{mob}

Symbol	Progr. Name	Units	Description
υ	NU	-	Exponent of the field dependence of the mobility model at the reference temperature
υ_{EXP}	NUEXP	-	Exponent of the temperature dependence of parameter ν
C_S	CS	-	Coefficient of Coulomb scattering
C_{sR}	CSR	-	Prefactor of scaling rule for C_S
$S_{L;C_s}$	SLCS	-	Coefficient of the length dependence of C_S
C_{sEXP}	CSEXP	-	Exponent of the length dependence of C_S
$S_{W;C_s}$	SWCS	-	Coefficient of the width dependence of C_S
η_{C_s}	ETACS	-	Exponent of the temperature dependence of C_S
θ_{RR}	THERR	V^{-1}	Coefficient of the series resistance per unit length for an infinitely wide transistor
η_R	ETAR	-	Exponent of the temperature dependence of θ_R
$S_{W;\theta_R}$	SWTHER	-	Coefficient of the width dependence of θ_R
θ_{R1}	THER1	V	Numerator of the gate voltage dependent part of series resistance
θ_{R2}	THER2	V	Denominator of the gate voltage dependent part of series resistance
θ_{satR}	THESATR	V^{-1}	Velocity saturation parameter due to optical/acoustic phonon scattering for an infinite square transistor at the reference temper-ature
η_{sat}	ETASAT	-	Exponent of the temperature dependence of θ_{sat}
$S_{L;\theta_{sat}}$	SLTHESAT	-	Coefficient of the length dependence of θ_{sat}
θ_{satEXP}	THESATEXP	-	Exponent of the length dependence of θ_{sat}

Symbol	Progr. Name	Units	Description
$S_{W;\theta_{sat}}$	SWTHESAT	-	Coefficient of the width dependence of θ_{sat}
θ_{ThR}	THETHR	V^{-3}	Coefficient of self-heating per unit length for an infinitely wide transistor at the reference temperature
θ_{ThEXP}	THETHEXP	-	Exponent of the length dependence of θ_{Th}
$S_{W;\theta_{Th}}$	SWTHETH	-	Coefficient of the width dependence of θ_{Th}
σ_{dibl0}	SDIBLO	$V^{-1/2}$	Drain-induced barrier-lowering parameter per unit length
$\sigma_{diblEXP}$	SDIBLEXP	-	Exponent of the length dependence of σ_{dibl}
m_{00}	MOO	-	Parameter for short-channel subthreshold slope
m_{0R}	MOR	-	Parameter for short-channel subthreshold slope per unit length
m_{0EXP}	MOEXP	-	Exponent of the length dependence of m_0
σ_{sfR}	SSFR	$V^{-1/2}$	Static feedback parameter for an infinite square transistor
$S_{L;\sigma_{sf}}$	SLSSF	-	Coefficient of the length dependence of σ_{sf}
$S_{W;\sigma_{sf}}$	SWSSF	-	Coefficient of the width dependence of σ_{sf}
α_R	ALPR	-	Factor of the channel length modulation for an infinite square transistor
$S_{L;\alpha}$	SLALP	-	Coefficient of the length dependence of α
α_{EXP}	ALPEXP	-	Exponent of the length dependence of α
$S_{W;\alpha}$	SWALP	-	Coefficient of the width dependence of α
V_P	VP	V	Characteristic voltage of the channel length modulation
L_{min}	LMIN	m	Minimum effective channel length in technology, used for calculation of smoothing factor *m*

Symbol	Progr. Name	Units	Description
a_{1R}	A1R	-	Factor of the weak-avalanche current for an infinite square transistor at the reference temperature
$S_{T;a_1}$	STA1	K^{-1}	Coefficient of the temperature dependence of a_1
$S_{L;a_1}$	SLA1	-	Coefficient of the length dependence of a_1
$S_{W;a_1}$	SWA1	-	Coefficient of the width dependence of a_1
a_{2R}	A2R	V	Exponent of the weak-avalanche current for an infinite square transistor
$S_{L;a_2}$	SLA2	-	Coefficient of the length dependence of a_2
$S_{W;a_2}$	SWA2	-	Coefficient of the width dependence of a_2
a_{3R}	A3R	-	Factor of the drain-source voltage above which weak-avalanche occurs, for an infinite square transistor
$S_{L;a_3}$	SLA3	-	Coefficient of the length dependence of a_3
$S_{W;a_3}$	SWA3	-	Coefficient of the width dependence of a_3
I_{GINVR}	IGINVR	AV^{-2}	Gain factor for intrinsic gate tunnelling current in inversion for a channel area of $1\mu m^2$
B_{inv}	BINV	V	Probability factor for intrinsic gate tunnelling current in inversion
I_{GACCR}	IGACCR	AV^{-2}	Gain factor for intrinsic gate tunnelling current in accumulation for a channel area of $1\mu m^2$
B_{acc}	BACC	V	Probability factor for intrinsic gate tunnelling current in accumulation
V_{FBov}	VFBOV	V	Flat-band voltage for the source/drain overlap extensions
k_{ov}	KOV	$V^{1/2}$	Body-effect factor for the source/drain overlap extensions

Symbol	Progr. Name	Units	Description
I_{GOVR}	IGOVR	AV^{-2}	Gain factor for source/drain overlap gate tunnelling current for a channel width of $1\mu m$
A_{GIDLR}	AGIDLR	AV^{-3}	Gain factor for gate-induced drain leakage current for a channel width of 1 m
B_{GIDL}	BGIDL	V	Probability factor for gate-induced drain leakage current at the reference temperature
$S_{T;B_{GIDL}}$	STBGIDL	VK^{-1}	Coefficient of the temperature dependence of BGIDL
C_{GIDL}	CGIDL	-	Factor for the lateral field dependence of the gate-induced drain leakage current
t_{ox}	TOX	m	Thickness of the gate-oxide layer.
C_{ol}	COL	F	Gate overlap capacitance for a channel width of $1\mu m$
-	GATENOISE	-	Flag for in/exclusion of induced gate thermal noise
N_T	NT	J	Coefficient of the thermal noise at the reference temperature
N_{FAR}	NFAR	$V^{-1}m^{-4}$	First coefficient of the flicker noise for a channel area of $1\mu m^2$
N_{FBR}	NFBR	$V^{-1}m^{-2}$	Second coefficient of the flicker noise for a channel area of $1\mu m^2$
N_{FCR}	NFCR	V^{-1}	Third coefficient of the flicker noise for a channel area of $1\mu m^2$
ΔT_A	DTA	K	Temperature offset of the device with respect to T_A
RG0	RGO	Ω	Gate Resistance
RINT	RINT	$\Omega\,m^2$	Contact resistance between silicide and poly
RVPOLY	RVPOLY	$\Omega\,m^2$	Vertical poly resistance

Symbol	Progr. Name	Units	Description
RSHG	RSHG	Ω/□	Gate electrode diffusion sheet resistance
DLSIL	DLSIL	m	Silicide extension over the physical gate length

The additional parameters for the model including self-heating (see section 15.6 on page 153) are listed in the table below.

Symbol	Progr. Name	Units	Description
R_{Th}	RTH	^{o}C/W	Thermal resistance
C_{Th}	CTH	J/^{o}C	Thermal capacitance
A_{TH}	ATH	-	Temperature coefficient of the thermal resistance

The instance parameters are listed in the table below.

Symbol	Progr. Name	Units	Description
L	L	m	Drawn channel length in the lay-out of the actual transistor
W	W	m	Drawn channel width in the lay-out of the actual transistor
N_{MULT}	MULT	-	Number of devices in parallel
NF	NF	-	Number of fingers
NGCON	NGCON	-	Number of gate contacts
XGW	XGW	m	Distance from the gate contact to the channel edge

Remark: The parameters *L, W*, and *DTA* are used to calculate the electrical parameters of the actual transistor, as specified in the section on parameter preprocessing.

Default and clipping values (physical geometrical model)

The default values and clipping values as used for the parameters of the physical geometrical MOS model, level 1102 (n-channel) are listed below.

Parameter	Units	Default	Clip low	Clip high
LEVEL	-	11020	-	-
LVAR	m	0.000	-	-
LAP	m	4.0×10^{-8}	-	-
WVAR	m	0.000	-	-
WOT	m	0.000	-	-
TR	°C	21.0	-273.0	-
VFB	V	-1.050	-	-
STVFB	VK^{-1}	0.5×10^{-3}	-	-
KOR	$V^{1/2}$	0.500	-	-
SLKO	-	0.000	-	-
SL2KO	-	0.000	-	-
SL3KO	-	0.000	-	-
SL3KOEXP	-	1.000	-	-
SWKO	-	0.000	-	-
KPINV	$V^{-1/2}$	0.000	-	-
PHIBR	V	0.950	-	-
STPHIB	VK^{-1}	-8.5×10^{-4}	-	-
SLPHIB	-	0.000	-	-
SL2PHIB	-	0.000	-	-
SWPHIB	-	0.000	-	-
BETSQ	AV^{-2}	3.709×10^{-4}	-	-
ETABETR	-	1.300	-	-
SLETABET	-	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
FBET1	-	0.000	-	-
LP1	m	0.8×10^{-6}	1.0×10^{-10}	-
FBET2	-	0.000	-	-
LP2	m	0.8×10^{-6}	1.0×10^{-10}	-
THESRR	V^{-1}	0.400	-	-
ETASR	-	0.650	-	-
SWTHESR	-	0.000	-	-
THEPHR	V^{-1}	1.29×10^{-2}	-	-
ETAPH	-	1.350	-	-
SWTHEPH	-	0.000	-	-
ETAMOBR	-	1.40	-	-
STETAMOB	K^{-1}	0.000	-	-
SWETAMOB	-	0.000	-	-
NU	-	2.000	1.000	100
NUEXP	-	5.250	-	-
CS	-	0	0	-
CSR	-	0.000	-	-
SLCS	-	0.000	-	-
CSEXP	-	1.000	0	-
SWCS	-	0.000	-	-
ETACS	-	0.000	-	-
THERR	V^{-1}	0.155	1.0×10^{-10}	-
ETAR	-	0.950	-	-
SWTHER	-	0.000	-	-
THER1	V	0.000	-	-
THER2	V	1.000	-	-

Parameter	Units	Default	Clip low	Clip high
THESATR	V^{-1}	0.500	-	-
ETASAT	-	1.040	-	-
SLTHESAT	-	1.000	-	-
THESATEXP	-	1.000	0.000	-
SWTHESAT	-	0.000	-	-
THETHR	V^{-3}	1.0×10^{-3}	-	-
THETHEXP	-	1.000	0.000	-
SWTHETH	-	0.000	-	-
SDIBLO	$V^{-1/2}$	1.0×10^{-4}	-	-
SDIBLEXP	-	1.350	-	-
MOO	-	0.000	-	-
MOR	-	0.000	-	-
MOEXP	-	1.340	-	-
SSFR	$V^{-1/2}$	6.25×10^{-3}	-	-
SLSSF	-	1.000	-	-
SWSSF	-	0.000	-	-
ALPR	-	1.0×10^{-2}	-	-
SLALP	-	1.000	-	-
ALPEXP	-	1.000	0.000	-
SWALP	-	0.000	-	-
VP	V	5.0×10^{-2}	-	-
LMIN	m	1.5×10^{-7}	1.0×10^{-10}	2.5×10^{-6}
A1R	-	6.000	-	-
STA1	K^{-1}	0.000	-	-
SLA1	-	0.000	-	-
SWA1	-	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
A2R	V	38.00	-	-
SLA2	-	0.000	-	-
SWA2	-	0.000	-	-
A3R	-	1.000	-	-
SLA3	-	0.000	-	-
SWA3	-	0.000	-	-
IGINVR	AV^{-2}	0.000	0.000	-
BINV	V	48.00	0.000	-
IGACCR	AV^{-2}	0.000	0.000	-
BACC	V	48.00	0.000	-
VFBOV	V	0.000	-	-
KOV	$V^{1/2}$	2.500	1.0×10^{-12}	-
IGOVR	AV^{-2}	0.000	0.000	-
AGIDLR	AV^{-3}	0.000	0.000	-
BGIDL	V	41.00	0.000	-
STBGIDL	VK^{-1}	$-3.638X10^{-4}$	-	-
CGIDL	-	0.000	0.000	-
TOX	m	3.2×10^{-9}	1.0×10^{-12}	-
COL	F	3.2×10^{-16}	-	-
GATENOISE	-	0.000	0.000	1.000
NT	J	1.624×10^{-20}	0.000	-
NFAR	$V^{-1}m^{-4}$	1.573×10^{23}	-	-
NFBR	$V^{-1}m^{-2}$	4.752×10^{9}	-	-
NFCR	V^{-1}	0.000	-	-
DTA	K	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
RGO	Ω	0.0	-	-
RINT	$\Omega\,m^2$	0.0	0.0	-
RVPOLY	$\Omega\,m^2$	0.0	0.0	-
RSHG	Ω/□	0.0	0.0	-
DLSIL	m	0.0	-	-

The additional values and clipping values of the additional parameters for the (**n-channel**) model including self-heating (see section 15.6 on page 153) are listed in the table below.

Parameter	Units	Default	Clip low	Clip high
RTH	$^oC/W$	300.0	0.000	-
CTH	$J/^oC$	3.0×10^{-9}	0.000	-
ATH	-	0.0	-	-

The instance parameters are listed in the table below.

Parameter	Units	Default	Clip low	Clip high
L	m	2.000×10^{-6}	-	-
W	m	1.000×10^{-5}	-	-
MULT	-	1.000	0.000	-
NF	-	1.0	1.0	-
NGCON	-	1.0	1.0	2.0
XGW	m	$1.0\text{x}10^{-7}$	-	-

Remark: The parameters *L, W*, and *DTA* are used to calculate the electrical parameters of the actual transistor, as specified in the section on parameter preprocessing.

The default values and clipping values as used for the parameters of the physical geometrical MOS model, level 1102 (p-channel) are listed below.

Parameter	Units	Default	Clip low	Clip high
LEVEL	-	11020	-	-
LVAR	m	0.000	-	-
LAP	m	4.0×10^{-8}	-	-
WVAR	m	0.000	-	-
WOT	m	0.000	-	-
TR	°C	21.0	-273.0	-
VFB	V	-1.050	-	-
STVFB	VK^{-1}	0.5×10^{-3}	-	-
KOR	$V^{1/2}$	0.500	-	-
SLKO	-	0.000	-	-
SL2KO	-	0.000	-	-
SL3KO	-	0.000	-	-
SL3KOEXP	-	1.000	-	-
SWKO	-	0.000	-	-
KPINV	$V^{-1/2}$	0.000	-	-
PHIBR	V	0.950	-	-
STPHIB	VK^{-1}	-8.5×10^{-4}	-	-
SLPHIB	-	0.000	-	-
SL2PHIB	-	0.000	-	-
SWPHIB	-	0.000	-	-
BETSQ	AV^{-2}	1.150×10^{-4}	-	-
ETABETR	-	0.500	-	-
SLETABET	-	0.000	-	-
FBET1	-	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
LP1	m	0.8×10^{-6}	1.0×10^{-10}	-
FBET2	-	0.000	-	-
LP2	m	0.8×10^{-6}	1.0×10^{-10}	-
THESRR	V^{-1}	0.730	-	-
ETASR	-	0500	-	-
SWTHESR	-	0.000	-	-
THEPHR	V^{-1}	1.0×10^{-3}	-	-
ETAPH	-	3.750	-	-
SWTHEPH	-	0.000	-	-
ETAMOBR	-	3.000	-	-
STETAMOB	K^{-1}	0.000	-	-
SWETAMOB	-	0.000	-	-
NU	-	2.000	1.000	100
NUEXP	-	3.230	-	-
CS	-	0	0	-
CSR	-	0.000	-	-
SLCS	-	0.000	-	-
CSEXP	-	1.000	0	-
SWCS	-	0.000	-	-
ETACS	-	0.000	-	-
THERR	V^{-1}	0.080	1.0×10^{-10}	-
ETAR	-	0.400	-	-
SWTHER	-	0.000	-	-
THER1	V	0.000	-	-
THER2	V	1.000	-	-
THESATR	V^{-1}	0.200	-	-

Parameter	Units	Default	Clip low	Clip high
ETASAT	-	0.860	-	-
SLTHESAT	-	1.000	-	-
THESATEXP	-	1.000	0.000	-
SWTHESAT	-	0.000	-	-
THETHR	V^{-3}	0.5×10^{-3}	-	-
THETHEXP	-	1.000	0.000	-
SWTHETH	-	0.000	-	-
SDIBLO	$V^{-1/2}$	1.0×10^{-4}	-	-
SDIBLEXP	-	1.350	-	-
MOO	-	0.000	-	-
MOR	-	0.000	-	-
MOEXP	-	1.340	-	-
SSFR	$V^{-1/2}$	6.25×10^{-3}	-	-
SLSSF	-	1.000	-	-
SWSSF	-	0.000	-	-
ALPR	-	1.0×10^{-2}	-	-
SLALP	-	1.000	-	-
ALPEXP	-	1.000	0.000	-
SWALP	-	0.000	-	-
VP	V	5.0×10^{-2}	-	-
LMIN	m	1.5×10^{-7}	1.0×10^{-10}	2.5×10^{-6}
A1R	-	6.000	-	-
STA1	K^{-1}	0.000	-	-
SLA1	-	0.000	-	-
SWA1	-	0.000	-	-
A2R	V	38.00	-	-

Parameter	Units	Default	Clip low	Clip high
SLA2	-	0.000	-	-
SWA2	-	0.000	-	-
A3R	-	1.000	-	-
SLA3	-	0.000	-	-
SWA3	-	0.000	-	-
IGINVR	AV^{-2}	0.000	0.000	-
BINV	V	87.50	0.000	-
IGACCR	AV^{-2}	0.000	0.000	-
BACC	V	48.00	0.000	-
VFBOV	V	0.000	-	-
KOV	$V^{1/2}$	2.500	1.0×10^{-12}	-
IGOVR	AV^{-2}	0.000	0.000	-
AGIDLR	AV^{-3}	0.000	0.000	-
BGIDL	V	41.00	0.000	-
STBGIDL	VK^{-1}	$-3.638X10^{-4}$	-	-
CGIDL	-	0.000	0.000	-
TOX	m	3.2×10^{-9}	1.0×10^{-12}	-
COL	F	3.2×10^{-16}	-	-
GATENOISE	-	0.000	0.000	1.000
NT	J	1.656×10^{-20}	0.000	-
NFAR	$V^{-1}m^{-4}$	3.825×10^{24}	-	-
NFBR	$V^{-1}m^{-2}$	1.015×10^{9}	-	-
NFCR	V^{-1}	7.300×10^{-8}	-	-
DTA	K	0.000	-	-
RGO	Ω	0.0	-	-

Parameter	Units	Default	Clip low	Clip high
RINT	$\Omega\,m^2$	0.0	0.0	-
RVPOLY	$\Omega\,m^2$	0.0	0.0	-
RSHG	$\Omega/\square$	0.0	0.0	-
DLSIL	m	0.0	-	-

The additional values and clipping values of the additional parameters for the (**p-channel**) model including self-heating (see section 15.6 on page 153) are listed in the table below.

Parameter	Units	Default	Clip low	Clip high
RTH	$^oC/W$	300.0	0.000	-
CTH	$J/^oC$	3.0×10^{-9}	0.000	-
ATH	-	0.0	-	-

The instance parameters are listed in the table below.

Parameter	Units	Default	Clip low	Clip high
L	m	2.000×10^{-6}	-	-
W	m	1.000×10^{-5}	-	-
MULT	-	1.000	0.000	-
NF	-	1.0	1.0	-
NGCON	-	1.0	1.0	2.0
XGW	m	$1.0\text{x}10^{-7}$	-	-

Remark: The parameters *L, W*, and *DTA* are used to calculate the electrical parameters of the actual transistor, as specified in the section on parameter preprocessing.

Parameters for Binning Geometrical Scaling

These parameters correspond to the geometrical model (MN, MP, MOS 11021), for binning geometrical scaling of the model. Note that for each bin (W_{min},W_{max},L_{min},L_{max}), there is a separate parameter set, which is valid for (W,L) values with $W_{min} \leq W \leq W_{max}$ and $L_{min} \leq L \leq L_{max}$.

Symbol	Progr. Name	Units	Description
	LEVEL	-	Must be 11021
ΔL_{PS}	LVAR	m	Difference between the actual and the programmed poly-silicon gate length
$\Delta L_{\mathrm{overlap}}$	LAP	m	Effective channel length reduction per side due to the lateral diffusion of the source/drain dopant ions
ΔW_{OD}	WVAR	m	Difference between the actual and the programmed field-oxide opening
$\Delta W_{\mathrm{narrow}}$	WOT	m	Effective reduction of the channel width per side due to the lateral diffusion of the channel-stop dopant ions
T_R	TR	°C	Reference temperature
V_{FB}	VFB	V	Flat-band voltage for all the transistors in the bin at the reference temperature
$P_{0;k_0}$	POKO	$\mathrm{V}^{1/2}$	Coefficient for the geometry independent part of k_0
$P_{L;k_0}$	PLKO	$\mathrm{V}^{1/2}$	Coefficient for the length dependence of k_0
$P_{W;k_0}$	PWKO	$\mathrm{V}^{1/2}$	Coefficient for the width dependence of k_0
$P_{LW;k_0}$	PLWKO	$\mathrm{V}^{1/2}$	Coefficient for the length times width dependence of k_0
$1/k_P$	KPINV	$\mathrm{V}^{-1/2}$	Inverse of the body-effect factor of the poly-silicon gate

Symbol	Progr. Name	Units	Description
$P_{0;\phi_B}$	POPHIB	V	Coefficient for the geometry independent part of ϕ_B
$P_{L;\phi_B}$	PLPHIB	V	Coefficient for the length dependence of ϕ_B
$P_{W;\phi_B}$	PWPHIB	V	Coefficient for the width dependence of ϕ_B
$P_{LW;\phi_B}$	PLWPHIB	V	Coefficient for the length times width dependence of ϕ_B
$P_{0;\beta}$	POBET	AV^{-2}	Coefficient for the geometry independent part of β
$P_{L;\beta}$	PLBET	AV^{-2}	Coefficient for the length dependence of β
$P_{W;\beta}$	PWBET	AV^{-2}	Coefficient for the width dependence of β
$P_{LW;\beta}$	PLWBET	AV^{-2}	Coefficient for the width over length dependence of β
$P_{0;\theta_{sr}}$	POTHESR	V^{-1}	Coefficient for the geometry independent part of θ_{sr}
$P_{L;\theta_{sr}}$	PLTHESR	V^{-1}	Coefficient for the length dependence of θ_{sr}
$P_{W;\theta_{sr}}$	PWTHESR	V^{-1}	Coefficient for the width dependence of θ_{sr}
$P_{LW;\theta_{sr}}$	PLWTHESR	V^{-1}	Coefficient for the length times width dependence of θ_{sr}
$P_{0;\theta_{ph}}$	POTHEPH	V^{-1}	Coefficient for the geometry independent part of θ_{ph}
$P_{L;\theta_{ph}}$	PLTHEPH	V^{-1}	Coefficient for the length dependence of θ_{ph}

Symbol	Progr. Name	Units	Description
$P_{W;\theta_{ph}}$	PWTHEPH	V^{-1}	Coefficient for the width dependence of θ_{ph}
$P_{LW;\theta_{ph}}$	PLWTHEPH	V^{-1}	Coefficient for the length times width dependence of θ_{ph}
$P_{0;\eta_{mob}}$	POETAMOB	-	Coefficient for the geometry independent part of η_{mob}
$P_{L;\eta_{mob}}$	PLETAMOB	-	Coefficient for the length dependence of η_{mob}
$P_{W;\eta_{mob}}$	PWETAMOB	-	Coefficient for the width dependence of η_{mob}
$P_{LW;\eta_{mob}}$	PLWETAMOB	-	Coefficient for the length times width dependence of η_{mob}
$P_{0;C_s}$	POCS	-	Coefficient for the geometry independent part of C_s
$P_{L;C_s}$	PLCS	-	Coefficient for the length dependence of C_s
$P_{W;C_s}$	PWCS	-	Coefficient for the width dependence of C_s
$P_{LW;C_s}$	PLWCS	-	Coefficient for the length times width dependence of C_s
$P_{0;\theta_R}$	POTHER	V^{-1}	Coefficient for the geometry independent part of θ_R
$P_{L;\theta_R}$	PLTHER	V^{-1}	Coefficient for the length dependence of θ_R
$P_{W;\theta_R}$	PWTHER	V^{-1}	Coefficient for the width dependence of θ_R
$P_{LW;\theta_R}$	PLWTHER	V^{-1}	Coefficient for the length times width dependence of θ_R

Symbol	Progr. Name	Units	Description
θ_{R1}	THER1	V	Numerator of the gate voltage dependent part of series resistance for all the transistors in the bin
θ_{R2}	THER2	V	Denominator of the gate voltage dependent part of series resistance for all the transistors in the bin
$P_{0;\theta_{sat}}$	POTHESAT	V^{-1}	Coefficient for the geometry independent part of θ_{sat}
$P_{L;\theta_{sat}}$	PLTHESAT	V^{-1}	Coefficient for the length dependence of θ_{sat}
$P_{W;\theta_{sat}}$	PWTHESAT	V^{-1}	Coefficient for the width dependence of θ_{sat}
$P_{LW;\theta_{sat}}$	PLWTHESAT	V^{-1}	Coefficient for the length times width dependence of θ_{sat}
$P_{0;\theta_{Th}}$	POTHETH	V^{-3}	Coefficient for the geometry independent part of θ_{Th}
$P_{L;\theta_{Th}}$	PLTHETH	V^{-3}	Coefficient for the length dependence of θ_{Th}
$P_{W;\theta_{Th}}$	PWTHETH	V^{-3}	Coefficient for the width dependence of θ_{Th}
$P_{LW;\theta_{Th}}$	PLWTHETH	V^{-3}	Coefficient for the length times width dependence of θ_{Th}
$P_{0;\sigma_{dibl}}$	POSDIBL	$V^{-1/2}$	Coefficient for the geometry independent part of σ_{dibl}
$P_{L;\sigma_{dibl}}$	PLSDIBL	$V^{-1/2}$	Coefficient for the length dependence of σ_{dibl}
$P_{W;\sigma_{dibl}}$	PWSDIBL	$V^{-1/2}$	Coefficient for the width dependence of σ_{dibl}
$P_{LW;\sigma_{dibl}}$	PLWSDIBL	$V^{-1/2}$	Coefficient for the length times width dependence of σ_{dibl}

Symbol	Progr. Name	Units	Description
$P_{0;m_0}$	POMO	-	Coefficient for the geometry independent part of m_0
$P_{L;m_0}$	PLMO	-	Coefficient for the length dependence of m_0
$P_{W;m_0}$	PWMO	-	Coefficient for the width dependence of m_0
$P_{LW;m_0}$	PLWMO	-	Coefficient for the length times width dependence of m_0
$P_{0;\sigma_{sf}}$	POSSF	$V^{-1/2}$	Coefficient for the geometry independent part of σ_{sf}
$P_{L;\sigma_{sf}}$	PLSSF	$V^{-1/2}$	Coefficient for the length dependence of σ_{sf}
$P_{W;\sigma_{sf}}$	PWSSF	$V^{-1/2}$	Coefficient for the width dependence of σ_{sf}
$P_{LW;\sigma_{sf}}$	PLWSSF	$V^{-1/2}$	Coefficient for the length times width dependence of σ_{sf}
$P_{0;\alpha}$	POALP	-	Coefficient for the geometry independent part of α
$P_{L;\alpha}$	PLALP	-	Coefficient for the length dependence of α
$P_{W;\alpha}$	PWALP	-	Coefficient for the width dependence of α
$P_{LW;\alpha}$	PLWALP	-	Coefficient for the length times width dependence of α
V_P	VP	V	Characteristic voltage of the channel length modulation
$P_{0;m}$	POMEXP	-	Coefficient for the geometry independent part of $1/m$
$P_{L;m}$	PLMEXP	-	Coefficient for the length dependence of $1/m$

Symbol	Progr. Name	Units	Description
$P_{W;m}$	PWMEXP	-	Coefficient for the width dependence of $1/m$
$P_{LW;m}$	PLWMEXP	-	Coefficient for the length times width dependence of $1/m$
$P_{0;a_1}$	POA1	-	Coefficient for the geometry independent part of a_1
$P_{L;a_1}$	PLA1	-	Coefficient for the length dependence of a_1
$P_{W;a_1}$	PWA1	-	Coefficient for the width dependence of a_1
$P_{LW;a_1}$	PLWA1	-	Coefficient for the length times width dependence of a_1
$P_{0;a_2}$	POA2	V	Coefficient for the geometry independent part of a_2
$P_{L;a_2}$	PLA2	V	Coefficient for the length dependence of a_2
$P_{W;a_2}$	PWA2	V	Coefficient for the width dependence of a_2
$P_{LW;a_2}$	PLWA2	V	Coefficient for the length times width dependence of a_2
$P_{0;a_3}$	POA3	-	Coefficient for the geometry independent part of a_3
$P_{L;a_3}$	PLA3	-	Coefficient for the length dependence of a_3
$P_{W;a_3}$	PWA3	-	Coefficient for the width dependence of a_3
$P_{LW;a_3}$	PLWA3	-	Coefficient for the length times width dependence of a_3

Symbol	Progr. Name	Units	Description
$P_{0;I_{GINV}}$	POIGINV	AV^{-2}	Coefficient for the geometry independent part of I_{GINV}
$P_{L;I_{GINV}}$	PLIGINV	AV^{-2}	Coefficient for the length dependence of I_{GINV}
$P_{W;I_{GINV}}$	PWIGINV	AV^{-2}	Coefficient for the width dependence of I_{GINV}
$P_{LW;I_{GINV}}$	PLWIGINV	AV^{-2}	Coefficient for the length times width dependence of I_{GINV}
$P_{0;B_{inv}}$	POBINV	V	Coefficient for the geometry independent part of B_{inv}
$P_{L;B_{inv}}$	PLBINV	V	Coefficient for the length dependence of B_{inv}
$P_{W;B_{inv}}$	PWBINV	V	Coefficient for the width dependence of B_{inv}
$P_{LW;B_{inv}}$	PLWBINV	V	Coefficient for the length times width dependence of B_{inv}
$P_{0;I_{GACC}}$	POIGACC	AV^{-2}	Coefficient for the geometry independent part of I_{GACC}
$P_{L;I_{GACC}}$	PLIGACC	AV^{-2}	Coefficient for the length dependence of I_{GACC}
$P_{W;I_{GACC}}$	PWIGACC	AV^{-2}	Coefficient for the width dependence of I_{GACC}
$P_{LW;I_{GACC}}$	PLWIGACC	AV^{-2}	Coefficient for the length times width dependence of I_{GACC}
$P_{0;B_{acc}}$	POBACC	V	Coefficient for the geometry independent part of B_{acc}
$P_{L;B_{acc}}$	PLBACC	V	Coefficient for the length dependence of B_{acc}

Symbol	Progr. Name	Units	Description
$P_{W;B_{acc}}$	PWBACC	V	Coefficient for the width dependence of B_{acc}
$P_{LW;B_{acc}}$	PLWBACC	V	Coefficient for the length times width dependence of B_{acc}
V_{FBov}	VFBOV	V	Flat-band voltage for the source/drain overlap extensions
k_{ov}	KOV	$V^{1/2}$	Bodu-effect factor for the source/drain overlap extensions
$P_{0;I_{GOV}}$	POIGOV	AV^{-2}	Coefficient for the geometry independent part of I_{GOV}
$P_{L;I_{GOV}}$	PLIGOV	AV^{-2}	Coefficient for the length dependence of I_{GOV}
$P_{W;I_{GOV}}$	PWIGOV	AV^{-2}	Coefficient for the width dependence of I_{GOV}
$P_{LW;I_{GOV}}$	PLWIGOV	AV^{-2}	Coefficient for the length times width dependence of I_{GOV}
$P_{0;A_{GIDL}}$	POAGIDL	AV^{-3}	Coefficient for the geometry independent part of A_{GIDL}
$P_{L;A_{GIDL}}$	PLAGIDL	AV^{-3}	Coefficient for the length dependence of A_{GIDL}
$P_{W;A_{GIDL}}$	PWAGIDL	AV^{-3}	Coefficient for the width dependence of A_{GIDL}
$P_{LW;A_{GIDL}}$	PLWAGIDL	AV^{-3}	Coefficient for the width over length dependence of A_{GIDL}
$P_{0;B_{GIDL}}$	POBGIDL	V	Coefficient for the geometry independent part of B_{GIDL}
$P_{L;B_{GIDL}}$	PLBGIDL	V	Coefficient for the length dependence of B_{GIDL}

Symbol	Progr. Name	Units	Description
$P_{W;B_{GIDL}}$	PWBGIDL	V	Coefficient for the width dependence of B_{GIDL}
$P_{LW;B_{GIDL}}$	PLWBGIDL	V	Coefficient for the length times width dependence of B_{GIDL}
$P_{0;C_{GIDL}}$	POCGIDL	-	Coefficient for the geometry independent part of C_{GIDL}
$P_{L;C_{GIDL}}$	PLCGIDL	-	Coefficient for the length dependence of C_{GIDL}
$P_{W;C_{GIDL}}$	PWCGIDL	-	Coefficient for the width dependence of C_{GIDL}
$P_{LW;C_{GIDL}}$	PLWCGIDL	-	Coefficient for the length times width dependence of C_{GIDL}
t_{ox}	TOX	m	Thickness of the gate oxide layer
$P_{0;C_{ox}}$	POCOX	F	Coefficient for the geometry independent part of C_{ox}
$P_{L;C_{ox}}$	PLCOX	F	Coefficient for the length dependence of C_{ox}
$P_{W;C_{ox}}$	PWCOX	F	Coefficient for the width dependence of C_{ox}
$P_{LW;C_{ox}}$	PLWCOX	F	Coefficient for the length times width dependence of C_{ox}
$P_{0;C_{GDO}}$	POCGDO	F	Coefficient for the geometry independent part of C_{GDO}
$P_{L;C_{GDO}}$	PLCGDO	F	Coefficient for the length dependence of C_{GDO}
$P_{W;C_{GDO}}$	PWCGDO	F	Coefficient for the width dependence of C_{GDO}
$P_{LW;C_{GDO}}$	PLWCGDO	F	Coefficient for the width over length dependence of C_{GDO}

Symbol	Progr. Name	Units	Description
$P_{0;C_{GSO}}$	POCGSO	F	Coefficient for the geometry independent part of C_{GSO}
$P_{L;C_{GSO}}$	PLCGSO	F	Coefficient for the length dependence of C_{GSO}
$P_{W;C_{GSO}}$	PWCGSO	F	Coefficient for the width dependence of C_{GSO}
$P_{LW;C_{GSO}}$	PLWCGSO	F	Coefficient for the width over length dependence of C_{GSO}
-	GATENOISE		Flag for in/exclusion of induced gate thermal noise
N_T	NT	J	Coefficient of the thermal noise at the reference temperature
$P_{0;N_{FA}}$	PONFA	$V^{-1}m^{-4}$	Coefficient for the geometry independent part of N_{FA}
$P_{L;N_{FA}}$	PLNFA	$V^{-1}m^{-4}$	Coefficient for the length dependence of N_{FA}
$P_{W;N_{FA}}$	PWNFA	$V^{-1}m^{-4}$	Coefficient for the width dependence of N_{FA}
$P_{LW;N_{FA}}$	PLWNFA	$V^{-1}m^{-4}$	Coefficient for the length times width dependence of N_{FA}
$P_{0;N_{FB}}$	PONFB	$V^{-1}m^{-2}$	Coefficient for the geometry independent part of N_{FB}
$P_{L;N_{FB}}$	PLNFB	$V^{-1}m^{-2}$	Coefficient for the length dependence of N_{FB}
$P_{W;N_{FB}}$	PWNFB	$V^{-1}m^{-2}$	Coefficient for the width dependence of N_{FB}
$P_{LW;N_{FB}}$	PLWNFB	$V^{-1}m^{-2}$	Coefficient for the length times width dependence of N_{FB}

Symbol	Progr. Name	Units	Description
$P_{0;N_{FC}}$	PONFC	V^{-1}	Coefficient for the geometry independent part of N_{FC}
$P_{L;N_{FC}}$	PLNFC	V^{-1}	Coefficient for the length dependence of N_{FC}
$P_{W;N_{FC}}$	PWNFC	V^{-1}	Coefficient for the width dependence of N_{FC}
$P_{LW;N_{FC}}$	PLWNFC	V^{-1}	Coefficient for the length times width dependence of N_{FC}
$P_{0;T;V_{FB}}$	POTVFB	VK^{-1}	Coefficient for the geometry independent part of $S_{T;V_{FB}}$
$P_{L;T;V_{FB}}$	PLTVFB	VK^{-1}	Coefficient for the length dependence of $S_{T;V_{FB}}$
$P_{W;T;V_{FB}}$	PWTVFB	VK^{-1}	Coefficient for the width dependence of $S_{T;V_{FB}}$
$P_{LW;T;V_{FB}}$	PLWTVFB	VK^{-1}	Coefficient for the length times width dependence of $S_{T;V_{FB}}$
$P_{0;T;\phi_B}$	POTPHIB	VK^{-1}	Coefficient for the geometry independent part of $S_{T;\phi_B}$
$P_{L;T;\phi_B}$	PLTPHIB	VK^{-1}	Coefficient for the length dependence of $S_{T;\phi_B}$
$P_{W;T;\phi_B}$	PWTPHIB	VK^{-1}	Coefficient for the width dependence of $S_{T;\phi_B}$
$P_{LW;T;\phi_B}$	PLWTPHIB	VK^{-1}	Coefficient for the length times width dependence of $S_{T;\phi_B}$
$P_{0;T;\eta_\beta}$	POTETABET	-	Coefficient for the geometry independent part of η_β
$P_{L;T;\eta_\beta}$	PLTETABET	-	Coefficient for the length dependence of η_β

Symbol	Progr. Name	Units	Description
$P_{W;T;\eta_\beta}$	PWTETABET	-	Coefficient for the width dependence of η_β
$P_{LW;T;\eta_\beta}$	PLWTETABET	-	Coefficient for the length times width dependence of η_β
$P_{0;T;\eta_{sr}}$	POTETASR	-	Coefficient for the geometry independent part of η_{sr}
$P_{L;T;\eta_{sr}}$	PLTETASR	-	Coefficient for the length dependence of η_{sr}
$P_{W;T;\eta_{sr}}$	PWTETASR	-	Coefficient for the width dependence of η_{sr}
$P_{LW;T;\eta_{sr}}$	PLWETASR	-	Coefficient for the length times width dependence of η_{sr}
$P_{0;T;\eta_{ph}}$	POTETAPH	-	Coefficient for the geometry independent part of η_{ph}
$P_{L;T;\eta_{ph}}$	PLTETAPH	-	Coefficient for the length dependence of η_{ph}
$P_{W;T;\eta_{ph}}$	PWTETAPH	-	Coefficient for the width dependence of η_{ph}
$P_{LW;T;\eta_{ph}}$	PLWETAPH	-	Coefficient for the length times width dependence of η_{ph}
$P_{0;T;\eta_{mob}}$	POTETAMOB	K^{-1}	Coefficient for the geometry independent part of $S_{T;\eta_{mob}}$
$P_{L;T;\eta_{mob}}$	PLTETAMOB	K^{-1}	Coefficient for the length dependence of $S_{T;\eta_{mob}}$
$P_{W;T;\eta_{mob}}$	PWTETAMOB	K^{-1}	Coefficient for the width dependence of $S_{T;\eta_{mob}}$
$P_{LW;T;\eta_{mob}}$	PLWTETAMOB	K^{-1}	Coefficient for the length times width dependence of $S_{T;\eta_{mob}}$

Symbol	Progr. Name	Units	Description
υ	NU	-	Exponent of the field dependence of the mobility model at the reference temperature
$P_{0;T;\upsilon_{exp}}$	POTNUEXP	-	Coefficient for the geometry independent part of υ_{exp}
$P_{L;T;\upsilon_{exp}}$	PLTNUEXP	-	Coefficient for the length dependence of υ_{exp}
$P_{W;T;\upsilon_{exp}}$	PWTNUEXP	-	Coefficient for the width dependence of υ_{exp}
$P_{LW;T;\upsilon_{exp}}$	PLWTNUEXP	-	Coefficient for the length times width dependence of υ_{exp}
$P_{0;T;\eta_{C_s}}$	POTETACS	-	Coefficient for the geometry independent part of η_{C_s}
$P_{L;T;\eta_{C_s}}$	PLTETACS	-	Coefficient for the length dependence of η_{C_s}
$P_{W;T;\eta_{C_s}}$	PWTETACS	-	Coefficient for the width dependence of η_{C_s}
$P_{LW;T;\eta_{C_s}}$	PLWTETACS	-	Coefficient for the length times width dependence of η_{C_s}
$P_{0;T;\eta_R}$	POTETAR	-	Coefficient for the geometry independent part of η_R
$P_{L;T;\eta_R}$	PLTETAR	-	Coefficient for the length dependence of η_R
$P_{W;T;\eta_R}$	PWTETAR	-	Coefficient for the width dependence of η_R
$P_{LW;T;\eta_R}$	PLWTETAR	-	Coefficient for the length times width dependence of η_R
$P_{0;T;\eta_{sat}}$	POTETASAT	-	Coefficient for the geometry independent part of η_{sat}

Symbol	Progr. Name	Units	Description
$P_{L;T;\eta_{sat}}$	PLTETASAT	-	Coefficient for the length dependence of η_{sat}
$P_{W;T;\eta_{sat}}$	PWTETASAT	-	Coefficient for the width dependence of η_{sat}
$P_{LW;T;\eta_{sat}}$	PLWTETASAT	-	Coefficient for the length times width dependence of η_{sat}
$P_{0;T;a_1}$	POTA1	K^{-1}	Coefficient for the geometry independent part of $S_{T;a_1}$
$P_{L;T;a_1}$	PLTA1	K^{-1}	Coefficient for the length dependence of $S_{T;a_1}$
$P_{W;T;a_1}$	PWTA1	K^{-1}	Coefficient for the width dependence of $S_{T;a_1}$
$P_{LW;T;a_1}$	PLWTA1	K^{-1}	Coefficient for the length times width dependence of $S_{T;a_1}$
$P_{0;T;B_{GIDL}}$	POTBGIDL	VK^{-1}	Coefficient for the geometry independent part of $S_{T;B_{GIDL}}$
$P_{L;T;B_{GIDL}}$	PLTBGIDL	VK^{-1}	Coefficient for the length dependence of $S_{T;B_{GIDL}}$
$P_{W;T;B_{GIDL}}$	PWTBGIDL	VK^{-1}	Coefficient for the width dependence of $S_{T;B_{GIDL}}$
$P_{LW;T;B_{GIDL}}$	PLWTBGIDL	VK^{-1}	Coefficient for the length times width dependence of $S_{T;B_{GIDL}}$
ΔT_A	DTA	K	Temperature offset of the device with respect to T_A
l_{min}	LMIN	m	Minimum length of the bin
l_{max}	LMAX	m	Maximum length of the bin
w_{min}	WMIN	m	Minimum width of the bin
w_{max}	WMAX	m	Maximum width of the bin

Symbol	Progr. Name	Units	Description
RG0	RGO	Ω	Gate Resistance
RINT	RINT	$\Omega\,m^2$	Contact resistance between silicide and poly
RVPOLY	RVPOLY	$\Omega\,m^2$	Vertical poly resistance
RSHG	RSHG	Ω/□	Gate electrode diffusion sheet resistance
DLSIL	DLSIL	m	Silicide extension over the physical gate length

The additional parameters for the model including self-heating (see section 15.6 on page 153) are listed in the table below.

Symbol	Progr. Name	Units	Description
R_{TH}	RTH	$^oC/W$	Thermal resistance
C_{TH}	CTH	$J/^oC$	Thermal capacitance
A_{TH}	ATH	-	Temperature coefficient of the thermal resistance

The instance parameters are listed in the table below.

Symbol	Progr. Name	Units	Description
L	L	m	Drawn channel length in the lay-out of the actual transistor
W	W	m	Drawn channel width in the lay-out of the actual transistor
NMULT	MULT	-	Number of devices in parallel
NF	NF	-	Number of fingers
NGCON	NGCON	-	Number of gate contacts
XGW	XGW	m	Distance from the gate contact to the channel edge

Remark: The parameters *L, W*, and *DTA* are used to calculate the electrical parameters of the actual transistor, as specified in the section on parameter preprocessing.

Default and clipping values (binning geometrical model)

The default values and clipping values for the parameters of the binning geometrical scaling rules of MOS model, level 1102 (n-channel) are listed below.

Parameter	Units	Default	Clip low	Clip high
LEVEL	-	11021	-	-
LVAR	m	0.000	-	-
LAP	m	4.0×10^{-8}	-	-
WVAR	m	0.000	-	-
WOT	m	0.000	-	-
TR	°C	21.0	-273.0	-
VFB	V	-1.050	-	-
POKO	$V^{1/2}$	0.500	-	-
PLKO	$V^{1/2}$	0.000	-	-
PWKO	$V^{1/2}$	0.000	-	-
PLWKO	$V^{1/2}$	0.000	-	-
KPINV	$V^{-1/2}$	0.000	-	-
POPHIB	V	0.950	-	-
PLPHIB	V	0.000	-	-
PWPHIB	V	0.000	-	-
PLWPHIB	V	0.000	-	-
POBET	AV^{-2}	1.922×10^{-3}	-	-
PLBET	AV^{-2}	0.000	-	-
PWBET	AV^{-2}	0.000	-	-
PLWBET	AV^{-2}	0.000	-	-
POTHESR	V^{-1}	3.562×10^{-1}	-	-
PLTHESR	V^{-1}	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
PWTHESR	V^{-1}	0.000	-	-
PLWTHESR	V^{-1}	0.000	-	-
POTHEPH	V^{-1}	1.290×10^{-2}	-	-
PLTHEPH	V^{-1}	0.000	-	-
PWTHEPH	V^{-1}	0.000	-	-
PLWTHEPH	V^{-1}	0.000	-	-
POETAMOB	-	1.400	-	-
PLETAMOB	-	0.000	-	-
PWETAMOB	-	0.000	-	-
PLWETAMOB	-	0.000	-	-
POCS	-	0.00	-	-
PLCS	-	0.000	-	-
PWCS	-	0.000	-	-
PLWCS	-	0.000	-	-
POTHER	V^{-1}	8.120×10^{-2}	-	-
PLTHER	V^{-1}	0.000	-	-
PWTHER	V^{-1}	0.000	-	-
PLWTHER	V^{-1}	0.000	-	-
THER1	V	0.000	-	-
THER2	V	1.000	-	-
POTHESAT	V^{-1}	2.513×10^{-1}	-	-
PLTHESAT	V^{-1}	0.000	-	-
PWTHESAT	V^{-1}	0.000	-	-
PLWTHESAT	V^{-1}	0.000	-	-
POTHETH	V^{-3}	1.0×10^{-5}	-	-

Parameter	Units	Default	Clip low	Clip high
PLTHETH	V^{-3}	0.000	-	-
PWTHETH	V^{-3}	0.000	-	-
PLWTHETH	V^{-3}	0.000	-	-
POSDIBL	$V^{-1/2}$	8.530×10^{-4}	-	-
PLSDIBL	$V^{-1/2}$	0.000	-	-
PWSDIBL	$V^{-1/2}$	0.000	-	-
PLWSDIBL	$V^{-1/2}$	0.000	-	-
POMO	-	0.000	-	-
PLMO	-	0.000	-	-
PWMO	-	0.000	-	-
PLWMO	-	0.000	-	-
POSSF	$V^{-1/2}$	1.200×10^{-2}	-	-
PLSSF	$V^{-1/2}$	0.000	-	-
PWSSF	$V^{-1/2}$	0.000	-	-
PLWSSF	$V^{-1/2}$	0.000	-	-
POALP	-	2.500×10^{-2}	-	-
PLALP	-	0.000	-	-
PWALP	-	0.000	-	-
PLWALP	-	0.000	-	-
VP	V	5.000×10^{-2}	-	-
POMEXP	-	0.200	-	-
PLMEXP	-	0.000	-	-
PWMEXP	-	0.000	-	-
PLWMEXP	-	0.000	-	-
POA1	-	6.022	-	-

Parameter	Units	Default	Clip low	Clip high
PLA1	-	0.000	-	-
PWA1	-	0.000	-	-
PLWA1	-	0.000	-	-
POA2	V	3.802×10^{1}	-	-
PLA2	V	0.000	-	-
PWA2	V	0.000	-	-
PLWA2	V	0.000	-	-
POA3	-	6.407×10^{-1}	-	-
PLA3	-	0.000	-	-
PWA3	-	0.000	-	-
PLWA3	-	0.000	-	-
POIGINV	AV^{-2}	0.000	-	-
PLIGINV	AV^{-2}	0.000	-	-
PWIGINV	AV^{-2}	0.000	-	-
PLWIGINV	AV^{-2}	0.000	-	-
POBINV	V	4.800×10^{1}	-	-
PLBINV	V	0.000	-	-
PWBINV	V	0.000	-	-
PLWBINV	V	0.000	-	-
POIGACC	AV^{-2}	0.000	-	-
PLIGACC	AV^{-2}	0.000	-	-
PWIGACC	AV^{-2}	0.000	-	-
PLWIGACC	AV^{-2}	0.000	-	-
POBACC	V	4.800×10^{1}	-	-
PLBACC	V	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
PWBACC	V	0.000	-	-
PLWBACC	V	0.000	-	-
VFBOV	V	0.000	-	-
KOV	$V^{1/2}$	2.500	1.0×10^{-12}	-
POIGOV	AV^{-2}	0.000	-	-
PLIGOV	AV^{-2}	0.000	-	-
PWIGOV	AV^{-2}	0.000	-	-
PLWIGOV	AV^{-2}	0.000	-	-
POAGIDL	AV^{-3}	0.000	-	-
PLAGIDL	AV^{-3}	0.000	-	-
PWAGIDL	AV^{-3}	0.000	-	-
PLWAGIDL	AV^{-3}	0.000	-	-
POBGIDL	V	$4.100 \times 10^{+1}$	-	-
PLBGIDL	V	0.000	-	-
PWBGIDL	V	0.000	-	-
PLWBGIDL	V	0.000	-	-
POCGIDL	-	0.000	-	-
PLCGIDL	-	0.000	-	-
PWCGIDL	-	0.000	-	-
PLWCCGIDL	-	0.000	-	-
TOX	m	3.200×10^{-9}	1.0×10^{-12}	-
POCOX	F	2.980×10^{-14}	-	-
PLCOX	F	0.000	-	-
PWCOX	F	0.000	-	-
PLWCOX	F	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
POCGDO	F	6.392×10^{-15}	-	-
PLCGDO	F	0.000	-	-
PWCGDO	F	0.000	-	-
PLWCGDO	F	0.000	-	-
POCGSO	F	6.392×10^{-15}	-	-
PLCGSO	F	0.000	-	-
PWCGSO	F	0.000	-	-
PLWCGSO	F	0.000	-	-
GATENOISE	-	0.000	0.000	1.000
NT	J	1.624×10^{-20}	0.000	-
PONFA	$V^{-1}m^{-4}$	8.323×10^{22}	-	-
PLNFA	$V^{-1}m^{-4}$	0.000	-	-
PWNFA	$V^{-1}m^{-4}$	0.000	-	-
PLWNFA	$V^{-1}m^{-4}$	0.000	-	-
PONFB	$V^{-1}m^{-2}$	2.514×10^{7}	-	-
PLNFB	$V^{-1}m^{-2}$	0.000	-	-
PWNFB	$V^{-1}m^{-2}$	0.000	-	-
PLWNFB	$V^{-1}m^{-2}$	0.000	-	-
PONFC	V^{-1}	0.000	-	-
PLNFC	V^{-1}	0.000	-	-
PWNFC	V^{-1}	0.000	-	-
PLWNFC	V^{-1}	0.000	-	-
POTVFB	VK^{-1}	5.000×10^{-4}	-	-
PLTVFB	VK^{-1}	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
PWTVFB	VK^{-1}	0.000	-	-
PLWTVFB	VK^{-1}	0.000	-	-
POTPHIB	VK^{-1}	-8.500×10^{-4}	-	-
PLTPHIB	VK^{-1}	0.000	-	-
PWTPHIB	VK^{-1}	0.000	-	-
PLWTPHIB	VK^{-1}	0.000	-	-
POTETABET	-	1.300	-	-
PLTETABET	-	0.000	-	-
PWTETABET	-	0.000	-	-
PLWTETABET	-	0.000	-	-
POTETASR	-	0.650	-	-
PLTETASR	-	0.000	-	-
PWTETASR	-	0.000	-	-
PLWETASR	-	0.000	-	-
POTETAPH	-	1.350	-	-
PLTETAPH	-	0.000	-	-
PWTETAPH	-	0.000	-	-
PLWETAPH	-	0.000	-	-
POTETAMOB	K^{-1}	0.000	-	-
PLTETAMOB	K^{-1}	0.000	-	-
PWTETAMOB	K^{-1}	0.000	-	-
PLWTETAMOB	K^{-1}	0.000	-	-
NU	-	2.000	1.000	100
POTNUEXP	-	5.250	-	-
PLTNUEXP	-	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
PWTNUEXP	-	0.000	-	-
PLWTNUEXP	-	0.000	-	-
POTETACS	-	0.000	-	-
PLTETACS	-	0.000	-	-
PWTETACS	-	0.000	-	-
PLWTETACS	-	0.000	-	-
POTETAR	-	0.950	-	-
PLTETAR	-	0.000	-	-
PWTETAR	-	0.000	-	-
PLWTETAR	-	0.000	-	-
POTETASAT	-	1.040	-	-
PLTETASAT	-	0.000	-	-
PWTETASAT	-	0.000	-	-
PLWTETASAT	-	0.000	-	-
POTA1	K^{-1}	0.000	-	-
PLTA1	K^{-1}	0.000	-	-
PWTA1	K^{-1}	0.000	-	-
PLWTA1	K^{-1}	0.000	-	-
POTBGIDL	VK^{-1}	-3.638×10^{-4}	-	-
PLTBGIDL	VK^{-1}	0.000	-	-
PWTBGIDL	VK^{-1}	0.000	-	-
PLWTBGIDL	VK^{-1}	0.000	-	-
DTA	K	0.000	-	-
LMIN	m	0.000	-	-
LMAX	m	1.000	-	-
WMIN	m	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
WMAX	m	1.000	-	-
RGO	Ω	0.0	-	-
RINT	$\Omega\,m^2$	0.0	0.0	-
RVPOLY	$\Omega\,m^2$	0.0	0.0	-
RSHG	Ω/□	0.0	0.0	-
DLSIL	m	0.0	-	-

The additional values and clipping values of the additional parameters for the (**n-channel**) model including self-heating (see section 15.6 on page 153) are listed in the table below.

Parameter	Units	Default	Clip low	Clip high
RTH	$^oC/W$	300.0	0.000	-
CTH	$J/^oC$	3.0×10^{-9}	0.000	-
ATH	-	0.0	-	-

The instance parameters are listed in the table below.

Parameter	Units	Default	Clip low	Clip high
L	m	2.000×10^{-6}	-	-
W	m	1.000×10^{-5}	-	-
MULT	-	1.000	0.000	-
NF	-	1.0	1.0	-
NGCON	-	1.0	1.0	2.0
XGW	m	$1.0\text{x}10^{-7}$	-	-

Remark: The parameters *L, W*, and *DTA* are used to calculate the electrical parameters of the actual transistor, as specified in the section on parameter preprocessing.

The default values and clipping values for the parameters of the binning geometrical scaling rules of MOS model, level 1102 (p-channel) are listed below.

Parameter	Units	Default	Clip low	Clip high
LEVEL	-	11021	-	-
LVAR	m	0.000	-	-
LAP	m	4.0×10^{-8}	-	-
WVAR	m	0.000	-	-
WOT	m	0.000	-	-
TR	°C	21.0	-273.0	-
VFB	V	-1.050	-	-
POKO	$V^{1/2}$	0.500	-	-
PLKO	$V^{1/2}$	0.000	-	-
PWKO	$V^{1/2}$	0.000	-	-
PLWKO	$V^{1/2}$	0.000	-	-
KPINV	$V^{-1/2}$	0.000	-	-
POPHIB	V	0.950	-	-
PLPHIB	V	0.000	-	-
PWPHIB	V	0.000	-	-
PLWPHIB	V	0.000	-	-
POBET	AV^{-2}	3.814×10^{-4}	-	-
PLBET	AV^{-2}	0.000	-	-
PWBET	AV^{-2}	0.000	-	-
PLWBET	AV^{-2}	0.000	-	-
POTHESR	V^{-1}	7.300×10^{-1}	-	-
PLTHESR	V^{-1}	0.000	-	-
PWTHESR	V^{-1}	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
PLWTHESR	V^{-1}	0.000	-	-
POTHEPH	V^{-1}	1.000×10^{-3}	-	-
PLTHEPH	V^{-1}	0.000	-	-
PWTHEPH	V^{-1}	0.000	-	-
PLWTHEPH	V^{-1}	0.000	-	-
POETAMOB	-	3.000	-	-
PLETAMOB	-	0.000	-	-
PWETAMOB	-	0.000	-	-
PLWETAMOB	-	0.000	-	-
POCS	-	0.00	-	-
PLCS	-	0.000	-	-
PWCS	-	0.000	-	-
PLWCS	-	0.000	-	-
POTHER	V^{-1}	7.900×10^{-2}	-	-
PLTHER	V^{-1}	0.000	-	-
PWTHER	V^{-1}	0.000	-	-
PLWTHER	V^{-1}	0.000	-	-
THER1	V	0.000	-	-
THER2	V	1.000	-	-
POTHESAT	V^{-1}	1.728×10^{-1}	-	-
PLTHESAT	V^{-1}	0.000	-	-
PWTHESAT	V^{-1}	0.000	-	-
PLWTHESAT	V^{-1}	0.000	-	-
POTHETH	V^{-3}	0.000	-	-
PLTHETH	V^{-3}	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
PWTHETH	V^{-3}	0.000	-	-
PLWTHETH	V^{-3}	0.000	-	-
POSDIBL	$V^{-1/2}$	3.551×10^{-5}	-	-
PLSDIBL	$V^{-1/2}$	0.000	-	-
PWSDIBL	$V^{-1/2}$	0.000	-	-
PLWSDIBL	$V^{-1/2}$	0.000	-	-
POMO	-	0.000	-	-
PLMO	-	0.000	-	-
PWMO	-	0.000	-	-
PLWMO	-	0.000	-	-
POSSF	$V^{-1/2}$	1.000×10^{-2}	-	-
PLSSF	$V^{-1/2}$	0.000	-	-
PWSSF	$V^{-1/2}$	0.000	-	-
PLWSSF	$V^{-1/2}$	0.000	-	-
POALP	-	2.500×10^{-2}	-	-
PLALP	-	0.000	-	-
PWALP	-	0.000	-	-
PLWALP	-	0.000	-	-
VP	V	5.000×10^{-2}	-	-
POMEXP	-	0.200	-	-
PLMEXP	-	0.000	-	-
PWMEXP	-	0.000	-	-
PLWMEXP	-	0.000	-	-
POA1	-	6.858	-	-
PLA1	-	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
PWA1	-	0.000	-	-
PLWA1	-	0.000	-	-
POA2	V	5.732×10^{1}	-	-
PLA2	V	0.000	-	-
PWA2	V	0.000	-	-
PLWA2	V	0.000	-	-
POA3	-	4.254×10^{-1}	-	-
PLA3	-	0.000	-	-
PWA3	-	0.000	-	-
PLWA3	-	0.000	-	-
POIGINV	AV^{-2}	0.000	-	-
PLIGINV	AV^{-2}	0.000	-	-
PWIGINV	AV^{-2}	0.000	-	-
PLWIGINV	AV^{-2}	0.000	-	-
POBINV	V	87.50	-	-
PLBINV	V	0.000	-	-
PWBINV	V	0.000	-	-
PLWBINV	V	0.000	-	-
POIGACC	AV^{-2}	0.000	-	-
PLIGACC	AV^{-2}	0.000	-	-
PWIGACC	AV^{-2}	0.000	-	-
PLWIGACC	AV^{-2}	0.000	-	-
POBACC	V	48.00	-	-
PLBACC	V	0.000	-	-
PWBACC	V	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
PLWBACC	V	0.000	-	-
VFBOV	V	0.000	-	-
KOV	$V^{1/2}$	2.500	1e-12	-
POIGOV	AV^{-2}	0.000	-	-
PLIGOV	AV^{-2}	0.000	-	-
PWIGOV	AV^{-2}	0.000	-	-
PLWIGOV	AV^{-2}	0.000	-	-
POAGIDL	AV^{-3}	0.000	-	-
PLAGIDL	AV^{-3}	0.000	-	-
PWAGIDL	AV^{-3}	0.000	-	-
PLWAGIDL	AV^{-3}	0.000	-	-
POBGIDL	V	$4.100 \times 10^{+1}$	-	-
PLBGIDL	V	0.000	-	-
PWBGIDL	V	0.000	-	-
PLWBGIDL	V	0.000	-	-
POCGIDL	-	0.000	-	-
PLCGIDL	-	0.000	-	-
PWCGIDL	-	0.000	-	-
PLWCCGIDL	-	0.000	-	-
TOX	m	3.200×10^{-9}	1e-12	-
POCOX	F	2.717×10^{-14}	-	-
PLCOX	F	0.000	-	-
PWCOX	F	0.000	-	-
PLWCOX	F	0.000	-	-
POCGDO	F	6.358×10^{-15}	-	-

Parameter	Units	Default	Clip low	Clip high
PLCGDO	F	0.000	-	-
PWCGDO	F	0.000	-	-
PLWCGDO	F	0.000	-	-
POCGSO	F	6.358×10^{-15}	-	-
PLCGSO	F	0.000	-	-
PWCGSO	F	0.000	-	-
PLWCGSO	F	0.000	-	-
GATENOISE	-	0.000	0.000	1.000
NT	J	1.656×10^{-20}	0	-
PONFA	$V^{-1}m^{-4}$	1.900×10^{22}	-	-
PLNFA	$V^{-1}m^{-4}$	0.000	-	-
PWNFA	$V^{-1}m^{-4}$	0.000	-	-
PLWNFA	$V^{-1}m^{-4}$	0.000	-	-
PONFB	$V^{-1}m^{-2}$	5.043×10^{6}	-	-
PLNFB	$V^{-1}m^{-2}$	0.000	-	-
PWNFB	$V^{-1}m^{-2}$	0.000	-	-
PLWNFB	$V^{-1}m^{-2}$	0.000	-	-
PONFC	V^{-1}	3.627×10^{-10}	-	-
PLNFC	V^{-1}	0.000	-	-
PWNFC	V^{-1}	0.000	-	-
PLWNFC	V^{-1}	0.000	-	-
POTVFB	VK^{-1}	0.5×10^{-3}	-	-
PLTVFB	VK^{-1}	0.000	-	-
PWTVFB	VK^{-1}	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
PLWTVFB	VK^{-1}	0.000	-	-
POTPHIB	VK^{-1}	-8.5×10^{-4}	-	-
PLTPHIB	VK^{-1}	0.000	-	-
PWTPHIB	VK^{-1}	0.000	-	-
PLWTPHIB	VK^{-1}	0.000	-	-
POTETABET	-	0.500	-	-
PLTETABET	-	0.000	-	-
PWTETABET	-	0.000	-	-
PLWTETABET	-	0.000	-	-
POTETASR	-	0.500	-	-
PLTETASR	-	0.000	-	-
PWTETASR	-	0.000	-	-
PLWTETASR	-	0.000	-	-
POTETAPH	-	3.750	-	-
PLTETAPH	-	0.000	-	-
PWTETAPH	-	0.000	-	-
PLWTETAPH	-	0.000	-	-
POTETAMOB	K^{-1}	0.000	-	-
PLTETAMOB	K^{-1}	0.000	-	-
PWTETAMOB	K^{-1}	0.000	-	-
PLWTETAMOB	K^{-1}	0.000	-	-
NU	-	2.000	1	100
POTNUEXP	-	3.230	-	-
PLTNUEXP	-	0.000	-	-
PWTNUEXP	-	0.000	-	-
PLWTNUEXP	-	0.000	-	-

Parameter	Units	Default	Clip low	Clip high
POTETACS	-	0.000	-	-
PLTETACS	-	0.000	-	-
PWTETACS	-	0.000	-	-
PLWTETACS	-	0.000	-	-
POTETAR	-	0.400	-	-
PLTETAR	-	0.000	-	-
PWTETAR	-	0.000	-	-
PLWTETAR	-	0.000	-	-
POTETASAT	-	0.860	-	-
PLTETASAT	-	0.000	-	-
PWTETASAT	-	0.000	-	-
PLWTETASAT	-	0.000	-	-
POTA1	K^{-1}	0.000	-	-
PLTA1	K^{-1}	0.000	-	-
PWTA1	K^{-1}	0.000	-	-
PLWTA1	K^{-1}	0.000	-	-
POTBGIDL	VK^{-1}	-3.638×10^{-4}	-	-
PLTBGIDL	VK^{-1}	0.000	-	-
PWTBGIDL	VK^{-1}	0.000	-	-
PLWTBGIDL	VK^{-1}	0.000	-	-
DTA	K	0.000	-	-
LMIN	m	0.000	-	-
LMAX	m	1.000	-	-
WMIN	m	0.000	-	-
WMAX	m	1.000	-	-

Parameter	Units	Default	Clip low	Clip high
RGO	Ω	0.0	-	-
RINT	$\Omega\,m^2$	0.0	0.0	-
RVPOLY	$\Omega\,m^2$	0.0	0.0	-
RSHG	Ω/□	0.0	0.0	-
DLSIL	m	0.0	-	-

The additional values and clipping values of the additional parameters for the (**p-channel**) model including self-heating (see section 15.6 on page 153) are listed in the table below.

Parameter	Units	Default	Clip low	Clip high
RTH	$^oC/W$	300.0	0.000	-
CTH	$J/^oC$	3.0×10^{-9}	0.000	-
ATH	-	0.0	-	-

The instance parameters are listed in the table below.

Parameter	Units	Default	Clip low	Clip high
L	m	2.000×10^{-6}	-	-
W	m	1.000×10^{-5}	-	-
MULT	-	1.000	0.000	-
NF	-	1.0	1.0	-
NGCON	-	1.0	1.0	2.0
XGW	m	$1.0\text{x}10^{-7}$	-	-

Remark: The parameters *L, W*, and *DTA* are used to calculate the electrical parameters of the actual transistor, as specified in the section on parameter preprocessing.

Parameters of the electrical model

These parameters correspond to the electrical model (MNE, MPE, MOS1102e).

Parameter	Progr. Name	Units	Description
	LEVEL	-	Must be 1102
T_R	TR	^oC	Reference temperature
V_{FB}	VFB	V	Flat-band voltage for the actual transistor at the reference temperature
$S_{T;V_{FB}}$	STVFB	VK^{-1}	Coefficient of the temperature dependence of V_{FB}
k_0	K0	$V^{1/2}$	Body-effect factor for the actual transistor
1/kp	KPINV	$V^{-1/2}$	Inverse of body-effect of the poly-silicon gate for the actual transistor
ϕ_B	PHIB	V	Surface potential at the onset of strong inversion for the actual transistor at the reference temperature
$S_{T;\phi_B}$	STPHIB	VK^{-1}	Coefficient of the temperature dependence of ϕ_B
β	BET	AV^{-2}	Gain factor for the actual transistor at the reference temperature
η_β	ETABET	-	Exponent of the temperature dependence of the gain factor
θ_{sr}	THESR	V^{-1}	Coefficient of the mobility reduction due to surface roughness scattering for the actual transistor at the reference temperature
η_{sr}	ETASR	-	Exponent of the temperature dependence of θ_{sr}
θ_{ph}	THEPH	V^{-1}	Coefficient of the mobility reduction due to phonon scattering for the actual transistor at the reference temperature
η_{ph}	ETAPH	-	Exponent of the temperature dependence of θ_{ph}

Parameter	Progr. Name	Units	Description
η_{mob}	ETAMOB	-	Effective field parameter for dependence on depletion/ inversion charge for the actual transistor at the reference temperature
$S_{T;\eta_{mob}}$	STETAMOB	K^{-1}	Coefficient of the temperature dependence of η_{mob}
ν	NU	-	Exponent of field dependence of mobility model at the reference temperature
υ_{exp}	NUEXP	-	Exponent of the temperature dependence of υ
Cs	CS	-	Coulomb scattering parameter for the actual transistor at the reference temperature.
ηc_s	ETACS	-	Exponent of the temperature dependence of C_S
θ_R	THER	V^{-1}	Coefficient of the series resistance for the actual transistor at the reference temperature: $\theta_R = 2 \cdot \beta \cdot R_S$
η_R	ETAR	-	Exponent of the temperature dependence of θ_R
θ_{R1}	THER1	V	Numerator of the gate voltage dependent part of series resistance for the actual transistor
θ_{R2}	THER2	V	Denominator of the gate voltage dependent part of series resistance for the actual transistor
θ_{sat}	THESAT	V^{-1}	Velocity saturation parameter due to optical/acoustic phonon scattering for the actual transistor at the reference temperature
η_{sat}	ETASAT	-	Exponent of the temperature dependence of θ_{sat}
θ_{Th}	THETH	V^{-3}	Coefficient of self-heating for the actual transistor at the reference temperature
σ_{dibl}	SDIBL	$V^{-1/2}$	Drain-induced barrier-lowering parameter for the actual transistor

Parameter	Progr. Name	Units	Description
m_0	MO	-	Parameter for (short-channel) subthreshold slope for the actual transistor
σ_{sf}	SSF	$V^{-1/2}$	Static-feedback parameter for the actual transistor
α	ALP	-	Factor of the channel-length modulation for the actual transistor
V_P	VP	V	Characteristic voltage of the channel-length modulation
m	MEXP	-	Smoothing factor for the actual transistor
a_1	A1	-	Factor of the weak-avalanche current for the actual transistor at the reference temperature
$S_{T;a_1}$	STA1	K^{-1}	Coefficient of the temperature dependence of a_1
a_2	A2	V	Exponent of the weak-avalanche current for the actual transistor
a_3	A3	-	Factor of the drain-source voltage above which weak-avalanche occurs for the actual transistor
I_{GINV}	IGINV	AV^{-2}	Gain factor for intrinsic gate tunnelling current in inversion for the actual transistor
B_{inv}	BINV	V	Probability factor for intrinsic gate tunnelling current in inversion
I_{GACC}	IGACC	AV^{-2}	Gain factor for intrinsic gate tunnelling current in accumulation for the actual transistor
B_{acc}	BACC	V	Probability factor for intrinsic gate tunnelling current in accumulation
V_{FBov}	VFBOV	V	Flat-band voltage for the source/drain overlap extensions
k_{ov}	KOV	$V^{1/2}$	Body-effect factor for the sourcedrain overlap extensions
I_{GOV}	IGOV	AV^{-2}	Gain factor for source/drain overlap gate tunnelling current for the actual transistor

Parameter	Progr. Name	Units	Description
A_{GIDL}	AGIDL	AV^{-3}	Gain factor for gate-induced drain leakage current for the actual transistor
B_{GIDL}	BGIDL	V	Probability factor for gate-induced leakage current at the reference temperature
$S_{T;B_{GIDL}}$	STBGIDL	VK^{-1}	Coefficient of the temperature dependence of B_{GIDL}
C_{GIDL}	CGIDL	-	Factor for the lateral field dependence of the gate-induced drain leakage current
C_{OX}	COX	F	Oxide capacitance for the intrinsic channel for the actual transistor
C_{GDO}	CGDO	F	Oxide capacitance for the gate-drain overlap for the actual transistor
C_{GSO}	CGSO	F	Oxide capacitance for the gate-source overlap for the actual transistor
-	GATENOISE		Flag for in/exclusion of induced gate thermal noise
N_T	NT	J	Coefficient of the thermal noise at the reference temperature
N_{FA}	NFA	$V^{-1}m^{-4}$	First coefficient of the flicker noise for the actual transistor
N_{FB}	NFB	$V^{-1}m^{-2}$	Second coefficient of the flicker noise for the actual transistor
N_{FC}	NFC	V^{-1}	Third coefficient of the flicker noise for the actual transistor
t_{ox}	TOX	m	Thickness of the gate-oxide layer
ΔT_A	DTA	K	Temperature offset of the device with respect to ambient circuit temperature T_A
R_G	RG	Ω	Gate resistance

The additional parameters for the model including self-heating (see section 15.6 on page 153) are listed in the table below.

Symbol	Progr. Name	Units	Description
R_{TH}	RTH	$^{o}C/W$	Thermal resistance
C_{TH}	CTH	$J/^{o}C$	Thermal capacitance
A_{TH}	ATH	-	Temperature coefficient of the thermal resistance

The *MULT* parameter is listed in the table below.

Symbol	Progr. Name	Units	Description
N_{MULT}	MULT	-	Number of devices in parallel

3 Note

The parameter t_{ox} is used for calculation of the effective oxide thickness (due to quantum-mechanical effects) and the 1/f noise, not for the calculation of β !!!

Default and clipping values (electrical model)

The default values and clipping values as used for the parameters of the electrical MOS model, level 1102 (n-channel) are listed below.

Parameter	Units	Default	Clip low	Clip high
LEVEL	-	1102	-	-
TR	^{o}C	21.0	-273.0	-
VFB	V	-1.0500	-	-
STVFB	VK^{-1}	0.5×10^{-3}	-	-
KO	$V^{1/2}$	0.5000	1.0×10^{-12}	-
KPINV	$V^{-1/2}$	0.000	0.000	-
PHIB	V	0.9500	1.0×10^{-12}	-
STPHIB	VK^{-1}	-8.5×10^{-4}	-	-
BET	AV^{-2}	1.9215×10^{-3}	0.000	-
ETABET	-	1.300	-	-
THESR	V^{-1}	0.3562	1.0×10^{-12}	-
ETASR	-	0.650	-	-
THEPH	V^{-1}	1.29×10^{-2}	1.0×10^{-12}	-
ETAPH	-	1.350	-	-
ETAMOB	-	1.4000	1e-12	-
STETAMOB	K^{-1}	0.000	-	-
NU	-	2.0000	1.000	100
NUEXP	-	5.250	-	-
CS	-	0.0000	0.000	-
ETACS	-	0.0000	-	-
THER	V^{-1}	8.12×10^{-2}	0.000	-
ETAR	-	0.950	-	-

Parameter	Units	Default	Clip low	Clip high
THER1	V	0.0000	0.000	-
THER2	V	1.0000	0.000	-
THESAT	V^{-1}	0.2513	0.000	-
ETASAT	-	1.040	-	-
THETH	V^{-3}	1.0×10^{-5}	0.000	-
SDIBL	$V^{-1/2}$	8.53×10^{-4}	1.0×10^{-12}	-
MO	V	0.0000	0.000	0.500
SSF	$V^{-1/2}$	0.0120	1.0×10^{-12}	-
ALP	-	0.0250	0.000	-
VP	V	0.0500	1.0×10^{-12}	-
MEXP	-	5.0000	1.000	-
A1	-	6.0221	0.000	-
STA1	K^{-1}	0.000	-	-
A2	V	38.017	1.0×10^{-12}	-
A3	-	0.6407	0.000	-
IGINV	AV^{-2}	0.0000	0.000	-
BINV	V	48.000	0.000	-
IGACC	AV^{-2}	0.0000	0.000	-
BACC	V	48.000	0.000	-
VFBOV	V	0.0000	-	-
KOV	$V^{1/2}$	2.5000	1.0×10^{-12}	-
IGOV	AV^{-2}	0.0000	0.000	-
AGIDL	AV^{-3}	0.0000	0.000	-
BGIDL	V	41.000	0.000	-
STBGIDL	VK^{-1}	-3.638×10^{-4}	-	-

Parameter	Units	Default	Clip low	Clip high
CGIDL	-	0.000	0.000	-
COX	F	2.98×10^{-14}	0.000	-
CGDO	F	6.392×10^{-15}	0.000	-
CGSO	F	6.392×10^{-15}	0.000	-
GATENOISE	-	0.0000	0.000	1.000
NT	J	1.656×10^{-20}	0.000	-
NFA	$V^{-1}m^{-4}$	8.323×10^{22}	0.000	-
NFB	$V^{-1}m^{-2}$	2.514×10^{7}	-	-
NFC	V^{-1}	0.0000	-	-
TOX	m	3.2×10^{-9}	1.0×10^{-12}	-
DTA	K	0.000	-	-
RG	Ω	0.000	0.000	-

The default values and clipping values of the additional parameters for the (**n-channel**) model including self-heating (see section 15.6 on page 153) are listed in the table below.

Parameter	Units	Default	Clip low	Clip high
RTH	$^{o}C/W$	300.0	0.000	-
CTH	$J/^{o}C$	3.0×10^{-9}	0.000	-
ATH	-	0.0	-	-

The *MULT* parameter is listed in the table below.

Parameter	Units	Default	Clip low	Clip high
MULT	-	1.000	0.000	-

The default values and clipping values as used for the parameters of the electrical MOS model, level 1102 (p-channel) are listed below.

Parameter	Units	Default	Clip low	Clip high
LEVEL	-	1102	-	-
TR	^{o}C	21.0	-273.0	-
VFB	V	-1.0500	-	-
STVFB	VK^{-1}	0.5×10^{-3}	-	-
KO	$V^{1/2}$	0.5000	1.0×10^{-12}	-
KPINV	$V^{-1/2}$	0.000	0.000	-
PHIB	V	0.9500	1.0×10^{-12}	-
STPHIB	VK^{-1}	-8.5×10^{-4}	-	-
BET	AV^{-2}	3.8140×10^{-4}	0.0	-
ETABET	-	0.500	-	-
THESR	V^{-1}	0.7300	1.0×10^{-12}	-
ETASR	-	0.500	-	-
THEPH	V^{-1}	0.0010	1.0×10^{-12}	-
ETAPH	-	3.750	-	-
ETAMOB	-	3.0000	1e-12	-
STETAMOB	K^{-1}	0.000	-	-
NU	-	2.0000	1.000	100
NUEXP	-	3.230	-	-
CS	-	0.0000	0.000	-
ETACS	-	0.0000	-	-
THER	V^{-1}	7.90×10^{-2}	0.000	-
ETAR	-	0.400	-	-
THER1	V	0.0000	0.000	-

Parameter	Units	Default	Clip low	Clip high
THER2	V	1.0000	0.000	-
THESAT	V^{-1}	0.1728	0.000	-
ETASAT	-	0.860	-	-
THETH	V^{-3}	0.000	0.000	-
SDIBL	$V^{-1/2}$	3.551×10^{-5}	1.0×10^{-12}	-
MO	V	0.0000	0.000	0.500
SSF	$V^{-1/2}$	0.0100	1.0×10^{-12}	-
ALP	-	0.0250	0.000	-
VP	V	0.0500	1.0×10^{-12}	-
MEXP	-	5.0000	1.000	-
A1	-	6.8583	0.000	-
STA1	K^{-1}	0.000	-	-
A2	V	57.324	1.0×10^{-12}	-
A3	-	0.4254	0.000	-
IGINV	AV^{-2}	0.0000	0.000	-
BINV	V	87.500	0.000	-
IGACC	AV^{-2}	0.0000	0.000	-
BACC	V	48.000	0.000	-
VFBOV	V	0.0000	-	-
KOV	$V^{1/2}$	2.5000	1.0×10^{-12}	-
IGOV	AV^{-2}	0.0000	0.000	-
AGIDL	AV^{-3}	0.0000	0.000	-
BGIDL	V	41.000	0.000	-
STBGIDL	VK^{-1}	-3.638×10^{-4}	-	-
CGIDL	-	0.000	0.000	-

Parameter	Units	Default	Clip low	Clip high
COX	F	2.717×10^{-14}	0.000	-
CGDO	F	6.358×10^{-15}	0.000	-
CGSO	F	6.358×10^{-15}	0.000	-
GATENOISE	-	0.0000	0.000	1.000
NT	J	1.656×10^{-20}	0.000	-
NFA	$V^{-1}m^{-4}$	1.900×10^{22}	0.000	-
NFB	$V^{-1}m^{-2}$	5.043×10^{6}	-	-
NFC	V^{-1}	3.627×10^{-10}	-	-
TOX	m	3.2×10^{-9}	1.0×10^{-12}	-
DTA	K	0.000	-	-
RG	Ω	0.000	0.000	-

The default values and clipping values of the additional parameters for the (**p-channel**) model including self-heating (see section 15.6 on page 153) are listed in the table below.

Parameter	Units	Default	Clip low	Clip high
RTH	$^{o}C/W$	300.0	0.000	-
CTH	$J/^{o}C$	3.0×10^{-9}	0.000	-
ATH	-	0.0	-	-

The *MULT* parameter is listed in the table below.

Parameter	Units	Default	Clip low	Clip high
MULT	-	1.000	0.000	-

15.3.3 Model constants

This table gives the symbolic representation, the recommended programming names and the value of the various physical constants used in MOS Model 11.

Constant	Progr. Name	Units	Description
T_0	TO	K	Offset for conversion from Celsius to Kelvin temperature scale (273.15)
k_B	KB	JK^{-1}	Boltzmann constant ($1.3806226.10^{-23}$)
q	Q	C	Elementary unit charge ($1.6021918.10^{-19}$)
ε_{ox}	EPSOX	Fm^{-1}	Absolute permittivity of the oxide layer ($3.453143800.10^{-11}$)
QM_N	QMN	$Vm^{4/3}C^{-2/3}$	Constant of quantum-mechanical behavior of electrons ($5.951993.10^{+00}$)
QM_p	QMP	$Vm^{4/3}C^{-2/3}$	Constant of quantum-mechanical behavior of holes ($7.448711.10^{+00}$)
χ_{BN}	CHIBN	V	Tunnelling barrier height for electrons for Si/SiO2-structure ($3.1.10^{+00}$)
χ_{Bp}	CHIBP	V	Tunnelling barrier height for holes for Si/SiO2-structure ($4.5.10^{+00}$)

15.4 Parameter Scaling

15.4.1 Geometrical scaling and temperature scaling

In this section the geometry and temperature scaling rules for the model parameters will be given. The temperature scaling rules have already been given in Section 15.2.2, but they are repeated here for the sake of completeness.

Calculation of Transistor Geometry

$$L_E = L - \Delta L = L + \Delta L_{PS} - 2 \cdot \Delta L_{\text{overlap}} \tag{15.121}$$

$$W_E = W - \Delta W = W/NF + \Delta W_{OD} - 2 \cdot \Delta W_{\text{narrow}} \tag{15.122}$$

WARNING : L_E and W_E after calculation cannot be less than 1.0×10^{-9} !

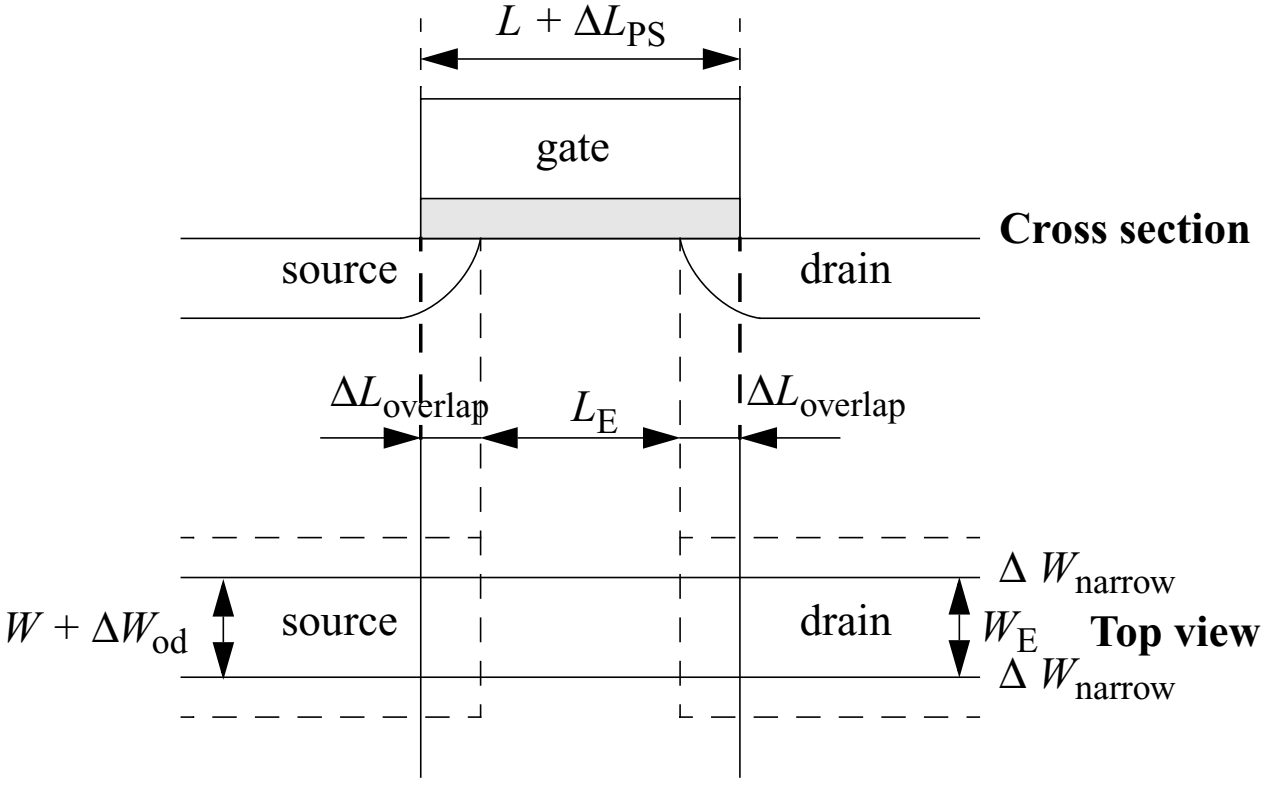


Figure 70: Specification of the dimensions of a MOS transistor

Calculation of Geometry-Dependent Parameters

In MOS Model 11, Level 1102, parameter binning has been facilitated by adding a second, separate set of geometry scaling rules. Consequently, besides the physical geometrical scaling rules there is also a set of binning geometrical scaling rules. The physical geometry scaling rules. The physical geometry scaling rules of Level 1102 have been developed to give a good description over the whole geometry range of CMOS technologies. For processes under development, however, it is sometimes useful to have more flexible scaling relations. In this case one could opt for a binning strategy, where the accuracy with geometry is mostly determined by the number of bins used. The physical scaling rules of Level 1102 are not straightforwardly applicable to binning strategies, since they may result in discontinuities in parameter values at the bin boundaries. Consequently, special binning geometrical scaling relations have been developed, which guarantee continuity in the model parameters at the bin boundaries.

It should be noted that when using the source code of the Modelkit on the Philips' website (which can be found at http://www.semiconductors.philips.com/Philips_Models):

1. The physical geometry scaling rules can be selected by using Level 11020, while
2. The binning geometry scaling rules can be selected by using Level 11021.

Three types of binning geometrical scaling rules can be distinguished:

1. Type I

$$P(W_E,L_E) = P_0 + \frac{L_{EN}}{L_E} \cdot P_L + \frac{W_{EN}}{W_E} \cdot P_W + \frac{L_{EN}}{L_E} \cdot \frac{W_{EN}}{W_E} \cdot P_{LW} \qquad (15.123)$$

2. Type II

$$P(W_E,L_E) = P_0 + \frac{L_E}{L_{EN}} \cdot P_L + \frac{W_E}{W_{EN}} \cdot P_W + \frac{L_E}{L_{EN}} \cdot \frac{W_E}{W_{EN}} \cdot P_{LW} \qquad (15.124)$$

3. Type III

$$P(W_E,L_E) = P_0 + \frac{L_{EN}}{L_E} \cdot P_L + \frac{W_E}{W_{EN}} \cdot P_W + \frac{W_E}{L_E} \cdot P_{LW} \quad (15.125)$$

In these equations L_{EN} and W_{EN} are constants. Table 18 below gives a survey of the parameters scaling.

When using the three binning rules given, the scaling parameters for one bin can be directly calculated from the minisets of the four corner devices of the bin. The binning scheme ensures that the minisets are exactly reproduced in the bin corners, and that no humps occur in parameter values accross bin borders. The exact way to calculate binning parameters from minisets is described in Appendix B.

Table 18: Survey of parameters scaling. The third column indicates if there is a physical geometrical scaling rule for the parameter; the fourth column indicates the type of binning geometrical scaling rule for the parameter.

#	**Parameter**	**physical scaling**	**binning**	#	**parameter**	**physi-cal scaling**	**binning**
0	$LEVEL$	no	no	1	T_R	no	no
2	V_{FB}	no	no	3	$S_{T;V_{FB}}$	no	type I
4	k_0	yes	type I	5	$1/k_P$	no	no
6	ϕ_B	yes	type I	7	$S_{T;\phi_B}$	no	type I
8	β	yes	type III	9	η_β	yes	type I
10	θ_{sr}	yes	type I	11	η_{sr}	no	type I
12	θ_{ph}	yes	type I	13	η_{ph}	no	type I
14	η_{mob}	yes	type I	15	$S_{T;\eta_{mob}}$	no	type I

Table 18: Survey of parameters scaling. The third column indicates if there is a physical geometrical scaling rule for the parameter; the fourth column indicates the type of binning geometrical scaling rule for the parameter.

#	Parameter	physical scaling	binning	#	parameter	physi-cal scaling	binning
16	υ	no	no	17	υ_{EXP}	no	type I
18	C_s	yes	type I	19	η_{C_s}	no	type I
20	θ_R	yes	type I	21	η_R	no	type I
22	θ_{R1}	no	no	23	θ_{R2}	no	no
24	θ_{sat}	yes	type I	25	η_{sat}	no	type I
26	θ_{Th}	yes	type I	27	σ_{dibl}	yes	type I
28	m_0	yes	type I	29	σ_{sf}	yes	type I
30	α	yes	type I	31	V_P	no	no
32	m	yes	type I	33	a_1	yes	type I
34	$S_{T;a_1}$	no	type I	35	a_2	yes	type I
36	a_3	yes	type I	37	I_{GINV}	yes	type II
38	B_{INV}	no	type I	39	I_{GACC}	yes	type II
40	B_{ACC}	no	type I	41	V_{RFBov}	no	no
42	k_{ov}	no	no	43	I_{GOV}	yes	type III
44	A_{GIDL}	yes	type III	45	B_{GIDL}	yes	type I

Table 18: Survey of parameters scaling. The third column indicates if there is a physical geometrical scaling rule for the parameter; the fourth column indicates the type of binning geometrical scaling rule for the parameter.

#	Parameter	physical scaling	binning	#	parameter	physi-cal scaling	binning
46	$S_{T;B_{GIDL}}$	yes	type I	47	C_{GIDL}	yes	type I
48	C_{ox}	yes	type II	49	C_{GDO}	yes	type III
50	C_{GSO}	yes	type III	51	$GATENOISE$	no	no
52	N_T	no	no	53	N_{FA}	yes	type I
54	N_{FB}	yes	type I	55	N_{FC}	yes	type I
56	t_{ox}	no	no	57	ΔT_A	no	no
58	N_{MULT}	no	no				

Calculation of Geometry-Dependent Parameters using the Physical Scaling Rules

$$L_{EN} = 10^{-6} \tag{15.126}$$

$$W_{EN} = 10^{-6} \tag{15.127}$$

Calculation of Threshold-Voltage Parameters

$$klen = 1 + \frac{L_{EN}}{L_E} \cdot S_{L;k_0} + \left(\frac{L_{EN}}{L_E}\right)^2 \cdot S_{L2;k_0} + \left(\frac{L_{EN}}{L_E}\right)^{SL3KOEXP} \cdot S_{L3;k_0}$$

$$kwid = 1 + \frac{W_{EN}}{W_E} \cdot S_{W;k_0}$$

$$k_0 = k_{0R} \cdot klen \cdot kwid \tag{15.128}$$

$$\phi_B = \phi_{BR} \cdot \left[1 + \frac{L_{EN}}{L_E} \cdot S_{L;\phi_B} + \left(\frac{L_{EN}}{L_E} \right)^2 \cdot S_{L2;\phi_B} \right] \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;\phi_B} \right] \tag{15.129}$$

Calculation of Mobility/Series-Resistance Parameters

$$G_{P,E} = 1 + f_{\beta,1} \cdot \frac{L_{P,1}}{L_E} \cdot \left\{ 1 - \exp\left(-\frac{L_E}{L_{P,1}} \right) \right\} + \quad f_{\beta,2} \cdot \frac{L_{P,2}}{L_E} \cdot \left\{ 1 - \exp\left(-\frac{L_E}{L_{P,2}} \right) \right\} \tag{15.130}$$

$$\beta = \frac{\beta_{sq}}{G_{P,E}} \cdot \frac{W_E}{L_E} \tag{15.131}$$

$$\theta_{sr} = \theta_{srR} \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;\theta_{sr}} \right] \tag{15.132}$$

$$\theta_{ph} = \theta_{phR} \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;\theta_{ph}} \right] \tag{15.133}$$

$$\eta_{mob} = \theta_{mobR} \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;\eta_{mob}} \right] \tag{15.134}$$

$$C_s = C_{sR} \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;C_s} \right] \cdot \left[1 + S_{L;C_s} \cdot \left\{ \left(\frac{L_{EN}}{L_E} \right)^{C_{sEXP}} - 1 \right\} \right] \quad (15.135)$$

$$\theta_R = \theta_{RR} \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;\theta_R} \right] \cdot \frac{L_{EN}}{L_E} \cdot \frac{1}{G_{P,E}} \quad (15.136)$$

$$\theta_{sat} = \theta_{satR} \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;\theta_{sat}} \right] \cdot \left[1 + S_{L;\theta_{sat}} \cdot \left\{ \left(\frac{L_{EN}}{L_E} \right)^{\theta_{satEXP}} - 1 \right\} \right] \quad (15.137)$$

Calculation of Conductance Parameters

$$\theta_{Th} = \theta_{ThR} \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;\theta_{Th}} \right] \cdot \left[\frac{L_{EN}}{L_E} \right]^{\theta_{ThEXP}} \quad (15.138)$$

$$\sigma_{sf} = \sigma_{sfR} \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;\sigma_{sf}} \right] \cdot \left[1 + \frac{L_{EN}}{L_E} \cdot S_{L;\sigma_{sf}} \right] \quad (15.139)$$

$$\alpha = \alpha_R \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;\alpha} \right] \cdot \left[1 + S_{L;\alpha} \cdot \left\{ \left(\frac{L_{EN}}{L_E} \right)^{\alpha_{EXP}} - 1 \right\} \right] \quad (15.140)$$

Calculation of Sub-Threshold Parameters

$$\sigma_{dibl} = \sigma_{dibl0} \cdot \left(\frac{L_{EN}}{L_E} \right)^{\sigma_{diblEXP}} \quad (15.141)$$

$$m_0 = m_{00} + m_{0R} \cdot \left(\frac{L_{EN}}{L_E} \right)^{m_{0EXP}} \quad (15.142)$$

Calculation of Smoothing Parameters

$$L_{max} = 10 \cdot 10^{-6} \tag{15.143}$$

$$m = \frac{8 \cdot (L_{max} - L_{min})}{L_{max} - 4 \cdot L_{min} + 3 \cdot \frac{L_{max} \cdot L_{min}}{L_E}} \tag{15.144}$$

Calculation of Weak-Avalanche Parameters

$$a_1 = a_{1R} \cdot \left[1 + \frac{L_{EN}}{L_E} \cdot S_{L;a_1}\right] \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;a_1}\right] \tag{15.145}$$

$$a_2 = a_{2R} \cdot \left[1 + \frac{L_{EN}}{L_E} \cdot S_{L;a_2}\right] \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;a_2}\right] \tag{15.146}$$

$$a_3 = a_{3R} \cdot \left[1 + \frac{L_{EN}}{L_E} \cdot S_{L;a_3}\right] \cdot \left[1 + \frac{W_{EN}}{W_E} \cdot S_{W;a_3}\right] \tag{15.147}$$

Calculation of Gate Current Parameters

$$I_{GINV} = \frac{W_E \cdot L_E}{W_{EN} \cdot L_{EN}} \cdot I_{GINVR} \tag{15.148}$$

$$I_{GACC} = \frac{W_E \cdot L_E}{W_{EN} \cdot L_{EN}} \cdot I_{GACCR} \tag{15.149}$$

$$I_{GOV} = \frac{W_E}{W_{EN}} \cdot I_{GOVR} \tag{15.150}$$

Calculation of Gate-Induced Drain Leakage Parameters

$$A_{GIDL} = \frac{W_E}{W_{EN}} \cdot A_{GIDLR} \tag{15.151}$$

Calculation of Charge Parameters

$$C_{OX} = \varepsilon_{ox} \cdot \frac{W_E \cdot L_E}{t_{ox}} \tag{15.152}$$

$$C_{GDO} = \frac{W_E}{W_{EN}} \cdot C_{ol} \tag{15.153}$$

$$C_{GSO} = \frac{W_E}{W_{EN}} \cdot C_{ol} \tag{15.154}$$

Calculation of Noise Parameters

$$N_{FA} = \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E} \cdot N_{FAR} \tag{15.155}$$

$$N_{FB} = \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E} \cdot N_{FBR} \tag{15.156}$$

$$N_{FC} = \frac{W_{EN} \cdot L_{EN}}{W_E \cdot L_E} \cdot N_{FCR} \tag{15.157}$$

Calculation of Mobility/Series-Resistance Temperature-Scaling Coefficients

$$\eta_\beta = \eta_{\beta R} + S_{L;\eta_\beta} \cdot \frac{L_{EN}}{L_E} \tag{15.158}$$

Calculation of Geometry-Dependent Parameters using the Binning Scaling Rules

Note that for each bin (W_{min},W_{max},L_{min},L_{max}), there is a separate parameter set, which is valid for (W,L) values with $W_{min} \le W \le W_{max}$ and $L_{min} \le L \le L_{max}$.

$$L_{EN} = 10^{-6} \tag{15.159}$$

$$W_{EN} = 10^{-6} \tag{15.160}$$

Calculation of Threshold-Voltage Parameters

$$k_0 = P_{0;k_0} + \frac{L_{EN}}{L_E} \cdot P_{L;k_0} + \frac{W_{EN}}{W_E} \cdot P_{W;k_0} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;k_0} \tag{15.161}$$

$$\phi_B = P_{0;\phi_B} + \frac{L_{EN}}{L_E} \cdot P_{L;\phi_B} + \frac{W_{EN}}{W_E} \cdot P_{W;\phi_B} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;\phi_B} \tag{15.162}$$

Calculation of Mobility/Series-Resistance Parameters

$$\beta = P_{0;\beta} + \frac{L_{EN}}{L_E} \cdot P_{L;\beta} + \frac{W_E}{W_{EN}} \cdot P_{W;\beta} + \frac{W_E}{L_E} \cdot P_{LW;\beta} \tag{15.163}$$

$$\theta_{sr} = P_{0;\theta_{sr}} + \frac{L_{EN}}{L_E} \cdot P_{L;\theta_{sr}} + \frac{W_{EN}}{W_E} \cdot P_{W;\theta_{sr}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;\theta_{sr}} \tag{15.164}$$

$$\theta_{ph} = P_{0;\theta_{ph}} + \frac{L_{EN}}{L_E} \cdot P_{L;\theta_{ph}} + \frac{W_{EN}}{W_E} \cdot P_{W;\theta_{ph}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;\theta_{ph}} \quad (15.165)$$

$$\eta_{mob} = P_{0;\eta_{mob}} + \frac{L_{EN}}{L_E} \cdot P_{L;\eta_{mob}} + \frac{W_{EN}}{W_E} \cdot P_{W;\eta_{mob}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;\eta_{mob}} \quad (15.166)$$

$$C_s = P_{0;C_s} + \frac{L_{EN}}{L_E} \cdot P_{L;C_s} + \frac{W_{EN}}{W_E} \cdot P_{W;C_s} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;C_s} \quad (15.167)$$

$$\theta_R = P_{0;\theta_R} + \frac{L_{EN}}{L_E} \cdot P_{L;\theta_R} + \frac{W_{EN}}{W_E} \cdot P_{W;\theta_R} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;\theta_R} \quad (15.168)$$

$$\theta_{sat} = P_{0;\theta_{sat}} + \frac{L_{EN}}{L_E} \cdot P_{L;\theta_{sat}} + \frac{W_{EN}}{W_E} \cdot P_{W;\theta_{sat}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;\theta_{sat}} \quad (15.169)$$

Calculation of Conductance Parameters

$$\theta_{Th} = P_{0;\theta_{Th}} + \frac{L_{EN}}{L_E} \cdot P_{L;\theta_{Th}} + \frac{W_{EN}}{W_E} \cdot P_{W;\theta_{Th}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;\theta_{Th}} \quad (15.170)$$

$$\sigma_{sf} = P_{0;\sigma_{sf}} + \frac{L_{EN}}{L_E} \cdot P_{L;\sigma_{sf}} + \frac{W_{EN}}{W_E} \cdot P_{W;\sigma_{sf}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;\sigma_{sf}} \quad (15.171)$$

$$\alpha = P_{0;\alpha} + \frac{L_{EN}}{L_E} \cdot P_{L;\alpha} + \frac{W_{EN}}{W_E} \cdot P_{W;\alpha} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;\alpha} \quad (15.172)$$

Calculation of Sub-Threshold Parameters

$$\sigma_{dibl} = P_{0;\sigma_{dibl}} + \frac{L_{EN}}{L_E} \cdot P_{L;\sigma_{dibl}} + \frac{W_{EN}}{W_E} \cdot P_{W;\sigma_{dibl}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;\sigma_{dibl}} \tag{15.173}$$

$$m_0 = P_{0;m_0} + \frac{L_{EN}}{L_E} \cdot P_{L;m_0} + \frac{W_{EN}}{W_E} \cdot P_{W;m_0} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;m_0} \tag{15.174}$$

Calculation of Smoothing Parameters

$$\frac{1}{m} = P_{0;m} + \frac{L_{EN}}{L_E} \cdot P_{L;m} + \frac{W_{EN}}{W_E} \cdot P_{W;m} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;m} \tag{15.175}$$

Calculation of Weak-Avalanche Parameters

$$a_1 = P_{0;a_1} + \frac{L_{EN}}{L_E} \cdot P_{L;a_1} + \frac{W_{EN}}{W_E} \cdot P_{W;a_1} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;a_1} \tag{15.176}$$

$$a_2 = P_{0;a_2} + \frac{L_{EN}}{L_E} \cdot P_{L;a_2} + \frac{W_{EN}}{W_E} \cdot P_{W;a_2} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;a_2} \tag{15.177}$$

$$a_3 = P_{0;a_3} + \frac{L_{EN}}{L_E} \cdot P_{L;a_3} + \frac{W_{EN}}{W_E} \cdot P_{W;a_3} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;a_3} \tag{15.178}$$

Calculation of Gate Current Parameters

$$I_{GINV} = P_{0;I_{GINV}} + \frac{L_E}{L_{EN}} \cdot P_{L;I_{GINV}} + \frac{W_E}{W_{EN}} \cdot P_{W;I_{GINV}} + \frac{L_E \cdot W_E}{L_{EN} \cdot W_{EN}} \cdot P_{LW;I_{GINV}}$$

(15.179)

$$B_{INV} = P_{0;B_{INV}} + \frac{L_{EN}}{L_E} \cdot P_{L;B_{INV}} + \frac{W_{EN}}{W_E} \cdot P_{W;B_{INV}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;B_{INV}}$$

(15.180)

$$I_{GACC} = P_{0;I_{GACC}} + \frac{L_E}{L_{EN}} \cdot P_{L;I_{GACC}} + \frac{W_E}{W_{EN}} \cdot P_{W;I_{GACC}} + \frac{L_E \cdot W_E}{L_{EN} \cdot W_{EN}} \cdot P_{LW;I_{GACC}}$$

(15.181)

$$B_{acc} = P_{0;B_{acc}} + \frac{L_{EN}}{L_E} \cdot P_{L;B_{acc}} + \frac{W_{EN}}{W_E} \cdot P_{W;B_{acc}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;B_{acc}}$$

(15.182)

$$I_{GOV} = P_{0;I_{GOV}} + \frac{L_{EN}}{L_E} \cdot P_{L;I_{GOV}} + \frac{W_E}{W_{EN}} \cdot P_{W;I_{GOV}} + \frac{W_E}{L_E} \cdot P_{LW;I_{GOV}} \quad (15.183)$$

Calculation of Gate-Induced Drain Leakage Parameters

$$A_{GIDL} = P_{0;A_{GIDL}} + \frac{L_{EN}}{L_E} \cdot P_{L;A_{GIDL}} + \frac{W_E}{W_{EN}} \cdot P_{W;A_{GIDL}} + \frac{W_E}{L_E} \cdot P_{LW;A_{GIDL}} \quad (15.184)$$

$$B_{GIDL} = P_{0;B_{GIDL}} + \frac{L_{EN}}{L_E} \cdot P_{L;B_{GIDL}} + \frac{W_{EN}}{W_E} \cdot P_{W;B_{GIDL}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;B_{GIDL}}$$

(15.185)

$$C_{GIDL} = P_{0;C_{GIDL}} + \frac{L_{EN}}{L_E} \cdot P_{L;C_{GIDL}} + \frac{W_{EN}}{W_E} \cdot P_{W;C_{GIDL}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;C_{GIDL}}$$

(15.186)

Calculation of Charge Parameters

$$C_{OX} = P_{0;C_{ox}} + \frac{L_E}{L_{EN}} \cdot P_{L;C_{ox}} + \frac{W_E}{W_{EN}} \cdot P_{W;C_{ox}} + \frac{L_E \cdot W_E}{L_{EN} \cdot W_{EN}} \cdot P_{LW;C_{ox}} \quad (15.187)$$

$$C_{GDO} = P_{0;C_{GD0}} + \frac{L_{EN}}{L_E} \cdot P_{L;C_{GD0}} + \frac{W_E}{W_{EN}} \cdot P_{W;C_{GD0}} + \frac{W_E}{L_E} \cdot P_{LW;C_{GD0}} \quad (15.188)$$

$$C_{GSO} = P_{0;C_{GS0}} + \frac{L_{EN}}{L_E} \cdot P_{L;C_{GS0}} + \frac{W_E}{W_{EN}} \cdot P_{W;C_{GS0}} + \frac{W_E}{L_E} \cdot P_{LW;C_{GS0}} \quad (15.189)$$

Calculation of Noise Parameters

$$N_{FA} = P_{0;N_{FA}} + \frac{L_{EN}}{L_E} \cdot P_{L;N_{FA}} + \frac{W_{EN}}{W_E} \cdot P_{W;N_{FA}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;N_{FA}} \quad (15.190)$$

$$N_{FB} = P_{0;N_{FB}} + \frac{L_{EN}}{L_E} \cdot P_{L;N_{FB}} + \frac{W_{EN}}{W_E} \cdot P_{W;N_{FB}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;N_{FB}} \quad (15.191)$$

$$N_{FC} = P_{0;N_{FC}} + \frac{L_{EN}}{L_E} \cdot P_{L;N_{FC}} + \frac{W_{EN}}{W_E} \cdot P_{W;N_{FC}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;N_{FC}} \quad (15.192)$$

Calculation of Treshold-voltage Temperature-Scaling Coefficients

$$S_{T;V_{FB}} = P_{0;T;V_{FB}} + \frac{L_{EN}}{L_E} \cdot P_{L;T;V_{FB}} + \frac{W_{EN}}{W_E} \cdot P_{W;T;V_{FB}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;V_{FB}}$$

(15.193)

$$S_{T;\phi_B} = P_{0;T;\phi_B} + \frac{L_{EN}}{L_E} \cdot P_{L;T;\phi_B} + \frac{W_{EN}}{W_E} \cdot P_{W;T;\phi_B} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;\phi_B}$$

(15.194)

Calculation of Mobility/Series-Resistance Temperature-Scaling Coefficients

$$\eta_\beta = P_{0;T;\eta_\beta} + \frac{L_{EN}}{L_E} \cdot P_{L;T;\eta_\beta} + \frac{W_{EN}}{W_E} \cdot P_{W;T;\eta_\beta} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;\eta_\beta}$$

(15.195)

$$\eta_{sr} = P_{0;T;\eta_{sr}} + \frac{L_{EN}}{L_E} \cdot P_{L;T;\eta_{sr}} + \frac{W_{EN}}{W_E} \cdot P_{W;T;\eta_{sr}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;\eta_{sr}}$$

(15.196)

$$\eta_{ph} = P_{0;T;\eta_{ph}} + \frac{L_{EN}}{L_E} \cdot P_{L;T;\eta_{ph}} + \frac{W_{EN}}{W_E} \cdot P_{W;T;\eta_{ph}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;\eta_{ph}}$$

(15.197)

$$S_{T;\eta_{mob}} = P_{0;T;\eta_{mob}} + \frac{L_{EN}}{L_E} \cdot P_{L;T;\eta_{mob}} + \frac{W_{EN}}{W_E} \cdot P_{W;T;\eta_{mob}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;\eta_{mob}}$$

(15.198)

$$\upsilon_{exp} = P_{0;T;\upsilon_{exp}} + \frac{L_{EN}}{L_E} \cdot P_{L;T;\upsilon_{exp}} + \frac{W_{EN}}{W_E} \cdot P_{W;T;\upsilon_{exp}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;\upsilon_{exp}}$$

(15.199)

$$\eta_{C_s} = P_{0;T;\eta_{C_s}} + \frac{L_{EN}}{L_E} \cdot P_{L;T;\eta_{C_s}} + \frac{W_{EN}}{W_E} \cdot P_{W;T;\eta_{C_s}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;\eta_{C_s}}$$

(15.200)

$$\eta_R = P_{0;T;\eta_R} + \frac{L_{EN}}{L_E} \cdot P_{L;T;\eta_R} + \frac{W_{EN}}{W_E} \cdot P_{W;T;\eta_R} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;\eta_R}$$

(15.201)

$$\eta_{sat} = P_{0;T;\eta_{sat}} + \frac{L_{EN}}{L_E} \cdot P_{L;T;\eta_{sat}} + \frac{W_{EN}}{W_E} \cdot P_{W;T;\eta_{sat}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;\eta_{sat}}$$

(15.202)

Calculation of Weak-Avalanche Temperature-Scaling Coefficients

$$S_{T;a_1} = P_{0;T;a_1} + \frac{L_{EN}}{L_E} \cdot P_{L;T;a_1} + \frac{W_{EN}}{W_E} \cdot P_{W;T;a_1} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;a_1}$$

(15.203)

Calculation of Gate-Induced Drain Leakage Temperature-Scaling Coefficients

$$S_{T;B_{GIDL}} = P_{0;T;B_{GIDL}} + \frac{L_{EN}}{L_E} \cdot P_{L;T;B_{GIDL}} + \frac{W_{EN}}{W_E} \cdot P_{W;T;B_{GIDL}} + \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \cdot P_{LW;T;B}$$

(15.204)

Calculation of Temperature-Dependent Parameters

Calculation of Transistor Temperature

3 Note

Note the addition of the voltage V_{dT} of the thermal node in order to include self-heating, see Section 15.6.

$$T_{KR} = T_0 + T_R \tag{15.205}$$

$$T_{KD} = T_0 + T_A + \Delta T_A + V_{dT} \tag{15.206}$$

Calculation of Threshold-Voltage Parameters

$$\phi_T = \frac{k_B \cdot T_{KD}}{q} \tag{15.207}$$

$$V_{FB_T} = V_{FB} + (T_{KD} - T_{KR}) \cdot S_{T;V_{FB}} \tag{15.208}$$

$$\phi_{B_T} = \phi_B + (T_{KD} - T_{KR}) \cdot S_{T;\phi_B} \tag{15.209}$$

Calculation of Mobility/Series-Resistance Parameters

$$\beta_T = \beta \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta_\beta} \tag{15.210}$$

$$\theta_{sr_T} = \theta_{sr} \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta_{sr}} \tag{15.211}$$

$$\theta_{ph_T} = \theta_{ph} \cdot \left(\frac{T_{KD}}{T_{KR}}\right)^{\eta_{ph}} \tag{15.212}$$

$$\eta_{mob_T} = \eta_{mob} \cdot [1 + (T_{KD} - T_{KR}) \cdot S_{T;\eta_{mob}}] \tag{15.213}$$

$$C_{s_T} = C_s \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta_{C_s}} \tag{15.214}$$

$$\nu_T = 1 + (\nu - 1) \cdot (T_{KR} / T_{KD})^{\nu_{exp}} \tag{15.215}$$

$$\theta_{R_T} = \theta_R \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta_R} \tag{15.216}$$

$$\theta_{sat_T} = \theta_{sat} \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta_{sat}} \tag{15.217}$$

Calculation of Conductance Parameters

$$\theta_{Th_T} = \theta_{Th} \cdot \left(\frac{T_{KR}}{T_{KD}}\right)^{\eta_\beta} \tag{15.218}$$

Calculation of Weak-Avalanche Parameters

$$a_{1_T} = a_1 \cdot [1 + (T_{KD} - T_{KR}) \cdot S_{T;a_1}] \tag{15.219}$$

Calculation of Gate-Induced Drain Leakage Parameters

$$B_{GIDL_T} = B_{GIDL} \cdot [1 + (T_{KD} - T_{KR}) \cdot S_{T;B_{GIDL}}] \tag{15.220}$$

Calculation of Noise Parameters

$$N_{T_T} = \frac{T_{KD}}{T_{KR}} \cdot N_T \tag{15.221}$$

15.5 Model Equations

The electrical equations of MOS Model 11 to be implemented are essentially the basic equations of Section 15.2. Since in circuit design equal parallel circuited transistors are frequently applied the specification of one transistor together with a multiplication factor $NF.N_{MULT}$ in the circuit description is convenient and saves computation time. The general and safe method to implement this mechanism into the model is to evaluate the currents, charges, noise spectral densities and their derivatives with respect to the external voltages and, at the end, to multiply them by $NF.N_{MULT}$. In MOS Model 11 it is allowed to circumvent these multiplications for each model evaluation during circuit simulation by adjusting some parameters. In this case the following rules apply:

$$\beta = \beta \cdot NF \cdot N_{MULT}$$

$$I_{GINV} = I_{GINV} \cdot NF \cdot N_{MULT}$$

$$I_{GACC} = I_{GACC} \cdot NF \cdot N_{MULT}$$

$$I_{GOV} = I_{GOV} \cdot NF \cdot N_{MULT}$$

$$A_{GIDL} = A_{GIDL} \cdot NF \cdot N_{MULT}$$

$$C_{OX} = C_{OX} \cdot NF \cdot N_{MULT}$$

$$C_{GDO} = C_{GDO} \cdot NF \cdot N_{MULT}$$

$$C_{GSO} = C_{GSO} \cdot NF \cdot N_{MULT}$$

$$N_{FA} = \frac{N_{FA}}{NF \cdot N_{MULT}}$$

$$N_{FB} = \frac{N_{FB}}{NF \cdot N_{MULT}}$$

$$N_{FC} = \frac{N_{FC}}{NF \cdot N_{MULT}}$$

Although the basic equations, given in Section 15.2, form a complete set of model equations, they are not yet suited for a circuit simulator. Several equations have to be adapted in order to obtain smooth transitions of the characteristics between adjacent regions of operation and to prevent numerical problems during the iteration process for solving the network equations. In the following section a list of numerical adaptations and elucidations is given, followed by the extended set of model equations.

The definition of the hyp-function, which provides for a smooth C_∞-continuous clipping, is to be found in Appendix A.

15.5.1 Extended Equations

In the following sections a function is denoted by *F{variable, ...}*, where *F* denotes the function name and the function variables are enclosed by braces {}. The definition of the hyp-functions can be found in *Appendix A Hyp functions*.

Internal Parameters

$$\varepsilon_1 = 1 \cdot 10^{-2}$$

$$\varepsilon_2 = 4 \cdot 10^{-2}$$

$$\varepsilon_3 = 1 \cdot 10^{-4}$$

$$P_D = 1 + (k_0/k_p)^2$$

$$V_{limit} = 4 \cdot \phi_T$$

$$\theta_{R_{eff}} = \frac{1}{2} \cdot \theta_{R_T} \cdot \left(1 + \frac{\theta_{R1}}{1/2 + \theta_{R2}}\right)$$

$$m_{\phi T} = (1 + m_0) \cdot \phi_T$$

$$Acc = \left.\frac{\partial \psi_s}{\partial V_{GB}}\right|_{V_{GB} = V_{FB_T}} = \frac{1}{1 + k_0 / \sqrt{2 \cdot \phi_T}}$$

$$Acc_{ov} = \left.\frac{\partial \psi_{sov}}{\partial V_{GB}}\right|_{V_{GB} = V_{FBov}} = \frac{1}{1 + k_{ov} / \sqrt{2 \cdot \phi_T}}$$

$$QM_{\psi} = \begin{cases} QM_N \cdot (\varepsilon_{ox} / t_{ox})^{2/3} & \text{for NMOS} \\ QM_P \cdot (\varepsilon_{ox} / t_{ox})^{2/3} & \text{for PMOS} \end{cases}$$

$$QM_{tox} = \frac{2}{5} \cdot QM_{\psi}$$

$$\chi_{B_{inv}} = \begin{cases} \chi_{B_N} & \text{for NMOS} \\ \chi_{B_P} & \text{for PMOS} \end{cases}$$

$$\chi_{B_{acc}} = \chi_{B_N}$$

Extended Current Equations

$$V_{GB_{eff}} = \text{hyp}_1(V_{GS} + V_{SB} - V_{FB_T}; \varepsilon_1) \tag{15.222}$$

$$V_{SB_t} = \text{hyp}_1(V_{SB} + 0.9 \cdot \phi_{B_T}; \varepsilon_2) + 0.1 \cdot \phi_{B_T} \tag{15.223}$$

$$\psi_{sat_0} = \left(\frac{\sqrt{P_D \cdot V_{GB_{eff}} + k_0^2/4} - k_0/2}{P_D} \right)^2 \tag{15.224}$$

Drain induced barrier lowering and Static Feedback

$$D_{dibl} = \sigma_{dibl} \cdot \sqrt{V_{SB_t}} \tag{15.225}$$

$$D_{sf} = \sigma_{sf} \cdot \sqrt{\mathrm{hyp}_1(\psi_{sat_0} - V_{SB_t}, \varepsilon_2)} \tag{15.226}$$

$$V_{DS_{eff}} = \frac{V_{DS}^4}{(V_{limit}^2 + V_{DS}^2)^{3/2}} \tag{15.227}$$

$$\Delta V_G = \sqrt{D_{dibl}{}^2 + D_{sf}{}^2} \cdot V_{DS_{eff}} \tag{15.228}$$

Effective Gate-Bulk Voltage

$$V_{GB}^* = V_{GS} + V_{SB} + \Delta V_G - V_{FB_T} \tag{15.229}$$

Drain Saturation Voltage

Equations 15.230 to 15.234 are only calculated for $V_{GB}^* > 0$:

$$\psi_{sat_1} = \left(\frac{\sqrt{P_D \cdot V_{GB}^* + k_0{}^2/4} - k_0/2}{P_D} \right)^2 \tag{15.230}$$

$$V_{DSAT_{long}} = \psi_{sat_1} - V_{SB_t} \tag{15.231}$$

$$T_{sat} = \begin{cases} \theta_{sat_T} & \text{for NMOS} \\ \dfrac{\theta_{sat_T}}{(1 + \theta_{sat_T}{}^2 \cdot V_{DSAT_{long}}{}^2)^{1/4}} & \text{for PMOS} \end{cases} \tag{15.232}$$

$$\Delta_{SAT} = \frac{(T_{sat} - \theta_{R_{eff}}) \cdot V_{DSAT_{long}}}{\frac{1}{2} \cdot \left(\sqrt{2} + \sqrt{2 + 2 \cdot T_{sat}^2 \cdot V_{DSAT_{long}}^2} \right) + \theta_{R_{eff}} \cdot V_{DSAT_{long}}} \tag{15.233}$$

$$V_{DSAT_{short}} = V_{DSAT_{long}} \cdot \left[1 - \frac{44/45 \cdot \Delta_{SAT}}{1 + \sqrt{1 - \dfrac{(\sqrt{2} - 1) \cdot T_{sat} - \theta_{R_{eff}}}{T_{sat} - \theta_{R_{eff}}} \cdot \Delta_{SAT}{}^2}} \right] \tag{15.234}$$

$$V_{Dsat} = \begin{cases} V_{limit} & \text{for: } V_{GB}^* \le 0 \\ V_{limit} + \text{hyp}_1\{V_{DSAT_{short}} - V_{limit}, \varepsilon_2\} & \text{for: } V_{GB}^* > 0 \end{cases} \tag{15.235}$$

$$V_{DS_x} = \frac{V_{DS}}{[1 + (V_{DS}/V_{DSAT})^{2 \cdot m}]^{\frac{1}{2 \cdot m}}} \tag{15.236}$$

$$V_{DB_t} = V_{DS_x} + \phi_{B_T} \tag{15.237}$$

Surface Potential

The surface potential ψ_s is given by the following implicit relation:

$$F\{\psi_s,\phi\} = -V_{ox}\{\psi_s\}^2 + k_0{}^2 \cdot d\{\psi_s,\phi\} = 0 \tag{15.238}$$

where ϕ can be either V_{SB_i} or V_{DB_i}, and:

$$V^*_{GC}\{\psi_s\} = V^*_{GB} - \psi_s \tag{15.239}$$

$$c\{\psi_s\} = \frac{1}{2} + \frac{1}{2} \cdot \sqrt{1 + 4/k_p^2 \cdot hyp_1\{V^*_{GC}\{\psi_s\},\varepsilon_1\}} \tag{15.240}$$

$$V_{ox}\{\psi_s\} = \frac{V^*_{GC}\{\psi_s\}}{c\{\psi_s\}} \tag{15.241}$$

$$\begin{aligned} d\{\psi_s,\phi\} = {} & \psi_s + \phi_T \cdot \left[\exp\left(-\frac{\psi_s}{\phi_T}\right) - 1\right] \\ & + \phi_T \cdot \exp\left(-\frac{\phi}{m_{\phi_T}}\right) \cdot \left[\exp\left(\frac{\psi_s}{m_{\phi_T}}\right) - \frac{\psi_s}{m_{\phi_T}} - 1\right] \end{aligned} \tag{15.242}$$

The surface potential is iteratively calculated using a second-order Newton Raphson procedure, where the surface potential ψ_{i+1} in the $i + 1^{\text{th}}$ iteration is given in terms of the surface potential ψ_i in the i^{th} iteration by:

$$\psi_{i+1} = \psi_i - \frac{F_i}{F'_i - \frac{1}{2} \cdot F_i \cdot F''_i / F'_i} \tag{15.243}$$

where:

$$F_i = F\{\psi_i,\phi\} = -V_{ox}\{\psi_i\}^2 + k_0{}^2 \cdot d\{\psi_i,\phi\} \tag{15.244}$$

$$F'_i = \left.\frac{\partial F\{\psi_i,\phi\}}{\partial \psi_s}\right|_{\psi_s=\psi_i} = -2 \cdot V_{ox}\{\psi_i\} \cdot V'_{ox}\{\psi_i\} + k_0{}^2 \cdot d'\{\psi_i,\phi\} \tag{15.245}$$

$$F''_i = \left.\frac{\partial^2 F\{\psi_i,\phi\}}{\partial \psi_s^2}\right|_{\psi_s=\psi_i} = -2 \cdot V'_{ox}\{\psi_i\}^2 - 2 \cdot V_{ox}\{\psi_i\} \cdot V''_{ox}\{\psi_i\} + k_0{}^2 \cdot d''\{\psi_i,\phi\} \tag{15.246}$$

The first-order and second-order derivatives are given by:

$$c'\{\psi_s\} = \frac{\partial c\{\psi_s\}}{\partial \psi_s} = -\frac{1}{4} \cdot \frac{4/k_p{}^2}{2 \cdot c\{\psi_s\} - 1} \cdot \frac{\partial hyp_1\{V^*_{GC}\{\psi_s\},\varepsilon_1\}}{\partial V^*_{GC}} \tag{15.247}$$

$$c''\{\psi_s\} = \frac{\partial^2 c\{\psi_s\}}{\partial \psi_s^2} = -\frac{2 \cdot c'\{\psi_s\}^2 - \frac{1}{k_p{}^2} \cdot \frac{\partial^2 hyp_1\{V^*_{GC}\{\psi_s\},\varepsilon_1\}}{\partial V^*_{GC}{}^2}}{2 \cdot c\{\psi_s\} - 1} \tag{15.248}$$

$$V'_{ox}\{\psi_s\} = \frac{\partial V_{ox}\{\psi_s\}}{\partial \psi_s} = -\frac{1 + V_{ox}\{\psi_s\} \cdot c'\{\psi_s\}}{c\{\psi_s\}} \tag{15.249}$$

$$V''_{ox}\{\psi_s\} = \frac{\partial^2 V_{ox}\{\psi_s\}}{\partial \psi_s^2} = -\frac{2 \cdot c'\{\psi_s\} \cdot V'_{ox}\{\psi_s\} + V_{ox}\{\psi_s\} \cdot c''\{\psi_s\}}{c\{\psi_s\}} \tag{15.250}$$

$$d'\{\psi_s,\phi\} = \frac{\partial d\{\psi_s,\phi\}}{\partial \psi_s} = 1 - \exp\left(-\frac{\psi_s}{\phi_T}\right) + \frac{\phi_T}{m_{\phi_T}} \cdot \exp\left(-\frac{\phi}{m_{\phi_T}}\right) \cdot \left[\exp\left(\frac{\psi_s}{m_{\phi_T}}\right) - 1\right] \quad (15.251)$$

$$d''\{\psi_s,\phi\} = \frac{\partial^2 d\{\psi_s,\phi\}}{\partial {\psi_s}^2} = \frac{\exp\left(-\frac{\psi_s}{\phi_T}\right)}{\phi_T} + \frac{\phi_T}{m_{\phi_T}} \cdot \frac{\exp\left(\frac{\psi_s - \phi}{m_{\phi_T}}\right)}{m_{\phi_T}} \quad (15.252)$$

The iterative loop is performed until $\left|\psi_{i+1} - \psi_i\right| < 10^{-10} \cdot \phi_T$, at which point ψ_s is taken to be equal to ψ_{i+1}. As a zero-order starting value ψ_0, the following approximation is used:

$$
\begin{cases}
\text{if } V_{GB}^{*} \geq \phi_T \begin{cases}
\psi_{sat} = \left(\dfrac{\sqrt{P_D \cdot (V_{GB}^{*} - \phi_T) + k_0^{\,2}/4} - k_0/2}{P_D} \right)^2 + \phi_T \\
\text{if } \psi_{sat} \leq \phi \{ \psi_0 = \psi_{sat} \\
\text{if } \psi_{sat} > \phi \begin{cases}
V_{ox} = \dfrac{2 \cdot [V_{GB}^{*} - \phi]}{1 + \sqrt{1 + 4/k_p^{\,2} \cdot [V_{GB}^{*} - \phi]}} \\
x = k_0^{\,2} \cdot max(V_{ox}^{\,2}/k_0^{\,2} - \phi + \phi_T, \phi_T) \\
y = k_0^{\,2} + \dfrac{2 \cdot V_{ox}}{\sqrt{1 + 4/k_p^{\,2} \cdot [V_{GB}^{*} - \phi]}} \\
z = 1 + 4/k_p^{\,2} \cdot (V_{GB}^{*} - \phi) \\
\psi_0 = \phi + \dfrac{2 \cdot m_{\phi_T} \cdot x \cdot ln\left(\dfrac{x}{\phi_T \cdot k_0^{\,2}} \right)}{x + m_{\phi_T} \cdot y + \sqrt{(x + m_{\phi_T} \cdot y)^2 - m_{\phi_T}^{\,2} \cdot (x/z - y^2/2) \cdot ln\left(\dfrac{x}{\phi_T \cdot k_0^{\,2}} \right)}}
\end{cases}
\end{cases} \\
\text{if } V_{GB}^{*} < \phi_T \begin{cases}
\text{if } V_{GB}^{*} \geq 0 \{ \psi_0 = 0 \\
\text{if } V_{GB}^{*} < 0 \begin{cases}
x = V_{GB}^{*\,2} + \phi_T \cdot k_0^{\,2} \\
y = k_0^{\,2} + 2 \cdot V_{GB}^{*} \\
\psi_0 = -\dfrac{2 \cdot \phi_T \cdot x \cdot ln\left(\dfrac{x}{\phi_T \cdot k_0^{\,2}} \right)}{x - \phi_T \cdot y + \sqrt{(x - \phi_T \cdot y)^2 - \phi_T^{\,2} \cdot (x - y^2/2) \cdot ln\left(\dfrac{x}{\phi_T \cdot k_0^{\,2}} \right)}}
\end{cases}
\end{cases}
\end{cases}
$$

(15.253)

When $V_{GB}^{*} = 0$, the starting value ψ_0 is equal to zero. No iterative solution is necessary, and ψ_s is automatically taken to be equal to zero. Surface potentials at source and drain are now calculated from the following implicit relations:

$$F\{\psi_{s_0}, V_{SB_t}\} = 0 \tag{15.254}$$

$$F\{\psi_{s_L}, V_{DB_t}\} = 0 \tag{15.255}$$

Auxiliary Variables:

$$\Delta\psi = \psi_{s_L} - \psi_{s_0} \tag{15.256}$$

$$\overline{\psi} = \frac{\psi_{s_L} + \psi_{s_0}}{2} \tag{15.257}$$

Inversion-Layer Charge ($Q_{inv} = -\varepsilon_{ox}/t_{ox} \cdot V_{inv}$):

$$V_{inv}\{\psi_s, \phi\} = \begin{cases} 0 & \text{for: } V^*_{GB} - \psi_s \le 0 \\ \dfrac{k_0 \cdot \phi_T \cdot \exp(-\phi/m_{\phi_T}) \cdot [\exp(\psi_s/m_{\phi_T}) - \psi_s/m_{\phi_T} - 1]}{\sqrt{d\{\phi, \psi_s\}} + \sqrt{\psi_s + \phi_T \cdot [\exp(-\psi_s/\phi_T) - 1]}} & \text{for: } V^*_{GB} - \psi_s > 0 \end{cases} \tag{15.258}$$

$$V_{inv_0} = V_{inv}\{\psi_{s_0}, V_{SB_t}\} \tag{15.259}$$

$$V_{inv_L} = V_{inv}\{\psi_{s_L}, V_{DB_t}\} \tag{15.260}$$

$$\overline{V}_{inv} = \frac{V_{inv_0} + V_{inv_L}}{2} \tag{15.261}$$

$$\overline{V}_{OX} = \frac{V_{ox}\{\psi_{s_0}\} + V_{ox}\{\psi_{s_L}\}}{2} \tag{15.262}$$

$$\overline{V}_{dep} = \overline{V}_{ox} - \overline{V}_{inv} \tag{15.263}$$

$$V_{eff} = \overline{V}_{inv} + \eta_{mob_T} \cdot (\overline{V}_{ox} - \overline{V}_{inv}) \tag{15.264}$$

$$\xi_{ox}(\psi_s) = -\phi_T \cdot V'_{ox}\{\psi_s\} \tag{15.265}$$

$$\bar{\xi}_{ox} = -\phi_T \cdot \frac{V'_{ox}\{\psi_{s_0}\} + V'_{ox}\{\psi_{s_L}\}}{2} \tag{15.266}$$

$$\xi\{\psi_s\} = \begin{cases} \xi_{ox}\{\psi_s\} + \phi_T \cdot \left[\frac{1}{Acc} - 1\right] & \text{for: } V^*_{GB} - \psi_s \le 0 \\ \xi_{ox}\{\psi_s\} + \phi_T \cdot \frac{k_0 \cdot [1 - \exp(-\psi_s/\phi_T)]}{2 \cdot \sqrt{\psi_s + \phi_T \cdot [\exp(-\psi_s/\phi_T) - 1]}} & \text{for: } V^*_{GB} - \psi_s > 0 \end{cases} \tag{15.267}$$

$$\bar{\xi} = \frac{\xi\{\psi_{s_0}\} + \xi\{\psi_{s_L}\}}{2} \tag{15.268}$$

$$\overline{V}^*_{inv} = \overline{V}_{inv} + (1 + m_0) \cdot \bar{\xi} \tag{15.269}$$

Second-Order Effects

The expressions related to the second-order effects (15.270) - (15.278) are only calculated for $V^*_{GB} - \overline{\psi} > 0$:

Mobility Degradation:

$$G_{mob} = \frac{\mu_0}{\mu} = \begin{cases} 1 + \left[(\theta_{ph_T} \cdot V_{eff})^{\nu_T/3} + (\theta_{sr_T} \cdot V_{eff})^{2 \cdot \nu_T} \right]^{1/\nu_T} + C_{s_T} \cdot \left(\dfrac{\overline{V}_{dep}}{\overline{V}_{dep} + \overline{V}_{inv} + \varepsilon_4} \right)^2 & \text{for NMOS} \\ 1 + \left[(\theta_{ph_T} \cdot V_{eff})^{\nu_T/3} + (\theta_{sr_T} \cdot V_{eff})^{\nu_T} \right]^{1/\nu_T} + C_{s_T} \cdot \left(\dfrac{\overline{V}_{dep}}{\overline{V}_{dep} + \overline{V}_{inv} + \varepsilon_4} \right)^2 & \text{for PMOS} \end{cases}$$

(15.270)

Channel Length Modulation:

$$\frac{\Delta L}{L} = \alpha \cdot ln \left[\frac{V_{DS} - V_{DS_x} + \sqrt{(V_{DS} - V_{DS_x})^2 + V_p^2}}{V_P} \right] \tag{15.271}$$

$$G_{\Delta L} = \frac{1}{1 + (\Delta L / L) + (\Delta L / L)^2} \tag{15.272}$$

Velocity Saturation:

$$x_{sat} = \begin{cases} \dfrac{\theta_{sat_T} \cdot \Delta\psi}{G_{mob}} & \text{for NMOS} \\ \dfrac{\theta_{sat_T}}{G_{mob}} \cdot \dfrac{\Delta\psi}{[1 + (\theta_{sat_T} \cdot \Delta\psi / G_{mob})^2]^{1/4}} & \text{for PMOS} \end{cases} \tag{15.273}$$

$$G_{vsat} = \frac{G_{mob}}{2} \cdot [1 + \sqrt{1 + 2 \cdot x_{sat}^2}] \tag{15.274}$$

Series Resistance and Self-Heating:

$$G_R = \theta_{R_T} \cdot \left(1 + \frac{\theta_{R1}}{\theta_{R2} + \overline{V}_{inv}} \right) \cdot \overline{V}^*_{inv} \tag{15.275}$$

$$G_{Th} = \theta_{Th_T} \cdot V_{DS} \cdot \Delta\psi \cdot \overline{V}^*_{inv} \tag{15.276}$$

$$G^*_{tot} = G_{vsat} \cdot G_{\Delta L} + G_R \tag{15.277}$$

$$G_{tot} = G_{Th} + \frac{G^*_{tot}}{2} + \sqrt{\mathrm{hyp}_1 \left\{ \frac{G^{*2}_{tot}}{4} - \frac{G_R}{G_{mob}} \cdot \frac{x^2_{sat}}{\sqrt{1 + 2 \cdot x^2_{sat}}}, \varepsilon_3 \right\}} \tag{15.278}$$

Drain-Source Channel Current:

Equations (15.279) - (15.280) are only calculated for $V^*_{GB} - \overline{\psi} > 0$:

$$I_{drift} = \beta_T \cdot \overline{V}_{inv} \cdot \Delta\psi \tag{15.279}$$

$$I_{diff} = \beta_T \cdot m_{\phi_T} \cdot (V_{inv_0} - V_{inv_L}) \tag{15.280}$$

$$I_{DS} = \begin{cases} 0 & \text{for: } V^*_{GB} - \overline{\psi} \le 0 \\ \dfrac{I_{drift} + I_{diff}}{G_{tot}} & \text{for: } V^*_{GB} - \overline{\psi} > 0 \end{cases} \tag{15.281}$$

Weak-Avalanche:

$$I_{avl} = \begin{cases} 0 & for: V_{DS} - a_3 \cdot V_{DSAT} \le -a_2/A \\ a_{1_T} \cdot I_{DS} \cdot \exp\left(-\dfrac{a_2}{V_{DS} - a_3 \cdot V_{DSAT}}\right) & for: V_{DS} - a_3 \cdot V_{DSAT} > -a_2/A \end{cases} \quad (15.282)$$

Surface Potential in Gate Overlap Regions:

The surface potential in the overlap region ψ_{ov} is given by the following implicit relation:

$$F_{ov}\{V_{GX}, \psi_{ov}\} = -V_{ov}\{V_{GX}, \psi_{ov}\}^2 + k_{ov}^2 \cdot d_{ov}\{\psi_{ov}\} = 0 \quad (15.283)$$

where:

$$V_{GX}^*\{V_{GX}, \psi_{ov}\} = V_{GX} - V_{FBov} - \psi_{ov} \quad (15.284)$$

$$c_{ov}\{V_{GX}, \psi_{ov}\} = \frac{1}{2} + \frac{1}{2} \cdot \sqrt{1 + 4/k_p^2 \cdot hyp_1\{V_{GX}^*\{V_{GX}, \psi_{ov}\}, \varepsilon_1\}} \quad (15.285)$$

$$V_{ov}\{V_{GX}, \psi_{ov}\} = \frac{V_{GX}^*\{V_{GX}, \psi_{ov}\}}{c\{V_{GX}, \psi_{ov}\}} \quad (15.286)$$

$$d_{ov}\{\psi_{ov}\} = -\psi_{ov} + \phi_T \cdot \left[\exp\left(\frac{\psi_{ov}}{\phi_T}\right) - 1\right] \quad (15.287)$$

The surface potential is iteratively calculated using a second-order Newton Taphson procedure, where the surface potential ψ_{i+1} in the $i + 1^{th}$ iteration is given in terms of the surface potential ψ_i in the i^{th} iteration by:

$$\psi_{i+1} = \psi_i - \frac{F_{ov_i}}{F'_{ov_i} - \frac{1}{2} \cdot F_{ov_i} \cdot F''_{ov_i} / F'_{ov_i}} \tag{15.288}$$

where:

$$F_{ov_i} = F_{ov}\{V_{GX}, \psi_i\} = -V_{ov}\{V_{GX}, \psi_i\}^2 + k_{ov}{}^2 \cdot d_{ov}\{\psi_i\} \tag{15.289}$$

$$F'_{ov_i} = \left.\frac{\partial F_{ov}\{V_{GX}, \psi_{ov}\}}{\partial \psi_{ov}}\right|_{\psi_{ov} = \psi_i} = -2 \cdot V_{ov}\{V_{GX}, \psi_i\} \cdot V'_{ov}\{V_{GX}, \psi_i\} + k_{ov}{}^2 \cdot d'_{ov}\{\psi_i\} \tag{15.290}$$

$$F''_{ov_i} = \left.\frac{\partial^2 F_{ov}\{V_{GX}, \psi_{ov}\}}{\partial \psi_{ov}{}^2}\right|_{\psi_{ov} = \psi_i} \tag{15.291}$$

$$= -2 \cdot V'_{ov}\{V_{GX}, \psi_i\}^2 - 2 \cdot V_{ov}\{V_{GX}, \psi_i\} \cdot V''_{ov}\{V_{GX}, \psi_i\} + k_{ov}{}^2 \cdot d'_{ov}\{\psi_i\} \tag{15.292}$$

The first-order and second-order derivatives are given by:

$$\begin{aligned} c'_{ov}\{V_{GX}, \psi_{ov}\} &= \frac{\partial c_{ov}\{V_{GX}, \psi_{ov}\}}{\partial \psi_{ov}} \\ &= -\frac{1}{4} \cdot \frac{4 / k_p{}^2}{2 \cdot c_{ov}\{V_{GX}, \psi_{ov}\} - 1} \cdot \frac{\partial hyp_1\{V^*_{GX}\{V_{GX}, \psi_{ov}\}, \varepsilon_1\}}{\partial V^*_{GX}} \end{aligned} \tag{15.293}$$

$$\begin{aligned} c''_{ov}\{V_{GX}, \psi_{ov}\} &= \frac{\partial^2 c_{ov}\{V_{GX}, \psi_{ov}\}}{\partial \psi_{ov}{}^2} \\ &= -\frac{2 \cdot c'_{ov}\{V_{GX}, \psi_{ov}\}^2 - \frac{1}{k_p{}^2} \cdot \frac{\partial^2 hyp_1\{V^*_{GX}\{V_{GX}, \psi_{ov}\}, \varepsilon_1\}}{\partial V^*_{GX}}}{2 \cdot c_{ov}\{V_{GX}, \psi_{ov}\} - 1} \end{aligned} \tag{15.294}$$

$$V'_{ov}\{V_{GX},\psi_{ov}\} = \frac{\partial V_{ov}\{V_{GX},\psi_{ov}\}}{\partial \psi_{ov}} = -\frac{1 + V_{ov}\{V_{GX},\psi_{ov}\} \cdot c'_{ov}\{V_{GX},\psi_{ov}\}}{c_{ov}\{V_{GX},\psi_{ov}\}} \tag{15.295}$$

$$V''_{ov}\{V_{GX},\psi_{ov}\} = \frac{\partial^2 V_{ov}\{V_{GX},\psi_{ov}\}}{\partial \psi_{ov}^{\,2}} = -\frac{2 \cdot c'_{ov}\{V_{GX},\psi_{ov}\} \cdot V'_{ov}\{V_{GX},\psi_{ov}\} + V_{ov}\{V_{GX},\psi_{ov}\} \cdot c'_{ov}\{V_{GX},\psi_{ov}\}}{c_{ov}\{V_{GX},\psi_{ov}\}} \tag{15.296}$$

$$d'_{ov}\{\psi_{ov}\} = \frac{\partial d_{ov}\{\psi_{ov}\}}{\partial \psi_{ov}} = -1 + \exp\left(\frac{\psi_{ov}}{\phi_T}\right) \tag{15.297}$$

$$d''_{ov}\{\psi_{ov}\} = \frac{\partial^2 d_{ov}\{\psi_{ov}\}}{\partial \psi_{ov}^{\,2}} = \frac{\exp\left(\frac{\psi_{ov}}{\phi_T}\right)}{\phi_T} \tag{15.298}$$

The iterative loop is performed until $\left|\psi_{i+1} - \psi_i\right| < 10^{-8} \cdot \phi_T$, at which point ψ_{ov} is taken to be equal to ψ_{i+1}. As a zero-order starting value ψ_0, the following approximation is used:

$$
\begin{cases}
\text{if } V_{GX} \le V_{FBov} \begin{cases}
x = Acc_{ov} \cdot (V_{GX} - V_{FBov}) / \phi_T \\
\Delta_{acc} = \begin{cases} -\phi_T & \text{for: } x \le -2 \\ \phi_T \cdot [\exp(x) - 1] & \text{for: } x > -2 \end{cases} \\
\psi_0 = \left(-\sqrt{-[V_{GX} - V_{FBov}] + \Delta_{acc} + \frac{k_{ov}^2}{4}} - \frac{k_{ov}}{2} \right)^2 + \Delta_{acc}
\end{cases} \\
\text{if } V_{GX} > V_{FBov} \begin{cases}
V_{ov} = \dfrac{2 \cdot (V_{GX} - V_{FBov})}{1 + \sqrt{1 + 4/k_p^2 \cdot [V_{GX} - V_{FBov}]}} \\
x = V_{ov}^2 + \phi_T \cdot k_{0v}^2 \\
y = -k_{ov}^2 + \dfrac{2 \cdot V_{ov}}{\sqrt{1 + 4/k_p^2 \cdot [V_{GX} - V_{FBov}]}} \\
z = 1 + 4/k_p^2 \cdot (V_{GX} - V_{FBov}) \\
\psi_0 = \dfrac{2 \cdot \phi_T \cdot x \cdot ln\left(\dfrac{x}{\phi_T \cdot k_{0v}^2} \right)}{x + \phi_T \cdot y + \sqrt{(x + \phi_T \cdot y)^2 - \phi_T^2 \cdot (x/z - y^2/2) \cdot ln\left(\dfrac{x}{\phi_T \cdot k_{0v}^2} \right)}}
\end{cases}
\end{cases}
\tag{15.299}
$$

When $V_{GX} - V_{FBov} = 0$, the starting value ψ_0 is equal to zero. No iterative solution is necessary, and ψ_{ov} is automatically taken to be equal to zero. Surface potentials in the gate/source overlap ψ_{ov_0} and in the gate/drain overlap ψ_{ov_L} are calculated from the following implicit relations:

$$F_{ov}\{V_{GS}, \psi_{ov_0}\} = 0 \tag{15.300}$$

$$F_{ov}\{V_{GD} - V_{DS}, \psi_{ov_L}\} = 0 \tag{15.301}$$

The oxide voltages in the gate/source overlap ψ_{ov_0} and the gate/drain overlap ψ_{ov_L} are given by:

$$V_{ov_0} = V_{ov}\{V_{GS},\psi_{ov_0}\} \tag{15.302}$$

$$V_{ov_L} = V_{ov}\{V_{GD} - V_{DS},\psi_{ov_L}\} \tag{15.303}$$

Gate Current Equations:

The tunnelling probability is given by:

$$P_{tun}\{V_{ox},\chi_B,B\} = \begin{cases} \exp\left(-\dfrac{B}{\chi_B}\cdot\dfrac{\left[\left(\dfrac{V_{ox}}{\chi_B}\right)^2 - 3\cdot\dfrac{V_{ox}}{\chi_B} + 3\right]}{1+\left(1-\dfrac{V_{ox}}{\chi_B}\right)^{\frac{3}{2}}}\right) & V_{ox} < \chi_B \\ \exp(-B/V_{ox}) & V_{ox} \geq \chi_B \end{cases} \tag{15.304}$$

Source/Drain Gate Overlap Current:

The gate tunnelling in both gate/source and gate/drain overlap are given by:

$$P_{ov}\{V_{ov}\} = P_{tun}\{V_{ov},\chi_{B_{inv}},B_{inv}\} \tag{15.305}$$

$$I_{Gov}\{V_{GX},V_{ov}\} = I_{GOV}\cdot V_{GX}\cdot V_{ov}\cdot[P_{ov}\{V_{ov}\} - P_{ov}\{-V_{ov}\}] \tag{15.306}$$

$$I_{Gov_0} = I_{Gov}\{V_{GS}\,,\,V_{ov_0}\} \tag{15.307}$$

$$I_{Gov_L} = I_{Gov}\{V_{GS} - V_{DS}\,,\,V_{ov_L}\} \tag{15.308}$$

Intrinsic Gate-to-Bulk Current:

The gate tunnelling currnt in accumulation:

$$P_{acc} = P_{tun}\{-\overline{V}_{ov},\chi_{B_{acc}},B_{acc}\} \tag{15.309}$$

$$V_{acc} = \overline{V}_{ox} - hyp_1\{\overline{V}_{ox},\varepsilon_3\} \tag{15.310}$$

$$I_{GB} = -I_{GACC}\cdot(V_{GS}+V_{SB})\cdot V_{acc}\cdot P_{acc} \tag{15.311}$$

Intrinsic Gate-to-Channel Current:

The tunnelling current in inversion, including quantum-mechanical barrier lowering $\Delta_{\chi B}$. Equations are only calculated for $V^*_{GB}-\overline{\psi}>0$:

$$\Delta\chi_B = QM_{\psi}\cdot(\overline{V}_{inv}/3+\overline{V}_{ox}-\overline{V}_{inv})^{2/3} \tag{15.312}$$

$$\chi_{B_{eff}} = 0.7\cdot\chi_{B_{inv}} + hyp_1\{0.3\cdot\chi_{B_{inv}}-\Delta\chi_B,\varepsilon_3\} \tag{15.313}$$

$$B_{eff} = B_{inv}\cdot(\chi_{B_{eff}}/\chi_{B_{inv}})^{3/2} \tag{15.314}$$

$$P_{inv} = P_{tun}\{\overline{V}_{ox},\chi_{B_{eff}},B_{eff}\} \tag{15.315}$$

$$r_B = \frac{3}{8}\cdot\frac{B_{eff}}{\chi^2_{B_{eff}}}\cdot\frac{\overline{\xi}_{ox}}{\phi_T} \tag{15.316}$$

$$r^* = \frac{\overline{\xi}}{\phi_T\cdot\overline{V}^*_{inv}} \tag{15.317}$$

$$r_{ox} = \frac{\bar{\xi}_{ox}}{\phi_T \cdot \bar{V}_{ox}} \tag{15.318}$$

$$P_{GC} = 1 + \frac{r_B{}^2 + 4 \cdot r_B \cdot r^* + 2 \cdot r_B \cdot r_{ox} + 2 \cdot r^{*2} + 4 \cdot r_{ox} \cdot r^*}{24} \cdot \Delta\psi^2 \tag{15.319}$$

$$\bar{I}_{GC} = I_{GINV} \cdot G_{\Delta L} \cdot \left(V_{GS} - \frac{1}{2} V_{DS_x} \right) \cdot P_{inv} \tag{15.320}$$

The total intrinsic gate current I_{GC}:

$$I_{GC} = \bar{I}_{GC} \cdot \bar{V}_{inv} \cdot P_{GC} \tag{15.321}$$

$$P_{GS} = [r_B + r_{ox}] \cdot \frac{\Delta\psi}{12} \tag{15.322}$$

$$I_{GS} = \begin{cases} I_{Gov_0} & \text{for: } V^*_{GB} - \bar{\psi} \le 0 \\ \frac{1}{2} \cdot I_{GC} + \left(P_{GS} \cdot \bar{V}_{inv} + \frac{V_{inv_0} - V_{inv_L}}{12} \right) \cdot \bar{I}_{GC} + I_{Gov_0} & \text{for: } V^*_{GB} - \bar{\psi} > 0 \end{cases} \tag{15.323}$$

$$I_{GD} = \begin{cases} I_{Gov_L} & \text{for: } V^*_{GB} - \bar{\psi} \le 0 \\ I_{GC} - I_{GS} + I_{Gov_0} + I_{Gov_L} & \text{for: } V^*_{GB} - \bar{\psi} > 0 \end{cases} \tag{15.324}$$

Gate-Induced Drain/Source Leakage Current:

$$V_{tov}\{V_{ov}, V\} = \sqrt{(V_{ov} - hyp_1\{V_{ov}, \varepsilon_3\})^2 + C^2_{GIDL} \cdot V^2} \tag{15.325}$$

$$I_{gixl}\{V_{ov},V\}= \begin{cases} A_{GIDL}\cdot V\cdot V_{tov}\{V_{ov},V\}^2\cdot \exp-\left(\frac{B_{GIDL_T}}{V_{tov}\{V_{ov},V\}}\right) & \text{for: } V_{tov}\{V_{ov},V\} > -\frac{B_{GIDL_T}}{A} \\ 0 & \text{for: } V_{tov}\{V_{ov},V\} \le -\frac{B_{GIDL_T}}{A} \end{cases}$$

(15.326)

$$I_{gisl}= I_{gixl}\{V_{ov_0},V_{SB}\} \tag{15.327}$$

$$I_{gidl}= I_{gixl}\{V_{ov_L},V_{DS} + V_{SB}\} \tag{15.328}$$

Extended Charge Equations

Bias-Dependent Overlap Capacitance:

$$Q_{ov_0} = C_{GSO}\cdot V_{ov_0} \tag{15.329}$$

$$Q_{ov_L} = C_{GDO}\cdot V_{ov_L} \tag{15.330}$$

Intrinsic Charges:

$$C_{OX_{eff}} = \frac{C_{OX}}{1+QM_{t_{ox}}\cdot\left[\left(\frac{V_{eff}}{\eta_{mob_T}}\right)^2+(5\cdot V_{limit})^2\right]^{-1/6}} \tag{15.331}$$

$$\Delta V_{inv} = (V_{inv_0}-V_{inv_L})\cdot\left(1-\frac{G_R}{G_{tot}}\right) \tag{15.332}$$

$$F_j = \frac{1}{2}\cdot\frac{\Delta V_{inv}}{\overline{V}^*_{inv}} \tag{15.333}$$

$$Q_S = -\frac{C_{OX_{eff}} \cdot G_{\Delta L}}{2} \cdot \left[\overline{V}_{inv} + \frac{\Delta V_{inv}}{6} \cdot \left(F_j - \frac{F_j^2}{5} + 1 \right) \right] \tag{15.334}$$

$$Q_D = -\frac{C_{OX_{eff}} \cdot G_{\Delta L}}{2} \cdot \left[\overline{V}_{inv} + \frac{\Delta V_{inv}}{6} \cdot \left(F_j + \frac{F_j^2}{5} - 1 \right) \right] \tag{15.335}$$

$$Q_G = C_{OX_{eff}} \cdot \left[\overline{V}_{ox} + \frac{\Delta V_{inv}}{6} \cdot F_j \cdot \frac{\overline{\xi}_{ox}}{\overline{\xi}} \right] \tag{15.336}$$

$$Q_B = -[Q_S + Q_D + Q_G] \tag{15.337}$$

Extended Noise Equations

The noise equations (15.338) to (15.356) are only calculated for $V^*_{GB} - \overline{\psi} > 0$. In these equations *f* represents the operation frequency of the transistor.

$$G_{eff} = 1 - \frac{G_R}{G_{tot}} \tag{15.338}$$

$$x_{sat}^2 = \begin{cases} \theta_{sat_T}^2 \cdot \Delta\psi^2 \cdot {G_{eff}}^2 & \text{for NMOS} \\ \dfrac{\theta_{sat_T}^2 \cdot \Delta\psi^2 \cdot {G_{eff}}^2}{\sqrt{1 + \theta_{sat_T}^2 \cdot \Delta\psi^2 \cdot {G_{eff}}^2}} & \text{for PMOS} \end{cases} \tag{15.339}$$

$$G_{vsatR} = \frac{G_{mob} + \sqrt{G_{mob}^2 + 2 + {x_{sat}}^2}}{2} \tag{15.340}$$

$$t_1 = \frac{\overline{V}_{inv}}{\overline{V}^*_{inv}} \tag{15.341}$$

$$t_2 = \frac{F_j^2}{36} \tag{15.342}$$

$$t_{sat} = \frac{x_{sat}^{\ 2}}{G^2_{vsatR}} \tag{15.343}$$

$$g_{ideal} = \frac{\beta_T \cdot \overline{V}^*_{inv}}{G_{vsatR} \cdot G_{\Delta L}} \tag{15.344}$$

$$S_{th} = N_{T_T} \cdot G_{eff}^{\ 2} \cdot g_{ideal} \cdot max \cdot \{t_1 + 12 \cdot t_2 \cdot (1 - 2 \cdot t_{sat} - 2 \cdot t_{sat}^{\ 2}), 0\} \tag{15.345}$$

$$C_{G_{eff}} = C_{OX_{eff}} \cdot \frac{\bar{\xi}_{ox}}{\phi_T} \cdot \frac{G_{vsat_R \cdot G_{\Delta L}}}{G_{mob}} \tag{15.346}$$

$$\begin{aligned} m_{ig} = \frac{1}{g_{ideal}} \cdot \Bigg[& \frac{t_1}{12} - t_1 \cdot t_2 - \frac{t_2}{5} + 12 \cdot t_2^{\ 2} \\ & + t_{sat} \cdot \left(\frac{t_1}{12} + 3 \cdot t_1 \cdot t_2 - \frac{9 \cdot t_2}{5} - 36 \cdot t_2^{\ 2} \right) \\ & + t_{sat}^{\ 2} \cdot \left(\frac{t_1}{12} + 4 \cdot t_1 \cdot t_2 - \frac{17 \cdot t_2}{5} - 24 \cdot t_2^{\ 2} \right) \Bigg] \end{aligned} \tag{15.347}$$

$$m_{igth} = G_{eff} \cdot \sqrt{t_2} \cdot [1 - 12 \cdot t_2 + t_{sat} \cdot \left(\frac{1}{2} - t_1 + 30 \cdot t_2\right) + t_{sat}{}^2 \cdot \left(\frac{3}{8} - \frac{3 \cdot t_1}{2} + \frac{51 \cdot t_2}{2}\right)] \tag{15.348}$$

$$f_{cross} = \frac{1}{2 \cdot \pi \cdot C_{G_{eff}} \cdot m_{ig}} \tag{15.349}$$

$$S_{ig} = \frac{N_T}{m_{ig}} \cdot \frac{(f_{op}/f_{cross})^2}{1 + (f_{op}/f_{cross})^2} \tag{15.350}$$

$$S_{igid} = j \cdot \frac{N_T}{m_{ig}} \cdot m_{igid} \cdot \frac{f_{op}/f_{cross}}{\sqrt{1 + (f_{op}/f_{cross})^2}} \tag{15.351}$$

$$\textit{for GATENOISE} = 1 : \begin{cases} g_{ideal} = \dfrac{\beta_T \cdot \overline{V}_{inv}}{G_{mob} \cdot G_{\Delta L}} \\ S_{th} = N_{T_T} \cdot G_{eff}^2 \cdot g_{ideal} / \sqrt{1 + t_{sat} + t_{sat}{}^2} \\ S_{ig} = 0 \\ S_{igth} = 0 \end{cases} \tag{15.352}$$

$$N_0 = \frac{\varepsilon_{ox}}{q \cdot t_{ox}} \cdot \left(\overline{V}_{inv} + \frac{\Delta V_{inv}}{2}\right) \tag{15.353}$$

$$N_L = \frac{\varepsilon_{ox}}{q \cdot t_{ox}} \cdot \left(\overline{V}_{inv} - \frac{\Delta V_{inv}}{2} \right) \tag{15.354}$$

$$N^* = \frac{\varepsilon_{ox}}{q \cdot t_{ox}} \cdot \bar{\xi} \tag{15.355}$$

$$\begin{aligned} S_{fl} = {} & \frac{q \cdot \phi_T{}^2 \cdot t_{ox} \cdot \beta_T \cdot I_{DS}}{f \cdot \varepsilon_{ox} \cdot G_{vsat} \cdot N^*} \cdot \left[(N_{FA} - N^* \cdot N_{FB} + N^{*2} \cdot N_{FC}) \cdot \ln\left(\frac{N_0 + N^*}{N_L + N^*} \right) \right. \\ & \left. + (N_{FB} - N^* \cdot N_{FC}) \cdot (N_0 - N_L) + \frac{N_{FC}}{2} \cdot (N_0{}^2 - N_L{}^2) \right] \\ & + \frac{\phi_T \cdot I_{DS}{}^2}{f} \cdot (1 - G_{\Delta L}) \cdot \left[\frac{N_{FA} + N_{FB} \cdot N_L + N_{FC} \cdot N_L{}^2}{(N_L + N^*)^2} \right] \end{aligned} \tag{15.356}$$

15.5.2 Parasitic Resistance

MOS Model 11 contains one parasitic element, the gate resistance. The gate resistance is scaled with the geometry, facilitating the implementation of multi-finger devices.

$$W_f = \frac{W}{NF} \tag{15.357}$$

$$W_{E,f} = W_f + \Delta W_{OD} \tag{15.358}$$

$$L_f = L + \Delta L_{PS} \tag{15.359}$$

$$L_{sil,\,f} \;=\; L_f + DLSIL \tag{15.360}$$

$$X_{GWE} \;=\; XGW - 0.5 \cdot \Delta W_{OD} \tag{15.361}$$

$$RG \;=\; \frac{RGO}{N_{MULT}} + \frac{1}{NF \cdot N_{MULT}} \cdot \left(\frac{RSHG \cdot \left(\frac{W_{E,\,f}}{3 \cdot NGCON} + X_{GWE} \right)}{NGCON \cdot L_{sil,\,f}} + \frac{RINT + RVPOLY}{W_{E,\,f} \cdot L_f} \right) \tag{15.362}$$

Note that if the values L_f, W_f, $L_{sil,\,f}$ or $XGWE$ are smaller than 1e-9, they will be clipped to 1e-9.

$NGCON$ is rounded of to an integer number (1 or 2).

15.5.3 Numerical Adaptation

The implemented electrical equations of MOS Model 11 are essentially based on the physical description given in Section 15.2. The following numerical adaptations have been made in order to obtain smooth transitions and prevent numerical problems, leading to the equations given in the section titled *Extended Equations on page 126*15.5.115.5.115.5.1:

- The piece-wise eqs. (15.20) for $V_{GB_{eff}}$, (15.23) for D_{sf}, (15.28) for $V_{DSAT_{long}}$, (15.33) for V_{DSAT} and (15.77) for I_{GB} have been replaced by smooth C_∞-continuous functions based on hyp-functions.

- Expression (15.22) describing the drain-induced barrier lowering effect has no numerical solution for $V_{SB} + \phi_{B_T} < 0$. In order to solve this problem the expression $V_{SB} + \phi_B$ is clipped at a minimum value of $0.1 \cdot \phi_{B_T}$ using Eq. (15.223). In order to maintain symmetry (with respect to source and drain) the same method must be applied to the drain side, this is done in Eq. (15.237).

- In the accumulation region (i.e., $V^*_{GB} \leq 0$), the inversion-layer charge density is equal to zero (i.e., $V_{inv_0} = V_{inv_L} = 0$), as a result the drain-source channel current I_{DS}, the weak-avalanche current I_{av1}, the gate-to-channel current I_{GC}, the total drain charge Q_D and source charge Q_S, and the noise spectral densities S_{th}, S_{fl} and S_{ig} are all equal to zero. In this case, the model equations can be simplified and only certain equations need to be calculated. The equations that only need to be calculated in the inversion region (i.e., $V^*_{GB} > 0$) are indicated.

- For a very small positive value of ψ_s (i.e., $\psi_s < 10^{-9}$ just above $V^*_{GB} = 0$, the expression (15.40) for V_{inv} may become numerically inaccurate. In this case V_{inv} is very small and can be taken to be equal to zero, see (15.258).

- The Coulomb-scattering part of the mobility model, Eq. (15.53) is protected against zero-division by adding a small $\varepsilon_4 = 1 \cdot 10^{-14}$ to its denominator, see Eq. (15.270).

- The theoretical channel length modulation expression (15.54) can become negative for high values of α and V_{DS}. This corresponds to a negative effective channel length, which is not physical. In order to prevent $G_{\Delta L}$ from becoming negative, a second-order Taylor polynomial in $\Delta L / L$ is used in the actual implementation, see eqs. (15.271) and (15.272).

- The term in the square root of Eq. (15.59) can become negative for very high values of parameter θ_R, which would result in numerical errors. This has been prevented in the actual implementation (15.278) by using a hyp-smoothing function.

- The derivative of the weak-avalanche expression (15.63) with respect to V_{DS} may become numerically unstable for V_{DS} values just above $a_3 \cdot V_{DSAT}$. This problem has been circumvented by using (15.308), where A is a numerical constant defined in Section 15.3.1.

- The exponent in the tunnelling probability P_{tun}, given by Eq. (15.71), results in zero divided by zero for $V_{ox} = 0$. By simply rewriting the exponent, this problem can be circumvented as has been done in Eq. (15.315).

- For very high gate bias values, which could occur during the iteration process of the circuit simulator, the expression of effective oxide barrier $\chi_{B_{eff}}$, given by Eq. (15.79), can become zero or negative resulting in numerical errors. In order to prevent this problem $\chi_{B_{eff}}$

is clipped at a minimum (arbitrary) value of $0.7 \cdot \chi_{B_{inv}}$ using a hyp-smoothing function, see Eq. (15.333).

- Gate-induced drain (or source) leakage only occurs when the oxide voltage in the drain overlap region is negative, in other words when the overlapped n^+ -drain region is depleted. For positive oxide voltage, no GIDL occurs, because, as the overlapped region is in accumulation, the band bending is minimal and as a result band-to-band tunnelling cannot occur. This is, however, not automatically accomplished using (15.112). In order to take this effect into account empirically, we replace V_{ov} in (15.111) by a smoothing function which is equal to V_{ov} for negative values of V_{ov} and equal to 0 for positive values, see (15.341).

- Similar to the weak-avalanche expression (15.63), the derivitives of the gate-induced drain leakage expression (15.112) may become numerically unstable for V_{tov} very close to 0. This problem has been circumvented in the same way as has been done for (15.308), see Eq. (15.342).

- The expression of effective oxide capacitance (15.97) due to quantum-mechanical effects gives erroneous results for $V_{eff} = 0$ (i.e., $V_{GB} = V_{FB}$). This can be prevented by replacing V_{eff}/η_{mob} by $\sqrt{(V_{eff}/\eta_{mob})^2 + (20 \cdot \phi_T)^2}$, where the value of $20 \cdot \phi_T$ is rather arbitrary but it nevertheless ensures a smooth transition from accumulation to depletion/inversion.

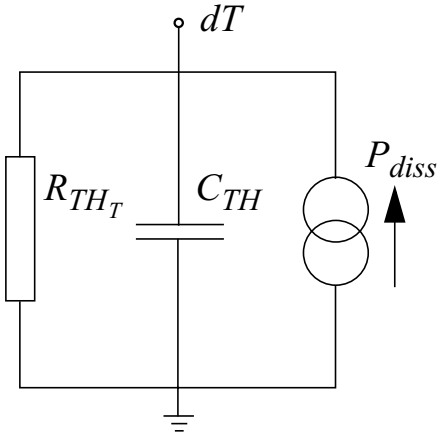
- The thermal noise spectral density S_{th} given by Eq. (15.112) can become negative for very high values of parameter θ_{sat}, which is not physical. In order to prevent this, S_{th} is clipped to zero in these cases, see Eq. (15.346).

- The spectral density of induced gate noise is given by Eq. (15.115), keeps rising infinitely for high frequencies. This is not realistic and unwanted in curcuit simulations. Therefore the induced gate noise as well as the cross-spectral density S_{igth} are limited above a cross-over frequency f_{cross}, see Eqs. (15.349), (15.350) and (15.351).

15.6 Self-heating

15.6.1 Equivalent circuit

Self-heating is part of the model. It is defined in the usual way by adding a self-heating network (see Figure 71) containing a current source describing the dissipated power and both a thermal resistance R_{TH} and a thermal capacitance C_{TH}.



Material	A_{th}
Si	1.3
Ge	1.25
GaAs	1.25
AlAs	1.37
InAs	1.1
InP	1.4
GaP	1.4
SiO_2	0.7

Figure 71: On the left, the self-heating network, where the node voltage V_{dT} is used in the temperature scaling relations. Note that for increased flexibility the node dT is available to the user. On the right are parameter values that can be used for A_{th}.

The resistance and capacitance are both connected between ground and the temperature node d_T. The value of the voltage V_{dT} at the temperature node gives the increase in local temperature, which is included in the calculation of the temperature scaling relation (15.3) and (15.206), see sections 15.2.2 and 15.4.

For the value of A_{th} we recommend using values from literature that describes the temperature scaling of the thermal conductivity. For the most important materials, the values are given in Figure 71, which is largely based on Ref. [23], see also [24].

For example, if the value of V_{dT} is 0.5V, the increase in temperature is 0.5 degrees Celsius.

The total dissipated power is a sum of the dissipated power of each branch of the equivalent circuit and is given by:

$$P_{diss} = I_D^e \cdot V_D^e + I_G^e \cdot V_G^e + I_S^e \cdot V_S^e + I_B^e \cdot V_B^e$$

$$= I_{DS}'' \cdot V_{DS}'' + I_{DB}'' \cdot (V_{DS}'' - V_{SB}'') + I_{SB}'' \cdot V_{SB}'' + I_{GS}'' \cdot V_{GS}''$$

$$+ I_{GD}'' \cdot (V_{GS}'' - V_{DS}'') + I_{GB}'' \cdot (V_{GS}'' - V_{SB}'')$$

where all variables are given in figure 72 on the previous pages. Note that only the steady-state currents contribute to the dissipated power.

The total dissipation applies for the electrical model (mnet[1], mpet[1], mos1102et[2]), geometrical binning model (mnt[1], mpt[1], mos11021t[2]), and geometrical physical model (mnt[1], mpt[1], mos11020t[2]).

Below a *Pstar* example is given to illustrate how self-heating works.

q Example

Title: example self-heating 1102;

```
circuit;
mnet_1(Vd, Vg, Vs, 0, dt) level=1102, Rth=1e4,Cth=1e-9;
R_1 ( Vdd, Vd) 100;
R_2 ( Vgg, Vg) 1k;
R_3 ( Vs, 0) 100;
e_SRC_2 (Vgg ,net101) 5;
e_SRC_1 ( Vdd, 0) 1;
e_SRC_3 ( net101, 0) 0;
end;

dc;
print: vn(dt), op(pdiss.mnet_1);
end; run;

result:
DC   Analysis.
VN(dt)        =9.533E+00
Pdiss.MNT_1   =953.327E-6
```

1. *Pstar* model name.
2. *Spectre*/*ADS* model name.

The voltage on node *dt* is 9.533E+00 V, which means that the local temperature is increased by 9.533E+00 ^{o}C.

15.7 DC Operating point output

15.7.1 DC operating point output

The DC operating point output facility gives information on the state of a device at its operation point. Besides terminal currents and voltages, the magnitudes of linearized internal elements are given. In some cases, meaningful quantities can be derived which are then also given (e.g. f_T). The objective of the DC operating-facility is twofold:

- Calculate small-signal equivalent circuit element values.
- Open a window on the internal bias conditions of the device and its basic capabilities.

Below, the printed items are described. $C_{x(y)}$ indicates the derivate of the charge Q at terminal x to the voltage at terminal y, when all other terminals remain constant.

No.	Symbol	Program Name	Units	Description
0	I_{DS}	IDS	A	Drain current, excl. avalanche and tunnel currents.
1	I_{avl}	IAVL	A	Substrate current due to weak-avalanche
2	I_{GS}	IGS	A	Gate-to-source current due to direct tunnelling
3	I_{GD}	IGD	A	Gate-to-drain current due to direct tunnelling
4	I_{GB}	IGB	A	Gate-to-bulk current due to direct tunnelling
5	V_{DS}	VDS	V	Drain-Source voltage
6	V_{GS}	VGS	V	Gate-Source voltage
7	V_{SB}	VSB	V	Source-Bulk voltage
8	V_{TO}	VTO	V	Zero-bias threshold voltage: $V_{TO} = V_{FB} + P_D \cdot (\phi_B + 2 \cdot \phi_T) + k_0 \cdot \sqrt{\phi_B + 2 \cdot \phi_T}$
9	V_{TS}	VTS	V	Threshold voltage including back-bias effects: $V_{TS} = V_{FB} + P_D \cdot (V_{SB_t} + 2 \cdot \phi_T) - (V_{SB_t} - \phi_B) + k_0 \cdot \sqrt{V_{SB_t} + 2 \cdot \phi_T}$

No.	Symbol	Program Name	Units	Description
10	V_{TH}	VTH	V	Threshold voltage including back-bias and drain-bias effects: $V_{TH} = V_{FB} + P_D \cdot (V_{SB_t} + 2 \cdot \phi_T) - (V_{SB_t} - \phi_B) + k_0 \cdot \sqrt{V_{SB_t} + 2 \cdot \phi_T} - \Delta V_G$
11	V_{GT}	VGT	V	Effective gate drive including back-bias and drain voltage effects: $V_{GT} = V_{inv_0}$
12	V_{DSAT}	VDSS	V	Drain saturation voltage at actual bias
13	$V_{DS_{eff}}$	VSAT	V	Saturation limit: $V_{DS_{eff}} = V_{DS} - V_{DSAT}$
14	g_m	GM	A/V	Transconductance (assumed V_{DS}>0): $g_m = \partial I_{DS} / \partial V_{GS}$
15	g_{mb}	GMB	A/V	Substrate-transconductance (assumed V_{DS}>0): $g_{mb} = \partial I_{DS} / \partial V_{BS}$
16	g_{ds}	GDS	A/V	Output conductance: $g_{ds} = \partial I_{DS} / \partial V_{DS}$
17	$C_{D(D)}$	CDD	F	$C_{D(D)} = \partial Q_D / \partial V_{DS}$
18	$C_{D(G)}$	CDG	F	$C_{D(G)} = -\partial Q_D / \partial V_{GS}$
19	$C_{D(S)}$	CDS	F	$C_{D(S)} = C_{D(D)} - C_{D(G)} - C_{D(B)}$
20	$C_{D(B)}$	CDB	F	$C_{D(B)} = \partial Q_D / \partial V_{SB}$
21	$C_{G(D)}$	CGD	F	$C_{G(D)} = -\partial Q_G / \partial V_{DS}$
22	$C_{G(G)}$	CGG	F	$C_{G(G)} = \partial Q_G / \partial V_{GS}$
23	$C_{D(S)}$	CGS	F	$C_{G(S)} = C_{G(G)} - C_{G(D)} - C_{G(B)}$
24	$C_{G(B)}$	CGB	F	$C_{G(B)} = \partial Q_G / \partial V_{SB}$
25	$C_{S(D)}$	CSD	F	$C_{S(D)} = -\partial Q_S / \partial V_{DS}$
26	$C_{S(G)}$	CSG	F	$C_{S(G)} = -\partial Q_S / \partial V_{GS}$

No.	Symbol	Program Name	Units	Description
27	$C_{S(S)}$	CSS	F	$C_{S(S)} = C_{S(G)} + C_{S(D)} + C_{S(B)}$
28	$C_{S(B)}$	CSB	F	$C_{S(B)} = \partial Q_S / \partial V_{SB}$
29	$C_{B(D)}$	CBD	F	$C_{B(D)} = -\partial Q_B / \partial V_{DS}$
30	$C_{B(G)}$	CBG	F	$C_{B(G)} = -\partial Q_B / \partial V_{GS}$
31	$C_{B(S)}$	CBS	F	$C_{B(S)} = C_{B(B)} - C_{B(D)} - C_{B(G)}$
32	$C_{B(B)}$	CBB	F	$C_{B(B)} = -\partial Q_B / \partial V_{SB}$
33	$C_{GD_{OV}}$	CGDOL	F	Gate-drain overlap capacitance of the actual transistor: $C_{GD_{OV}} = \partial Q_{OV_L} / \partial V_{DS}$
34	$C_{GS_{OV}}$	CGSOL	F	Gate-source overlap capacitance of the actual transistor: $C_{GS_{OV}} = \partial Q_{OV_0} / \partial V_{GS}$
35	W_E	WE	m	Effective channel width for geometrical models
36	L_E	LE	m	Effective channel length for geometrical models
37	u	U	-	Transistor gain: $u = g_m / g_{ds}$
38	R_{out}	ROUT	Ω	Small-signal output resistance: $R_{out} = 1 / g_{ds}$
39	V_{Early}	VEARLY	V	Equivalent Early voltage: $V_{Early} = \lvert I_{DS} \rvert / g_{ds}$
40	k_{eff}	KEFF	$\sqrt{V}$	Body effect parameter: $k_{eff} = k_0$
41	β_{eff}	BEFF	A/V^2	Gain factor: $2 \cdot \lvert I_{DS} \rvert / V_{inv_0}{}^2$
42	f_T	FUG	Hz	Unity gain frequency at actual bias: $f_T = \frac{g_m}{2\pi(C_{G(G)} + C_{GS_{OV}} + C_{GD_{OV}})}$
43	$\sqrt{S_{V_{Gth}}}$	SQRTSFW	$V/\sqrt{Hz}$	Input-referred RMS white noise voltage density: $\sqrt{S_{V_{Gth}}} = \sqrt{S_{th}} / g_m$

No.	Symbol	Program Name	Units	Description
44	$\sqrt{S_{V_{Gfl}}}$	SQRTSFF	$V/\sqrt{Hz}$	Input-referred RMS white noise voltage density at 1 kHz: $\sqrt{S_{V_{Gfl}}} = \sqrt{S_{fl}(1kHz)}/g_m$
45	f_{knee}	FKNEE	Hz	Cross-over frequency above which white noise is dominant: $f_{knee} = 1Hz \cdot S_{fl}(1Hz)/S_{tl}$
46	Rg	RG	Ω	Gate resistance

15.8 Embedding

15.8.1 Model embedding in a circuit simulator

In CMOS technologies both n- and p-channel MOS transistors are supported. It is convenient to use one model for both type of transistors instead of two separate models. This is accomplished by mapping a p-channel device with its bias conditions and parameter set onto an equivalent n-channel device with appropriately changed bias conditions (i.e. currents, voltages and charges) and parameters. In this way both type of transistors can be treated as an n-channel transistor. Nevertheless, the electrical behaviour of electrons and holes is not exactly the same (e.g. the mobility and tunnelling behaviour), and consequently slightly different equations have to be used in case of n- or p-type transistors, see section 15.2.3 on page 21.

As said earlier, any circuit simulator internally identifies the terminals of a MOS transistor by a number. However, designers are used to the standard terminology of source, drain, gate and bulk. Therefore, in the context of a circuit simulator it is traditionally possible to address, say, the drain of MOST number 17, even if in reality the corresponding source is at a higher potential (n-channel case). More strongly, most circuit simulators provide for model evaluation a so called V_{DS}, V_{GS} and V_{SB} based on an a priori assignment of source, drain and bulk that is independent of the actual bias conditions. Since MOS Model 1102 assumes saturation occurs at the drain side of the MOSFET, the basic model cannot cope with bias conditions that correspond to $V_{DS} < 0$. Again a transformation of the bias conditions is necessary. In this case, the transformation corresponds to internally reassigning source and drain, applying the standard electrical model, and then reassigning the currents and charges to the original terminals. In MOS Model 1102 care has been taken to preserve symmetry with respect to drain and source at $V_{DS} = 0$. In other words no non-singularities will occur in the higher-order derivatives at $V_{DS} = 0$.

In detail, in order to embed MOS Model 1102 correctly into a circuit simulator, the following procedure, illustrated in figure 72 should be followed. We have assumed that indeed the simulator provides the nodal potentials V_D^e, V_G^e, V_S^e and V_B^e based on an a priori assignment of drain, gate, source and bulk.

Step 1 Calculate the voltages V''_{DS}, V''_{GS} and V''_{SB}, and the additional voltages V''_{DG} and V''_{SG}. The latter are used for calculating the charges associated with overlap capacitances.

Step 2 Based on n- or p-channel devices, calculate the modified voltages V'_{DS}, V'_{GS} and V'_{SB}. From here onwards only n-channel behaviour needs to be considered.

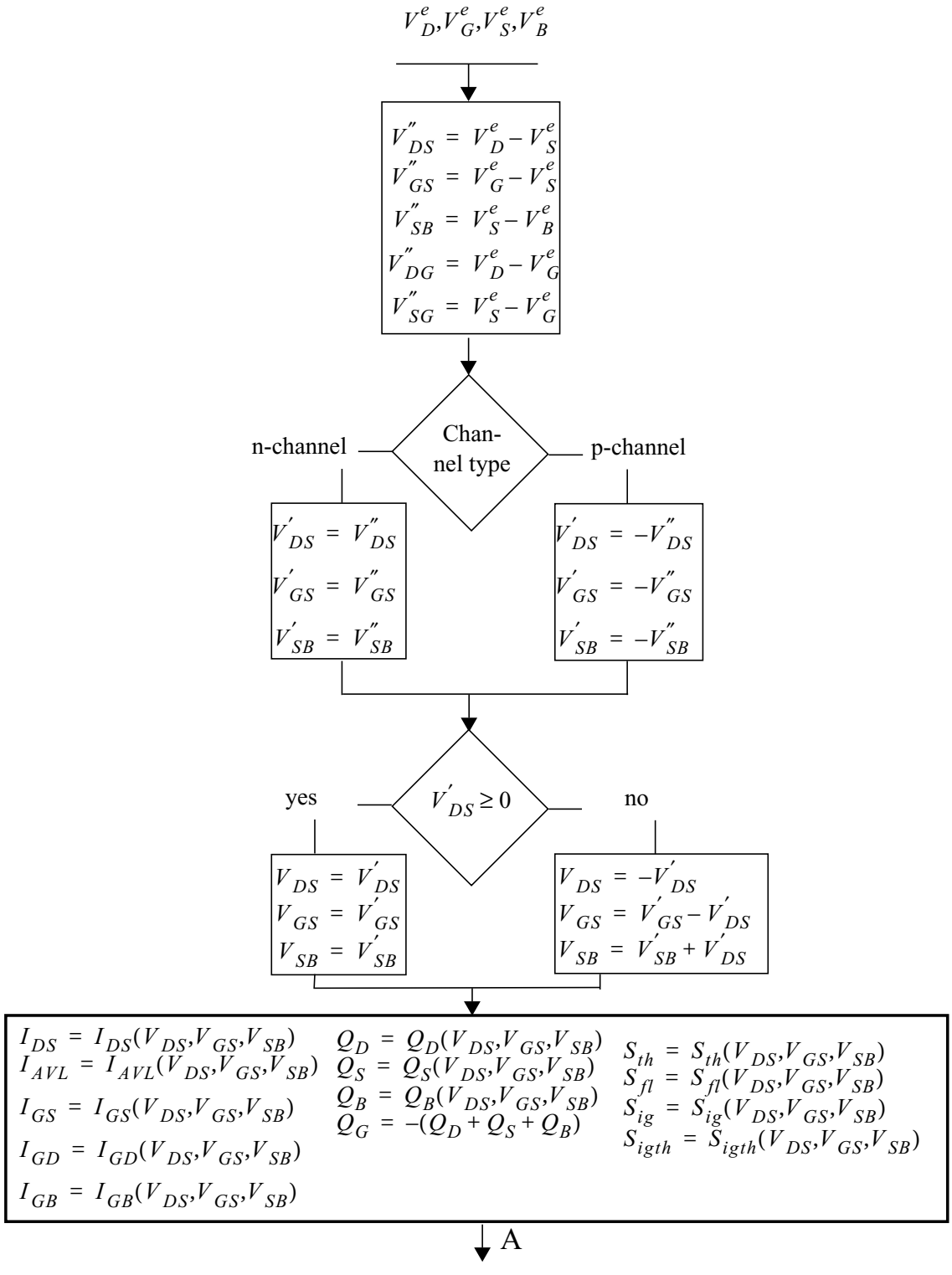
Step 3 Based on a positive or negative V'_{DS}, calculate the internal nodal voltages. At this level, the voltages - and the parameters, see below - comply to all the requirements for input quantities of MOS Model 1102.

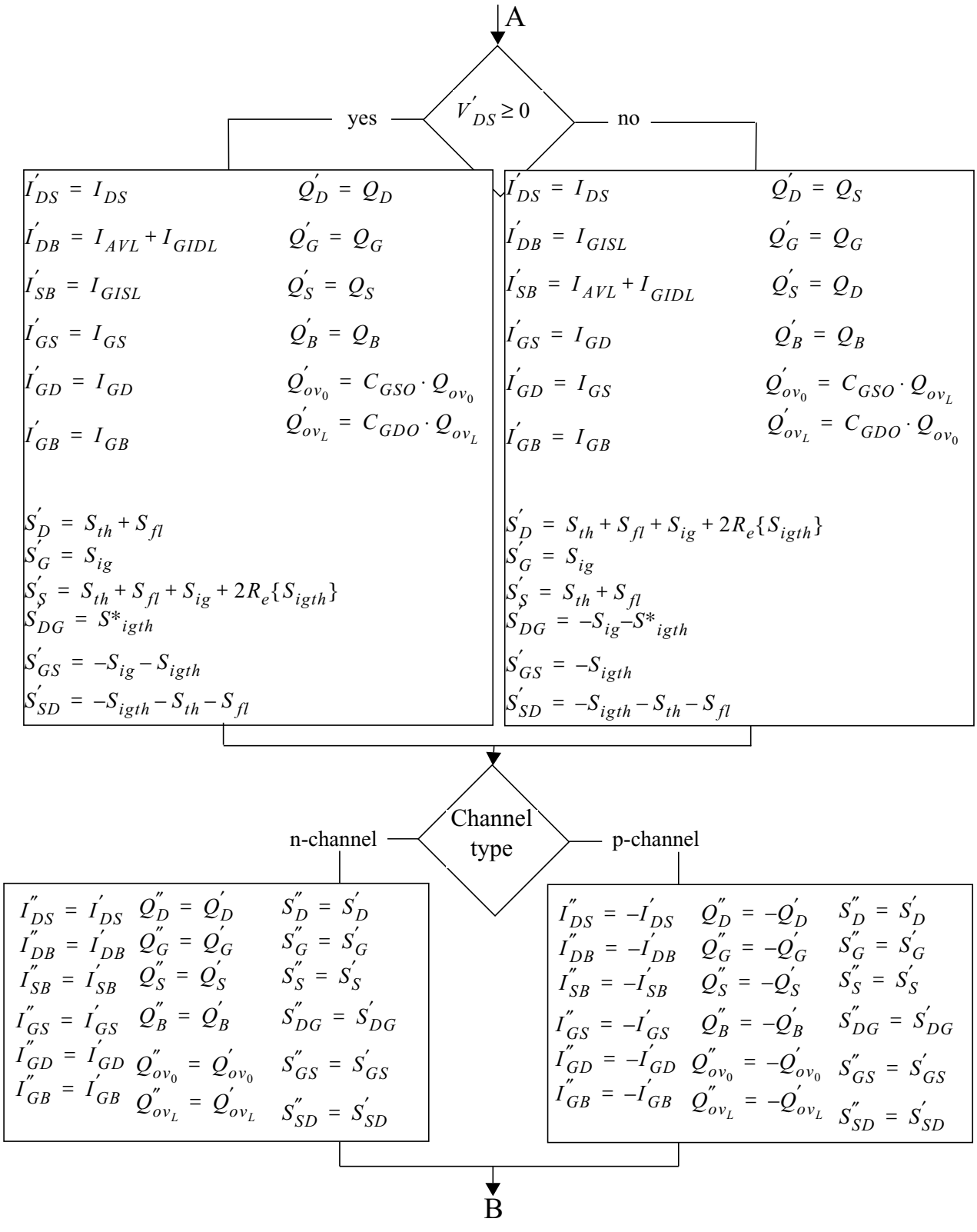
Step 4 Evaluate all the internal output quantities - channel current, weak-avalanche current, gate current, nodal charges, and noise-power spectral densities - using the standard MOS Model 1102 equations and the internal voltages.

Step 5 Correct the internal output quantities for a possible source-drain interchange. In fact, this directly establishes the external noise power spectral densities.

Step 6 Correct for a possible p-channel transformation.

Step 7 Change from branch current to nodal currents, establishing the external current output quantities. Calculate the overlap charges that are related to the physical regions and add them to the nodal charges, thus forming the external charge output quantities.




A
$V'_{DS} \geq 0$
yes
no
$I'_{DS} = I_{DS}$
$I'_{DB} = I_{AVL} + I_{GIDL}$
$I'_{SB} = I_{GISL}$
$I'_{GS} = I_{GS}$
$I'_{GD} = I_{GD}$
$I'_{GB} = I_{GB}$
$Q'_D = Q_D$
$Q'_G = Q_G$
$Q'_S = Q_S$
$Q'_B = Q_B$
$Q'_{ov_0} = C_{GSO} \cdot Q_{ov_0}$
$Q'_{ov_L} = C_{GDO} \cdot Q_{ov_L}$
$S'_D = S_{th} + S_{fl}$
$S'_G = S_{ig}$
$S'_S = S_{th} + S_{fl} + S_{ig} + 2R_e\{S_{igth}\}$
$S'_{DG} = S^*_{igth}$
$S'_{GS} = -S_{ig} - S_{igth}$
$S'_{SD} = -S_{igth} - S_{th} - S_{fl}$
$I'_{DS} = I_{DS}$
$I'_{DB} = I_{GISL}$
$I'_{SB} = I_{AVL} + I_{GIDL}$
$I'_{GS} = I_{GD}$
$I'_{GD} = I_{GS}$
$I'_{GB} = I_{GB}$
$Q'_D = Q_S$
$Q'_G = Q_G$
$Q'_S = Q_D$
$Q'_B = Q_B$
$Q'_{ov_0} = C_{GSO} \cdot Q_{ov_L}$
$Q'_{ov_L} = C_{GDO} \cdot Q_{ov_0}$
$S'_D = S_{th} + S_{fl} + S_{ig} + 2R_e\{S_{igth}\}$
$S'_G = S_{ig}$
$S'_S = S_{th} + S_{fl}$
$S'_{DG} = -S_{ig} - S^*_{igth}$
$S'_{GS} = -S_{igth}$
$S'_{SD} = -S_{igth} - S_{th} - S_{fl}$
Channel type
n-channel
p-channel
$I''_{DS} = I'_{DS}$ $Q''_D = Q'_D$ $S''_D = S'_D$
$I''_{DB} = I'_{DB}$ $Q''_G = Q'_G$ $S''_G = S'_G$
$I''_{SB} = I'_{SB}$ $Q''_S = Q'_S$ $S''_S = S'_S$
$I''_{GS} = I'_{GS}$ $Q''_B = Q'_B$ $S''_{DG} = S'_{DG}$
$I''_{GD} = I'_{GD}$ $Q''_{ov_0} = Q'_{ov_0}$ $S''_{GS} = S'_{GS}$
$I''_{GB} = I'_{GB}$ $Q''_{ov_L} = Q'_{ov_L}$ $S''_{SD} = S'_{SD}$
$I''_{DS} = -I'_{DS}$ $Q''_D = -Q'_D$ $S''_D = S'_D$
$I''_{DB} = -I'_{DB}$ $Q''_G = -Q'_G$ $S''_G = S'_G$
$I''_{SB} = -I'_{SB}$ $Q''_S = -Q'_S$ $S''_S = S'_S$
$I''_{GS} = -I'_{GS}$ $Q''_B = -Q'_B$ $S''_{DG} = S'_{DG}$
$I''_{GD} = -I'_{GD}$ $Q''_{ov_0} = -Q'_{ov_0}$ $S''_{GS} = S'_{GS}$
$I''_{GB} = -I'_{GB}$ $Q''_{ov_L} = -Q'_{ov_L}$ $S''_{SD} = S'_{SD}$
B

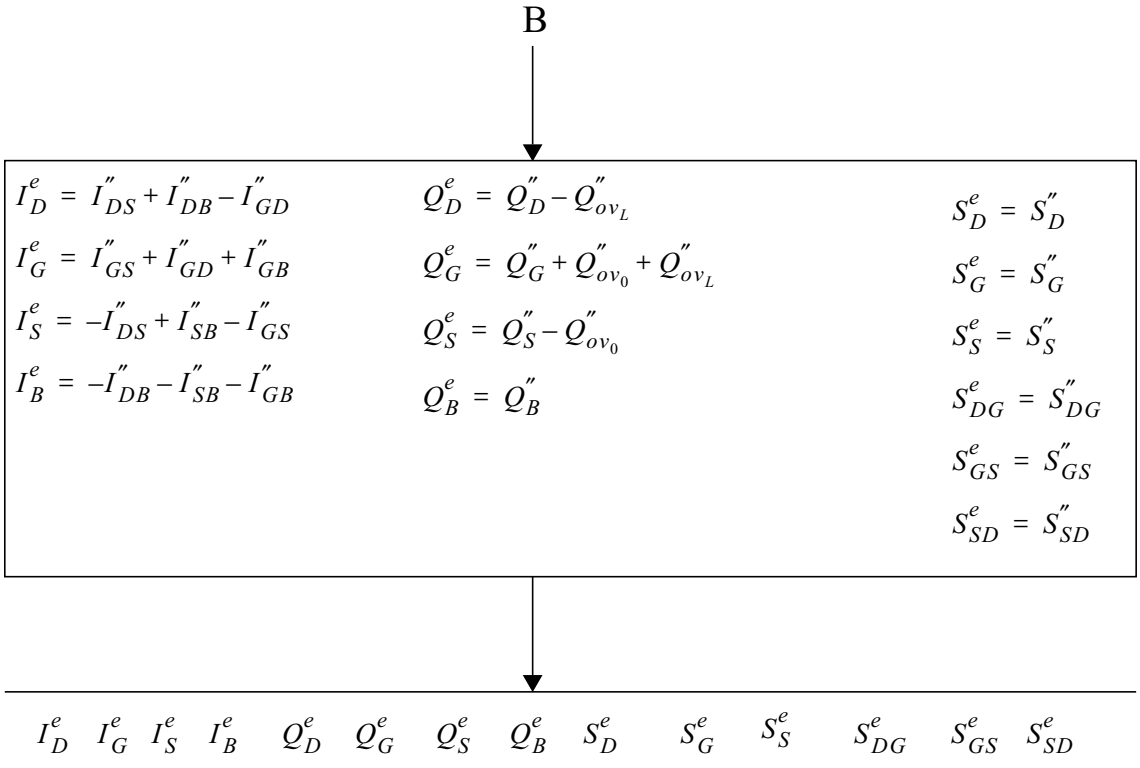


Figure 72: Transformation scheme

It is customary to have separate user models in the circuit simulators for n- and p-channel transistors. In that manner it is easy to use a different set of reference and scaling parameters for the two channel types. As a consequence, the changes in the parameter values necessary for a p-channel type transistor are normally already included in the parameter sets on file. The changes should not be included in the simulator.

15.9 Simulator specific items

15.9.1 Pstar syntax

n channel electrical model: mne_n (d,g,s,b) level=1102,<parameters>
p channel electrical model: mpe_n (d,g,s,b) level=1102, <parameters>
n channel electrical self-heating model:
mnet_n (d,g,s,b,dt) level=1102,<parameters>
p channel electrical self-heating model:
mpet_n (d,g,s,b,dt) level=1102, <parameters>
n channel physical geometrical model:
mn_n (d,g,s,b) level=11020 <parameters>
p channel physical geometrical model:
mp_n (d,g,s,b) level=11020 <parameters>
p channel physical geometrical self-heating model:
mpt_n (d,g,s,b,dt) level=11020 <parameters>
n channel physical geometrical self-heating model:
mnt_n (d,g,s,b,dt) level=11020 <parameters>
n channel binning geometrical model:
mn_n (d,g,s,b) level=11021 <parameters>
p channel binning geometrical model:
mp_n (d,g,s,b) level=11021 <parameters>
n channel binning geometrical self-heating model:
mnt_n (d,g,s,b,dt) level=11021 <parameters>
p channel binning geometrical self-heating model:
mpt_n (d,g,s,b,dt) level=11021 <parameters>

n : occurrence indicator
<parameters> : list of model parameters
d,g,s and b are drain, gate, source, bulk and self-heating terminals respectively.

15.9.2 Spectre syntax

n channel electrical model: model modelname mos1102e type=n <modpar>
componentname d g s b modelname <inpar>
p channel electrical model: model modelname mos1102e type=p <modpar>
componentname d g s b modelname <inpar>
n channel electrical self-heating model:
model modelname mos1102et type=n <modpar>
componentname d g s b dt modelname <inpar>
p channel electrical self-heating model:
model modelname mos1102et type=p <modpar>
componentname d g s b dt modelname <inpar>
n channel physical geometrical model:
model modelname mos11020 type=n <modpar>
componentname d g s b modelname <inpar>
p channel physical geometrical model:
model modelname mos11020 type=p <modpar>
componentname d g s b modelname <inpar>
n channel physical geometrical self-heating model:
model modelname mos11020t type=n <modpar>
componentname d g s b dt modelname <inpar>
p channel physical geometrical self-heating model:
model modelname mos11020t type=p <modpar>
componentname d g s b dt modelname <inpar>
n channel binning geometrical model:
model modelname mos11021 type=n <modpar>
componentname d g s b modelname <inpar>
p channel binning geometrical model:
model modelname mos11021 type=p <modpar>
componentname d g s b modelname <inpar>
n channel binning geometrical self-heating model:
model modelname mos11021t type=n <modpar>
componentname d g s b dt modelname <inpar>
p channel binning geometrical self-heating model:
model modelname mos11021t type=p <modpar>
componentname d g s b dt modelname <inpar>

modelname	:	name of model, user defined
componentname	:	occurrence indicator
<modpar>	:	list of model parameters
<inpar>	:	list of instance parameters

d,g,s and b are drain, gate, source, bulk and self-heating terminals respectively.

3 Note

Warning! In Spectre, use only the parameter statements type=n or type=p. Using any other string and/or numbers will result in unpredictable and possibly erroneous results.

15.9.3 ADS syntax

n channel electrical model: model modelname mos1102e gender=1 <modpar>
modelname:componentname d g s b <instpar>
p channel electrical model: model modelname mos1102e gender=0 <modpar>
modelname:componentname d g s b <instpar>
n channel electrical self-heating model:
model modelname mos1102et gender=1 <modpar>
modelname:componentname d g s b dt <instpar>
p channel electrical self-heating model:
model modelname mos1102et gender=0 <modpar>
modelname:componentname d g s b dt <instpar>
n channel physical geometrical model:
model modelname mos11020 gender=1 <modpar>
modelname:componentname d g s b <instpar>
p channel physical geometrical model:
model modelname mos11020 gender=0 <modpar>
modelname:componentname d g s b <instpar>
n channel physical geometrical self-heating model:
model modelname mos11020t gender=1 <modpar>
modelname:componentname d g s b dt <instpar>
p channel physical geometrical self-heating model:
model modelname mos11020t gender=0 <modpar>
modelname:componentname d g s b dt <instpar>
n channel binning geometrical model:
model modelname mos11021 gender=1 <modpar>
modelname:componentname d g s b <instpar>
p channel binning geometrical model:
model modelname mos11021 gender=0 <modpar>
modelname:componentname d g s b <instpar>
n channel binning geometrical self-heating model:
model modelname mos11021t gender=1 <modpar>
modelname:componentname d g s b dt <instpar>

p channel binning geometrical self-heating model:

model modelname mos11021t gender=0 <modpar>
modelname:componentname d g s b dt <instpar>

modelname	:	name of model, user defined
componentname	:	occurrence indicator
<modpar>	:	list of model parameters
<instpar>	:	list of instance parameters

d,g,s and b are drain, gate, source, bulk and self-heating terminals respectively.

15.9.4 The ON/OFF condition for Pstar

The solution for a circuit involves a process of successive calculations. The calculations are started from a set of 'initial guesses' for the electrical quantities of the nonlinear elements. A simplified DCAPPROX mechanism for devices using ON/OFF keywords is mentioned in [9]. By default the devices start in the default state.

n-channel			
	Default	ON	OFF
V_{DS}	1.25	1.25	2.5
V_{GS}	1.25	1.25	0.0
V_{SB}	0.0	0.0	0.0

p-channel			
	Default	ON	OFF
V_{DS}	-1.25	-1.25	-2.5
V_{GS}	-1.25	-1.25	0.0
V_{SB}	0.0	0.0	0.0

15.9.5 The ON/OFF condition for Spectre

n-channel							
	OFF	Triode	Saturation	Subthreshold	Reverse	Forward	Breakdown
V_{DS}	0.0	0.75	1.25	2.0	0	0	0
V_{GS}	0.0	2.0	1.25	0.25	0	0	0
V_{SB}	0.0	0.0	0.0	0.0	0	0	0

p-channel							
	OFF	Triode	Saturation	Subthreshold	Reverse	Forward	Breakdown
V_{DS}	0.0	-0.75	-1.25	-2.0	0	0	0
V_{GS}	0.0	-2.0	-1.25	-0.25	0	0	0
V_{SB}	0.0	0.0	0.0	0.0	0	0	0

15.9.6 The ON/OFF condition for ADS

n-channel	
	Default
V_{DS}	0
V_{GS}	0
V_{SB}	0

p-channel	
	Default
V_{DS}	0
V_{GS}	0
V_{SB}	0

15.10Parameter Extraction

The parameter extraction strategy for MOS Model 11 using an **optimization method** consists of four main steps:

1. measurements
2. extraction of miniset parameters at room temperature
3. extraction of temperature scaling parameters
4. extraction of geometry scaling parameters.

The above steps will be briefly described in the following sections.

15.10.1Measurements

The parameter extraction routine consists of four different dc-measurements and two (optional) capacitance measurements[1]:

- **Measurement I:** $I_D/g_m/I_G$-V_{GS} - characteristics in linear region:

n-channel : $V_{GS} = 0 \ldots V_{sup}$ (with steps of maximum 50 mV).
$V_{DS} = 50$ mV
$V_{BS} = 0 \ldots -V_{sup}$

p-channel : $V_{GS} = 0 \ldots -V_{sup}$ (with steps of maximum 50 mV).
$V_{DS} = -50$ mV
$V_{BS} = 0 \ldots V_{sup}$

- **Measurement II:** Subtreshold I_D-V_{GS} - characteristics:

n-channel : $V_{GS} = V_T - 0.6$ V ... $V_T + 0.3$ V
$V_{DS} = 3$ values starting from 100 mV to V_{sup}
$V_{BS} = 0 \ldots -V_{sup}$

p-channel : $V_{GS} = V_T + 0.6$ V ... $V_T - 0.3$ V
$V_{DS} = 3$ values starting from -100 mV to $-V_{sup}$
$V_{BS} = 0 \ldots V_{sup}$

1.The bias conditions to be used for the measurements are dependent on the supply voltage of the process. Of course it is adviseable to restrict the range of voltages to this supply voltage Vsup. Otherwise physical effects, atypical for normal transistor operation and therefore less well described by MOS Model 11, may dominate the characteristics.

- **Measurement III:** $I_D/g_{DS}/I_G$-V_{DS} - characteristics:

n-channel : V_{DS} = 0 ... V_{sup} (with steps of maximum 50 mV).
V_{GS} = 4 values starting from V_T + 0.1 V , not above V_{sup}
V_{BS} = 3 values starting from 0 V to -V_{sup}

p-channel : V_{DS} = 0 ... -V_{sup} (with steps of maximum 50 mV).
V_{GS} = 4 values starting from V_T + 0.1 V , not below -V_{sup}
V_{BS} = 3 values starting from 0 V to V_{sup}

- **Measurement IV:** $I_D/I_S/I_G/I_B$-V_{GS} - characteristics in all operation regions:

n-channel : V_{GS} = -V_{sup} ... V_{sup} (with steps of maximum 50 mV).
V_{DS} = 4 values starting from 0 V to V_{sup}
V_{BS} = 0 V

p-channel : V_{GS} = -V_{sup} ... -V_{sup} (with steps of maximum 50 mV).
V_{DS} = 4 values starting from 0 V to -V_{sup}
V_{BS} = 0 V

- **Measurement V:** C_{gg}-V_{GS} - characteristics (optional):

n/p-channel : V_{GS} = -V_{sup} ... V_{sup} (with steps of maximum 50 mV).
V_{DS} = 0 V
V_{BS} = 0 V

- **Measurement VI:** C_{cg}-V_{GS} - characteristics:

n/p-channel : V_{GS} = -V_{sup} ... V_{sup}
V_{DS} = 0 V
V_{BS} = 0 V

The values of transconductance g_m and output conductance g_{DS} are extracted from the I - V-curves by calculating in a numerical way the derivative of I_D to V_{GS} and V_{DS}, respectively. In the subthreshold measurements, Measurement II, use is made of threshold voltage V_T, which has to be determined for all the bulk-source bias values V_{BS}. The determination of V_T is rather arbitrary, and it can be either determined using the lineas extrapolation method or the constant current criterion. The channel-to-gate capacitance C_{cg} is the summation of the

drain-to-gate capacitance C_{dg} and the source-to-gate capacitance C_{sg} (i.e. source and drain are short-circuited), it is needed to extract overlap capacitance parameters.

For the miniset extraction measurements I through IV have to be performed at room temperature for every device. In addition measurements V and VI need to be performed for a long/broad and a short/broad (i.e. $L = L_{min}$) transistor (at room temperature). Furthermore, for the extraction of temperature scaling parameters measurements I, III and IV have to be performed at different temperatures (at least two, typically -40°C and 125°C) for at least a long/broad and a short/broad transistor.

15.10.2Extraction of Miniset Parameters at Room Temperature

The extraction of miniset parameters is performed for every device. In order to ensure that the temperature scaling relations do not affect the behaviour at room temperature, the reference temperature T_R is chosen equal to room temperture. In general the simultaneous determination of all miniset parameters is not advisable, because the value of some parameters can be wrong due to correlation and suboptimization. Therefore it is more practical to split the parameters into several groups, where each parameter group can be determined using specific measurements.

Although the poly-depletion effect affects the dc-behaviour of a MOSFET, the poly-depletion parameter KPINV can only be determined accurately from *C-V*-measurements. If the (physical) oxide thickness t_{ox} and the polysilicon impurity concentration N_P are known, the parameter KPINV ($= 1/(k_p)$) can be calculated from[1]:

$$k_p = \frac{t_{ox} \cdot \sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_p}}{\varepsilon_{ox}} \tag{15.363}$$

If the polysilicon impurity concentration N_P is not known, as a good first-order estimate one can use $N_p = 1 \cdot 10^{26} m^{-3}$ for n^+-polysilicon gates and $N_p = 5 \cdot 10^{25} m^{-3}$ for p^+-polysilicon gates. In the latter case a measured C_{GG}-V_{GS}-characteristic for a long-channel transistor is essential for an accurate determination of KPINV.

1.For metal gates the poly-depletion effect does not occur and in this case KPINV = 0.

Table 19: Starting miniset parameter values for parameter extraction at room temperature T_R of a typical MOSFET with channel length L (m), channel width W(m), oxide thickness t_{ox} (m), polysilicon impurity concentration N_P (m^{-3}) and minimum technology feature size L_{min}. If the polysilicon concentration N_P is not known, one can use $N_p = 1 \cdot 10^{26} m^{-3}$ or $5 \cdot 10^{25} m^{-3}$ for n^+- resp. p^+-polysilicon gates. Parameters C_{ox}, C_{GSO} and C_{GDO} are only important for the charge model, and do not affect the dc-model; they have to be extracted from C-V -characteristics. In order to determine the parameter geometry-scaling, the last column indicates for which conditions the parameters have to be extracted: L=long-channel device (fixed for short-channel devices), S=short-channel devices, A=all devices and F=fixed parameter.

Parameter	Program Name	Parameter Value		Extracted for
		NMOS	PMOS	
V_{FB}	VFB	-1.1	-0.95	L
k_0	KO	0.25	0.25	A
$1/k_p$	KPINV	$6.0 \cdot 10^3/(t_{OX} \cdot \sqrt{N_p})$	$6.0 \cdot 10^3/(t_{OX} \cdot \sqrt{N_p})$	L
ϕ_B	PHIB	0.95	0.95	A
β	BET	$1.7 \cdot 10^{-12}/t_{OX} \cdot W/L$	$4.5 \cdot 10^{-13}/t_{OX} \cdot W/L$	A
θ_{sr}	THESR	$1.5 \cdot 10^{-9}/t_{OX}$	$2.3 \cdot 10^{-9}/t_{OX}$	L
θ_{ph}	THEPH	$1.3 \cdot 10^{-10}/t_{OX}$	$2.2 \cdot 10^{-10}/t_{OX}$	L
η_{mob}	ETAMOB	1.3	3.0	L
ν	NU	2.0	2.0	A
C_s	CS	0.1	0.1	A
θ_R	THER	$1.3 \cdot 10^{-7}/L$	$8.0 \cdot 10^{-8}/L$	S
θ_{R1}	THER1	0	0	-
θ_{R2}	THER2	1	1	-
θ_{sat}	THESAT	$4.5 \cdot 10^{-7}/L$	$2.0 \cdot 10^{-7}/L$	A
θ_{Th}	THETH	$1.0 \cdot 10^{-6}$	$1.0 \cdot 10^{-6}$	A

Table 19: Starting miniset parameter values for parameter extraction at room temperature T_R of a typical MOSFET with channel length L (m), channel width W(m), oxide thickness t_{ox} (m), polysilicon impurity concentration N_P (m^{-3}) and minimum technology feature size L_{min}. If the polysilicon concentration N_P is not known, one can use $N_p = 1 \cdot 10^{26} m^{-3}$ or $5 \cdot 10^{25} m^{-3}$ for n^+- resp. p^+-polysilicon gates. Parameters C_{ox}, C_{GSO} and C_{GDO} are only important for the charge model, and do not affect the dc-model; they have to be extracted from C-V -characteristics. In order to determine the parameter geometry-scaling, the last column indicates for which conditions the parameters have to be extracted: L=long-channel device (fixed for short-channel devices), S=short-channel devices, A=all devices and F=fixed parameter.

Parameter	Program Name	Parameter Value		Extracted for
		NMOS	PMOS	
σ_{dib1}	SDIBL	$5.0 \cdot 10^{-2} \cdot (L_{min}/L)^2$	$5.0 \cdot 10^{-2} \cdot (L_{min}/L)^2$	S
m_0	MO	$1.0 \cdot 10^{-3}$	$1.0 \cdot 10^{-3}$	A
σ_{sf}	SSF	$6.0 \cdot 10^{-2} \cdot L_{min}/L$	$6.0 \cdot 10^{-2} \cdot L_{min}/L$	A
α	ALP	$6.0 \cdot 10^{-2} \cdot L_{min}/L$	$6.0 \cdot 10^{-2} \cdot L_{min}/L$	A
V_p	VP	$5.0 \cdot 10^{-2}$	$1.0 \cdot 10^{-1}$	F
m	MEXP	use Eq. (12.132)	use Eq. (12.132)	-
a_1	A1	25	100	A
a_2	A2	25	37	A
a_3	A3	1	1	A
I_{GINV}	IGINV	$3.0 \cdot 10^{-5} \cdot W \cdot L/{t_{ox}}^2$	$4.0 \cdot 10^{-5} \cdot W \cdot L/{t_{ox}}^2$	A
B_{INV}	BINV	$2.9 \cdot 10^{+10} \cdot t_{ox}$	$4.3 \cdot 10^{+10} \cdot t_{ox}$	L
I_{GACC}	IGACC	$3.0 \cdot 10^{-5} \cdot W \cdot L/{t_{ox}}^2$	$2.0 \cdot 10^{-5} \cdot W \cdot L/{t_{ox}}^2$	A
B_{ACC}	BACC	B_{INV}	$2.9 \cdot 10^{+10} \cdot t_{ox}$	L
$V_{FB_{OV}}$	VFBOV	0.1	0.1	L
k_{ov}	KOV	$9.3 \cdot 10^{+8} \cdot t_{ox}$	$3.8 \cdot 10^{+8} \cdot t_{ox}$	L
I_{GOV}	IGOV	$5.0 \cdot 10^{-13} \cdot W/{t_{ox}}^2$	$5.0 \cdot 10^{-12} \cdot W/{t_{ox}}^2$	A

Table 19: Starting miniset parameter values for parameter extraction at room temperature T_R of a typical MOSFET with channel length L (m), channel width W(m), oxide thickness t_{ox} (m), polysilicon impurity concentration N_P (m^{-3}) and minimum technology feature size L_{min}. If the polysilicon concentration N_P is not known, one can use $N_p = 1 \cdot 10^{26} m^{-3}$ or $5 \cdot 10^{25} m^{-3}$ for n^+- resp. p^+-polysilicon gates. Parameters C_{ox}, C_{GSO} and C_{GDO} are only important for the charge model, and do not affect the dc-model; they have to be extracted from C-V -characteristics. In order to determine the parameter geometry-scaling, the last column indicates for which conditions the parameters have to be extracted: L=long-channel device (fixed for short-channel devices), S=short-channel devices, A=all devices and F=fixed parameter.

Parameter	Program Name	Parameter Value		Extracted for
		NMOS	PMOS	
A_{GIDL}	AGIDL	$1.6 \cdot 10^{-13} \cdot W / t_{ox}^{\ 2}$	$1.2 \cdot 10^{-17} \cdot W / t_{ox}^{\ 2}$	A
B_{GIDL}	BGIDL	$1.6 \cdot 10^{+8} \cdot t_{ox}$	$1.0 \cdot 10^{+10} \cdot t_{ox}$	L
C_{GIDL}	CGIDL	0	0	L

Before the optimization is started a parameter set has to be determined which contains a first estimation of the parameters to be extracted and the parameters which remain constant. The value of smoothing factor *m* is calculated from the device length *L* and from the minimum feature size of the technology L_{min} using Eq. (15.136). The parameter set used as a first-order estimation of the parameters to be extracted is given in Table 20. With this parameter set a first optimization following the scheme below, is performed. After this the new parameter set serves as an estimation for the second optimization, which is performed following the same scheme. This method yields a proper set of parameters after the second optimization. Experi-

ments with transistors of different processes show that the parameter set does not change very much after a third optimization.

Table 20: DC-parameter extraction procedure for a long-channel n-MOSFET, where Steps 2 and 12 are optional. For p-type transistors all voltages and currents have to be multiplied by - 1. The optimization is either performed on the absolute or relative deviation between model and measurements. Parameter I_{tst} is 2.5 μA for NMOS and 0.8 μA for PMOS. For n-MOSFETs $B_{acc} = B_{inv}$, and as a result B_{acc} does not have to be extracted. For p-MOSFETs this is not the case, see Table. 10.

Step	Optimised Parameters	Measure-ment	Fitted On	Absolute/Relative	Specific Conditions
1	$\phi_B, k_0, \beta, \theta_{sr}, C_s$	I	I_D	Absolute	-
2	V_{FB}, k_0, k_P, C_{ox}	V	C_{gg}	Relative	-
3	ϕ_B, k_0, m_0	II	I_D	Relative	-
4	$\beta, \theta_{sr}, \theta_{ph}, C_s$	I	I_D / g_m	Relative	$V_{SB} = 0V$ $V_{GS} > V_T + 0.3V$
5	η_{mob}	I	I_D	Absolute	$I_D > W/L \cdot I_{tst}$
6	θ_{sat}	III	I_D	Absolute	-
7	$\sigma_{sf}, \alpha, \theta_{Th}$	III	g_{DS}	Relative	-
8	θ_{sat}	III	I_D	Absolute	-
9	I_{GINV}, B_{INV}	I	I_G	Absolute	-
19	$I_{GOV}, (B_{ACC}), I_{GACC}, k_{ov}$	IV	I_G	Relative	$V_{GS} < 0V$
11	a_1, a_2, a_3	IV	I_B	Absolute	$V_{GS} \geq 0V$
12	$A_{GIDL}, B_{GIDL}, C_{GIDL}$	IV	I_B	Absolute	$V_{GS} < 0V$
13	V_{FB}, k_p, C_{ox}	V	C_{gg}	Relative	-
14	Repeat steps 3, 4, 5, 6, 7, 8, 9, 10, 11and 12				

For an accurate extraction of parameter values, the parameter set for a long-channel transistor has to be determined first. In the long-channel case the poly-depletion parameter $1/k_P$, the flat-band voltage VFB, the carrier mobility (i.e. θ_{sr}, θ_{ph}, η_{mob}, and C_s) and the gate tunnel-

ling probability factors (B_{inv} and B_{acc}) can be determined, and they can subsequently be fixed for the short and narrow-channel devices, see Tab. 20. In Table 21 the extraction procedure for long-channel transistors is given. Since the value of body-factor k_0 may change much over geometry and over technology, the first-order estimate in Tab. 7.1 is very crude and a more accurate, preliminary value is obtained using Step 1. In Step 2 (optional) more accurate values of the poly-depletion parameter $1/k_P$ and the flat-band voltage V_{FB} (which determines the onset of accumulation) are extracted. Next the subthreshold parameters ϕ_B, k_0 and m_0 are optimized in Step 3, neglecting short-channel effects such as drain-induced barrier-lowering (DIBL). After that the mobility parameters are optimized using Steps 4 and 5, neglecting the influence of series-resistance. In Step 6 a preliminary value of the velocity saturation parameter is obtained, and subsequently the conductance parameters σ_{sf}, α and θ_{Th} are determined in Step 7. A more accurate value of θ_{sat} can now be obtained using Step 8 (which is Step 6 repeated). The gate current parameters are determined in Steps 9 and 10, followed by the weak-avalanche parameters in Step 11, and finally, the gate-induced leakage current parameters are optimized in step 12.

Table 21: DC-parameter extraction procedure for a short-channel n-MOSFET. For p-type transistors all voltages and currents have to be multiplied by - 1. Parameters $1/k_P$, V_{FB}, θ_{sr}, θ_{ph}, η_{mob}, B_{inv}, B_{acc}, k_{ov}, B_{GIDL} and C_{GIDL} are taken from the long-channel case. The optimization is either performed on the absolute or relative deviation between model and measurements.

Step	Optimised Parameters	Measure-ment	Fitted On	Absolute/Relative	Specific Conditions
1	ϕ_B, k_0, β, θ_R, C_s	I	I_D	Absolute	-
2	ϕ_B, k_0, m_0, σ_{dibl}	II	I_D	Relative	-
3	β, θ_R, C_s	I	I_D/g_m	Relative	$V_{SB} = 0V$ $V_{GS} > V_T + 0.3V$
4	θ_{sat}	III	I_D	Absolute	-
5	σ_{sf}, α, θ_{Th}, σ_{dibl}	III	g_{DS}	Relative	-
6	θ_{sat}	III	I_D	Absolute	-
7	I_{GINV}, I_{GOV}, I_{GACC}	IV	I_D	Relative	-
8	a_1, a_2, a_3	IV	I_B	Absolute	$V_{GS} \geq 0V$

Table 21: DC-parameter extraction procedure for a short-channel n-MOSFET. For p-type transistors all voltages and currents have to be multiplied by - 1. Parameters $1/k_P$, V_{FB}, θ_{sr}, θ_{ph}, η_{mob}, B_{inv}, B_{acc}, k_{ov}, B_{GIDL} and C_{GIDL} are taken from the long-channel case. The optimization is either performed on the absolute or relative deviation between model and measurements.

Step	Optimised Parameters	Measure-ment	Fitted On	Absolute/Relative	Specific Conditions
9	A_{GIDL}	IV	I_B	Absolute	$V_{GS} < 0V$
10	Repeat steps 2, 3, 4, 5, 7, 8 and 9.				

For short-channel devices the values of the poly-depletion parameter $1/k_P$, flat-band voltage V_{FB},the carrier mobility parameters (θ_{sr}, θ_{ph} and η_{mob}) and the gate tunnelling probability factors *(B_{inv}* and B_{acc}) of the long-channel device are copied, and next the extraction procedure as given in Table 23 is executed. In contrast to the long-channel case, the extraction procedure for short-channel devices also optimizes the parameters for series-resistance[1] and DIBL.

Table 22: Starting miniset parameter values for AC-parameter extraction of a typical MOSFET with channel length L (m), channel width W (m) and oxide thickness t_{ox} (m).

Parameter	Program Name	Parameter Value	
		NMOS	PMOS
C_{ox}	COX	$\varepsilon_{ox}/t_{ox} \cdot W \cdot L$	$\varepsilon_{ox}/t_{ox} \cdot W \cdot L$
C_{GDO}	CGDO	$3.0 \cdot 10^{-10} \cdot W$	$3.0 \cdot 10^{-10} \cdot W$
C_{GSO}	CGSO	$3.0 \cdot 10^{-10} \cdot W$	$3.0 \cdot 10^{-10} \cdot W$

AC-parameters: In Table 22**,** a first-order estimation of the AC-parameters is given. The AC-parameters C_{ox}, C_{GSO}, C_{GDO}, k_{ov} and V_{FBov} cannot be (accurately) de-termined from DC-characteristics, and as a consequence they have to be determined from C–V– characteristics[2]. Since normal MOS transistors are symmetrical devices, one can assume that the oxide

1.Note that in Table 10 parameters θ_{R1} and θ_{R2} are not included, which implies that the series-resistamce is assumed to be voltage-independent. This holdss true for modern CMOS technologies, where no use is made of LDD-structures.
2.Although parameter k_{ov} can be determined from overlap gate current, see Table 9, it is nonetheless more accurately determined from the C_{cg}-V_{GS} characteristics.

capacitance of the source and drain extension are identical, which implies that C_{GSO}=C_{GDO}. The oxide capacitance of the intrisic MOSFET C_{ox} can be extracted from Measurement VI. In Table 23 the extraction procedure for the AC-parameters is given.

Table 23: AC-parameter extraction procedure for a MOSFET. Here it is assumed that C_{GSO} = C_{GDO}. In the first instance flat-band voltage V_{FBov} is not optimised, although it may be optimised during Step 1 in order to ob-tain more accurate results. The optimization is either performed on the absolute or relative deviation between model and measurements.

Step	Optimised Parameters	Measure-ment	Fitted On	Absolute/Relative	Specific Conditions
1	k_{ov} , C_{GSO}	VI	C_{cg}	Relative	$V_{GS} < 0V$
2	C_{ox}	V	C_{gg}	Relative	-
3	Repeat steps 1 and 2				

15.10.3Extraction of Temperature Scaling Parameters

For a specific device the temperature scaling parameters can be extracted after the miniset at room temperature has been extracted. In order to do so, measurements I, III and IV need to be performed at various temperature values (at least two values different from room temperature, typically - 40^{o} C and 125^{o} C).

Since the reference temperature T_R has been chosen equal to room temperature, the modelled behaviour at room temperature is not affected by different values of the temperature scaling parameters. As a first-order estimation of the temperature scaling parameter values, the

default values as given in Section 15.3.2 are used. Again the parameter extraction scheme is slightly different for the long-channel and for the short-channel case.

Table 24: Temperature scaling parameter extraction procedure for a long-channel n-MOSFET, where measurements have been performed at various temperature values. For p-type transistors all voltages and currents have to be multiplied by -1. The optimization is either performed on the abso-lute or relative deviation between model and measurements. Parameter I_{tst} is 2.5 μA for NMOS and 0.8 μA forPMOS.

Step	Optimised Parameters	Measure-ment	Fitted On	Absolute/Relative	Specific Conditions
1	$S_{T;\phi_B}$	I	I_D	Relative	$I_D < W/L \cdot I_{tst}$
2	$\eta_\beta, \eta_{sr}, \eta_{ph}, \nu_{exp}, S_{T;\eta_{mob}}, \eta_{C_s}$	I	I_D	Relative	$I_D > W/L \cdot I_{tst}$
3	η_{sat}	III	I_D	Absolute	-
4	$S_{T;a_1}$	IV	I_B	Absolute	$V_{GS} \geq 0V$
5	$S_{T;B_{GIDL}}$	IV	I_B	Absolute	$V_{GS} < 0V$

For an accurate extraction, the temperature scaling parameters for a long-channel device have to be determined first. In the long-channel case the carrier mobility parameters (i.e. η_{sr}, η_{ph}, ν_{exp} and $S_{T;\eta_{mob}}$) can be determined, and they can subsequently be fixed for the short-channel devices. In Table 24 the extraction procedure for long-channel transistors is given. In Step 1 the subthreshold temperature dependence is optimized, followed by the optimization of mobility reduction parameters in Step 2. Next the temperature dependence of velocity saturation is optimized in Step 3. In Step 4 the temperature dependence of impact ionization is determined, and finally, in step 5 the temperature dependence of the gate-induced drain leakage is optimized.

For short-channel devices the values of the mobility reduction temperature scaling parameters (i.e. η_{sr}, η_{ph}, ν_{exp} and $S_{T;\eta_{mob}}$) of the long-channel device are copied, and next the extraction procedure as given in Table 25 is executed. In contrast to the long-channel case,

the extraction procedure for short-channel devices optimizes the parameter for series-resistance.

Table 25: Temperature scaling parameter extraction procedure for a short-channel n-MOSFET, where measurements have been performed at various temperature values. For p-type transistors all voltages and currents have to be multiplied by -1. The optimization is either performed on the absolute or relative deviation between model and measurements. Parameter I_{tst} is 2.5 μA for NMOS and 0.8 μA for PMOS.

Step	Optimised Parameters	Measure-ment	Fitted On	Absolute/Relative	Specific Conditions
1	$S_{T;\phi_B}$	I	I_D	Relative	$I_D < W/L \cdot I_{tst}$
2	$\eta_\beta, \eta_R, \eta_{C_s}$	I	I_D	Relative	$I_D > W/L \cdot I_{tst}$
3	η_{sat}	III	I_D	Absolute	-
4	$S_{T;a_1}$	IV	I_B	Absolute	$V_{GS} \geq 0V$
5	$S_{T;B_{GIDL}}$	IV	I_B	Absolute	$V_{GS} < 0V$

15.10.4Extraction of Geometry Scaling Parameters

In general the most important part of the geometry scaling scheme is the determination of ΔL and ΔW, see eqs. (15.114) and (15.117), since it affects the DC-, the AC- as well as the noise model. Tradi-tionally ΔW can be determined from the extrapolated zero-crossing in the gain factor β versus mask width *W*. In a similar way ΔL can be determined from the inverse gain factor $1/\beta$ versus mask length *L*. For modern MOS devices with pocket implants, however, it has been found that the above ΔL extraction method is no longer valid [16], [18]. Another, more accurate method is to measure the gate-to-bulk capacitance C_{GB} in accumulation for different channel lengths [17], [18]. In this case the extrapolated zero-crossing in the C_{GB} versus mask length *L* curve will give ΔL. Unfortunately for CMOS technologies in which gate current is non-negligible, capacitance measurements may be hampered by gate current [19]. In this case either gate current parameter I_{GINV} or I_{GACC} plotted as a function of channel length *L* may be used to extract ΔL [19].

In MM11, Level 1102, one can use either physical or binning geometry scaling rules. When using the binning rules of Section 15.3.3, the scaling parameters for one bin can be directly calculated from the minisets of the four corner devices of the bin. The binning scheme ensures that the minisets are exactly reproduced in the bin corners, and that no humps occur

in parameter values across bin borders. The exact way to calculate binning parameters from minisets is described in Appendix B.

When using the physical scaling relations of Section 15.3.2 it is possible to calculate a parameter set for a process, given the parameter set of typical transistors of this process. To accomplish this, transistors of different lengths, widths and at different temperatures have to be measured. Using these measurements the sensitivities of the parameters on length, width and temperature can be found. For the determination of a geometry-scaled parameter set a three-step procedure is recommended:

1. Determine minisets (ϕ_B, k_0, β, ...) for all measured devices, as explained in Sections 15.10.2 and 15.10.3.
2. The width and length sensitivity coefficients are optimized by fitting the appropriate geometry scaling rules to these miniset parameters.
3. Finally the width and length sensitivity coefficients are optimized by fitting the result of the scaling rules and current equations to the measured currents of all devices simultaneously.

Parameter sets have been determined for several processes using this parameter extraction strategy and taking care of not exceeding the supply voltage. For all processes good results have been obtained.

15.11References

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A Hyp functions

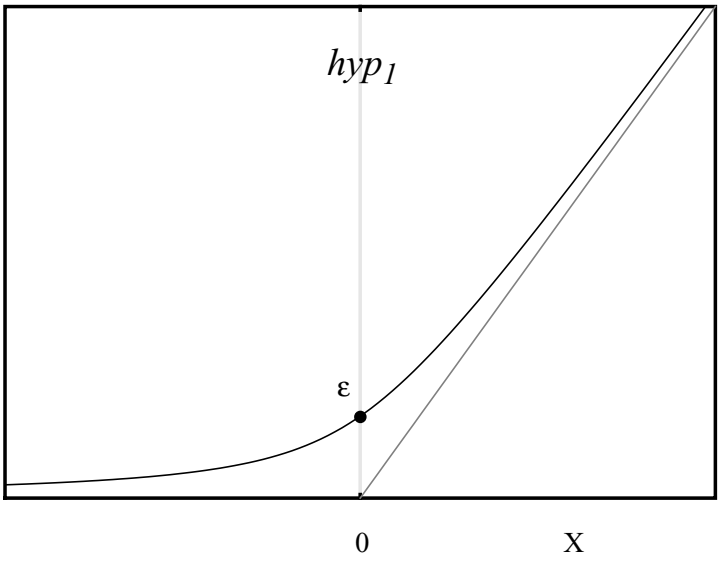


Figure 73: $hyp_1(x;\varepsilon) = \frac{1}{2} \cdot (x + \sqrt{x^2 + 4 \cdot \varepsilon^2})$

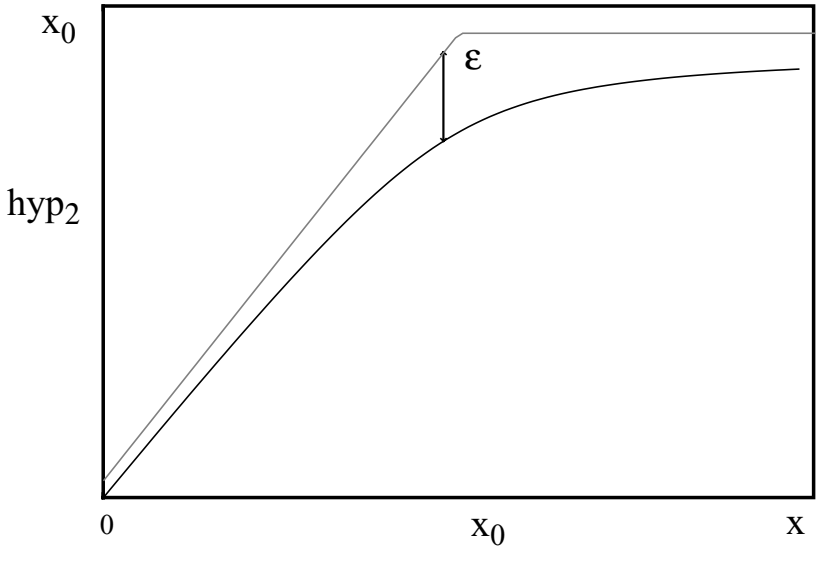


Figure 74: $hyp_2(x;x_0;\varepsilon) = x - hyp_1(x - x_0;\varepsilon)$

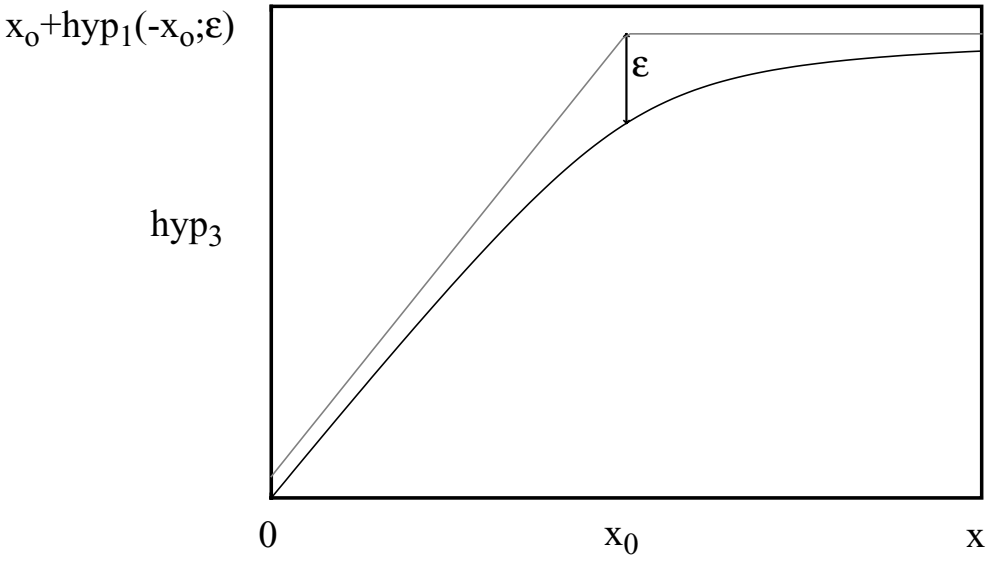


Figure 75: $hyp_3(x;x_0;\varepsilon) = hyp_2(x;x_0;\varepsilon) - hyp_2(0;x_0;\varepsilon)$ *for* $\varepsilon = \varepsilon(x_0)$

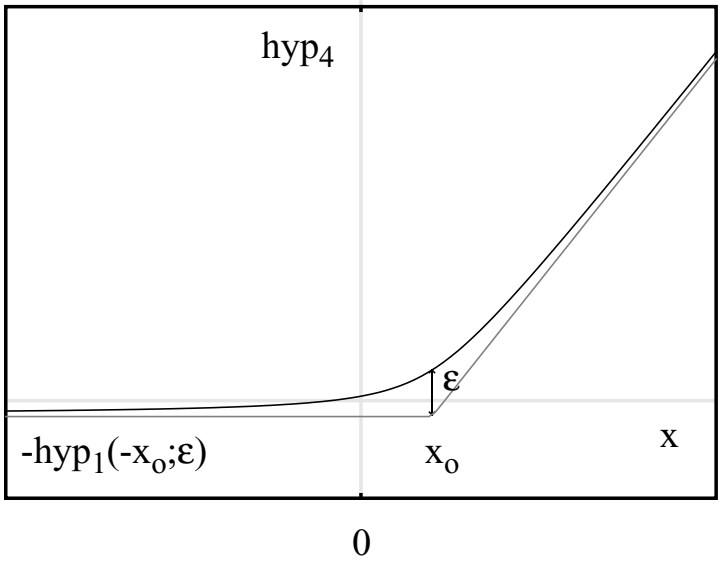


Figure 76: $hyp_4(x;x_0;\varepsilon) = hyp_1(x - x_0;\varepsilon) - hyp_1(-x_0;\varepsilon)$

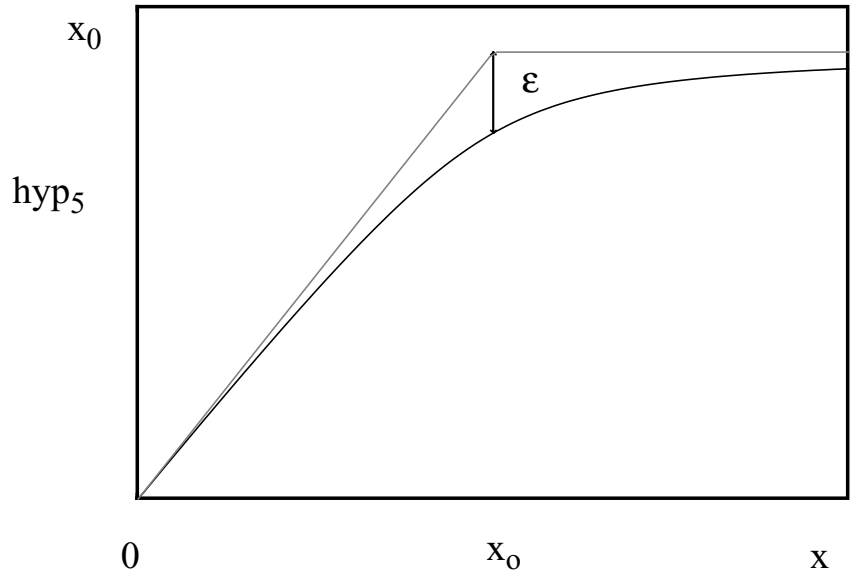


Figure 77: $hyp_5(x;x_0;\varepsilon) = x_0 - hyp_1\left(x_0 - x - \frac{\varepsilon^2}{x_0},\varepsilon\right)$ *for* $\varepsilon = \varepsilon(x_0)$

The hypm-function:

$$hypm[x,y;m] = \frac{x \cdot y}{(x^{2 \cdot m} + y^{2 \cdot m})^{1/(2 \cdot m)}} \qquad (15.364)$$

B Spectre Specific Information

Imax, Imelt, Jmelt parameters

Introduction

Imax, Imelt and Jmelt are Spectre-specific parameters used to help convergence and to prevent numerical problems. We refer in this text only to the use of Imax model parameter in Spectre with SiMKit devices since the other two parameters, Imelt and Jmelt, are not part of the SiMKit code. For information on Imelt and Jmelt refer to Cadence documentation.

Imax model parameter

Imax is a model parameter present in the following SiMKit models:
– juncap and juncap2
– psp and pspnqs (since they contain juncap models)

In Mextram 504 (bjt504) and Modella (bjt500) SiMKit models, Imax is an internal parameter and its value is set through the adapter via the Spectre-specific parameter Imax.
The default value of the Imax model parameter is 1000A. Imax should be set to a value which is large enough so it does not affect the extraction procedure.

In models that contain junctions, the junction current can be expressed as:

$$I = I_s \exp\left(\frac{V}{N \cdot \phi_{TD}} - 1\right) \tag{15.365}$$

The exponential formula is used until the junction current reaches a maximum (explosion) current Imax.

$$I_{max} = I_s \exp\left(\frac{V_{expl}}{N \cdot \phi_{TD}} - 1\right) \tag{15.366}$$

The corresponding voltage for which this happens is called Vexpl (explosion voltage). The voltage explosion expression can be derived from (1):

$$V_{expl} = N \cdot \phi_{TD} \log\left(\frac{I_{max}}{I_s}\right) + 1 \tag{15.367}$$

For $V > V_{expl}$ the following linear expression is used for the junction current:

$$I = I_{max} + (V - V_{\exp l})\frac{I_s}{N \cdot \phi_{TD}} \exp\left(\frac{V_{\exp l}}{N \cdot \phi_{TD}}\right) \quad (15.368)$$

Region parameter

Region is an Spectre-specific model parameter used as a convergence aid and gives an estimated DC operating region. The possible values of region depend on the model:

– For Bipolar models:
  – subth: Cut-off or sub-threshold mode
  – fwd: Forward
  – rev: Reverse
  – sat: Saturation.
  – off[1]
  –
– For MOS models:
  – subth: Cut-off or sub-threshold mode;
  – triode: Triode or linear region;
  – sat: Saturation
  – off[1]

For PSP and PSPNQS all regions are allowed, as the PSP(NQS) models both have a MOS part and a juncap (diode). Not all regions are valid for each part, but when e.g. region=forward is set, the initial guesses for the MOS will be set to zero. The same holds for setting a region that is not valid for the JUNCAP.

– For diode models:
  – fwd: Forward
  – rev: Reverse
  – brk: Breakdown
  – off[1]

Model parameters for device reference temperature in Spectre

This text describes the use of the tnom, tref and tr model parameters in Spectre with SiMKit devices to set the device reference temperature.

1.Off is not an electrical region, it just states that the user does not know in what state the device is operating

A Simkit device in Spectre has three model parameter aliases for the model reference temperature, tnom, tref and tr. These three parameters can only be used in a model definition, not as instance parameters.

There is no difference in setting tnom, tref or tr. All three parameters have exactly the same effect. The following three lines are therefore completely equivalent:

```
model nmos11020 mos11020 type=n tnom=30
model nmos11020 mos11020 type=n tref=30
model nmos11020 mos11020 type=n tr=30
```

All three lines set the reference temperature for the mos11020 device to 30 C.

Specifying combinations of tnom, tref and tr in the model definition has no use, only the value of the last parameter in the model definition will be used. E.g.:

```
model nmos11020 mos11020 type=n tnom=30 tref=34
```

will result in the reference temperature for the mos11020 device being set to 34 C, tnom=30 will be overridden by tref=34 which comes after it.

When there is no reference temperature set in the model definition (so no tnom, tref or tr is set), the reference temperature of the model will be set to the value of tnom in the options statement in the Spectre input file. So setting:

```
options1 options tnom=23 gmin=1e-15 reltol=1e-12 \
    vabstol=1e-12 iabstol=1e-16
model nmos11020 mos11020 type=n
```

will set the reference temperature of the mos11020 device to 23 C.

When no tnom is specified in the options statement and no reference temperature is set in the model definition, the default reference temperature is set to 27 C.
So the lines:

```
options1 options gmin=1e-15 reltol=1e-12 vabstol=1e-12 \
    iabstol=1e-16
model nmos11020 mos11020 type=n
```

will set the reference temperature of the mos11020 device to 27 C.

The default reference temperature set in the SiMKit device itself is in the Spectre simulator never used. It will always be overwritten by either the default "options tnom", an explicitly set option tnom or by a tnom, tref or tr parameter in the model definition.

C OvervoltageSpecification

Overvoltage warnings in SiMKit

Introduction

Overvoltage flagging is signalling that a (terminal) voltage is outside a specified safe range. A warning will be given when the conditions for giving a warning are fulfilled.

Simple checks for overvoltage have been added to the following models: mos903, mos1100, mos1101, mos1102, mos2002, mos2003, mos3100, mos4000, psp102, psp103.
The checks are done on terminal voltages of the models.

There are many ways to define overvoltage. For a general overvoltage flagging solution Verilog-A should be used.

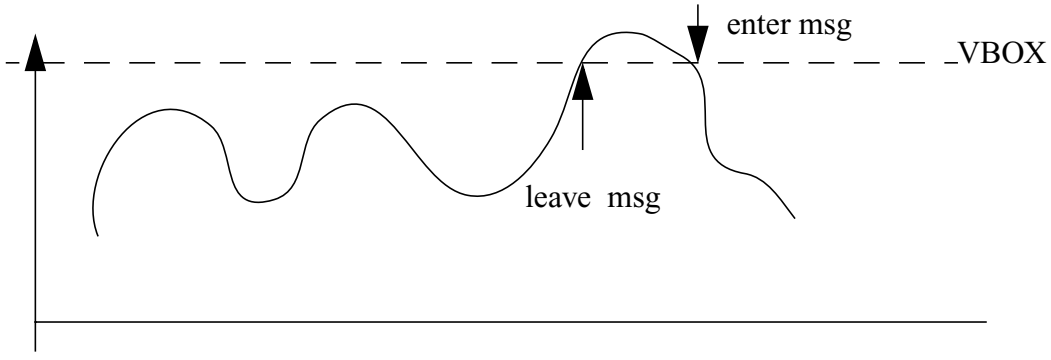
Extra parameters for overvoltage flagging

A set of extra parameters has been added to the mos models mos903, mos1100, mos1101, mos1102, mos2002, mos2003, mos3100, mos4000, psp102, psp103.

Table 26:

Name	Unit	Default	Description
VBOX	V	0.0	Oxide breakdown voltage. Checking will be done if $VBOX > 0$
VBDS	V	0.0	Drain-source breakdown voltage Checking will be done if $VBDS > 0$
TMIN	s	0.0	Ovcheck tmin value

For mos models the safe region is:
$|V_{gs}| < VBOX$ and $|V_{gd}| < VBOX$ and $|V_{ds}| < VBDS$



Ovcheck: two terminal dummy model

A (dummy) two-terminal model ovcheck has been implemented that can be used to check if the voltage between the two terminals is within or without a so called safe region.
The model parameters are:

Name	Unit	Default	Description
VLOW	V	0.0	Lower bound of safe region
VHIGH	V	0.0	Upper bound of safe region Checking will be done when $VHIGH > VLOW$
TMIN	s	0.0	Ovcheck tmin value

For the ovcheck model the safe region is:
$VLOW \le V_{t1} - V_{t2} \le VHIGH$, where t1 is the first and t2 is the second terminal.

Functionality

In Spectre and Pstar

At the end of a DC analysis or in a transient analysis after each time step a check wil be done if the device is inside or outside the safe region.
A warning is given whenever the device enters or leaves the safe region.

In Spectre only

To prevent too many warnings in a Spectre transient analysis the model parameter TMIN has been introduced. If the time between leaving and entering the safe region is less than the TMIN value no warning is given.

Because of the TMIN parameter a warning cannot be issued when leaving the safe region. A warning is given when the device enters the safe region again. This warning includes the time and the voltage when the safe region was exited.At the end of the transient warnings are given for devices that are still out of the safe range.

In Pstar TMIN may be specified as a model parameter, but it will be ignored.

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