HiSIM_HV 2.4.2 User's Manual

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1 LDMOS/HVMOS Structures

HiSIM (Hiroshima-university STARC IGFET Model) is the first complete surface-potential-based MOSFET model for circuit simulation based on the drift-diffusion theory [1], which was originally developed by Pao and Sah [2]. The model has been extended for power MOSFETs by considering the resistance effect explicitly, which is named HiSIM_HV [3].
There are two MOSFET types of structures commonly used for high voltage applications. One is the asymmetrical laterally diffused structure called LDMOS and the other is originally the symmetrical structure, which we distinguish by referring to it as HVMOS. However, the asymmetrical HVMOS structure is also possible. HiSIM_HV is valid for modeling all these structure types [4, 5].
The most important features of LDMOS/HVMOS devices, different from the conventional MOSFET, are originating from the drift region introduced to achieve the sustainability of high voltages. By varying the lengh as well as the dopant concentration of the drift region, various devices with various operating biase conditions are realized as shown in Fig. 1 for the LDMOS structure.

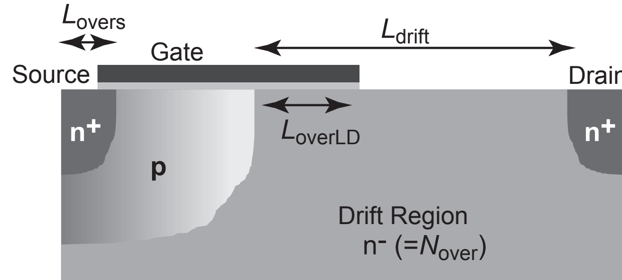

Fig. 1: Schematic of the typical LDMOS structure and device parameters.

A schmatic of the general structures for LDMOS and HVMOS are shown in Fig. 2 for the n-channel case.

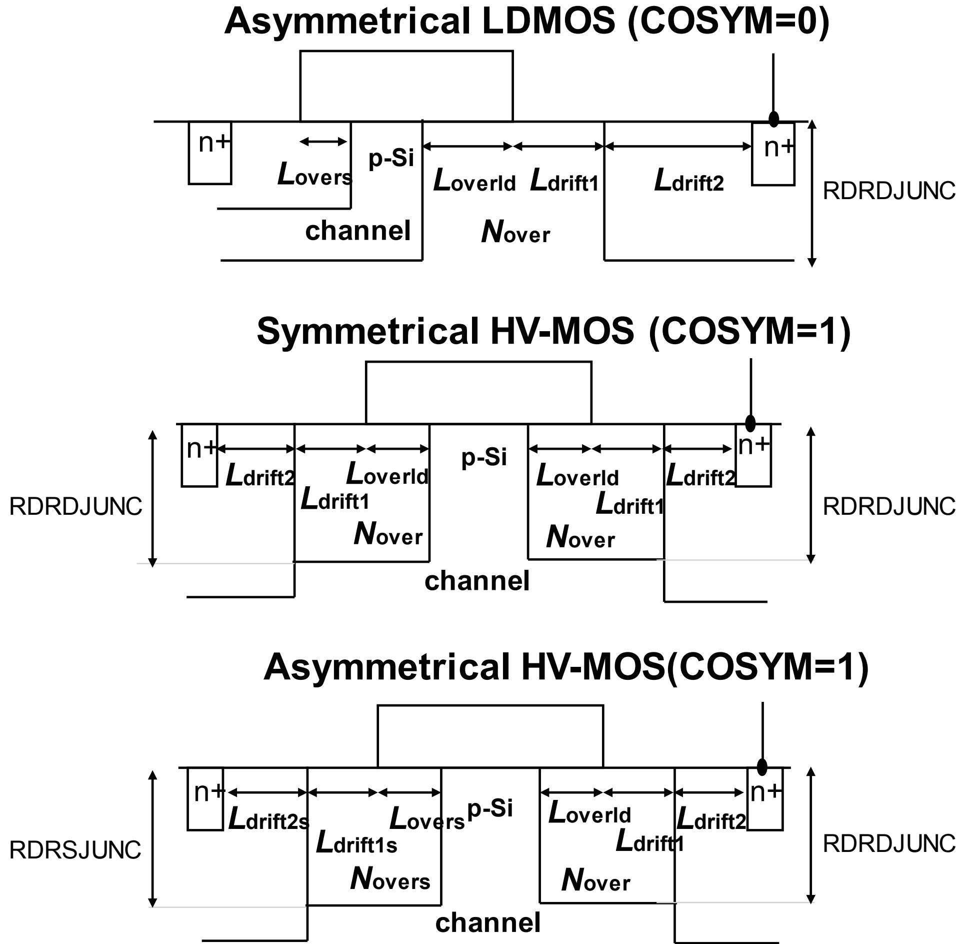

Fig. 2: Device parameters in HiSIM_HV.

To make the structural definition easy, Flag **COSYM** is introduced as shown in Fig. 3. **COSYM**=0 refers to the asymmetrical LDMOS, and all structural parameters have to be determined independently. **COSYM**=1 refers to symmetrical/asymmetrical HVMOS. If parameter values of the source side are given, they are activated. If they are not given, parameter values of the drain side are copied to the source side automatically.

HiSIM_HV 2.4.2 excludes the old resistance model implemented in the HiSIM_HV1 series.

Table 1 summarizes the structural parameters to be given. In case the overlap length **LOVER** is given instead of **LOVERS**, **LOVER** is taken for **LOVERS**. However, it is recommended to give **LOVERS** but not **LOVER**.

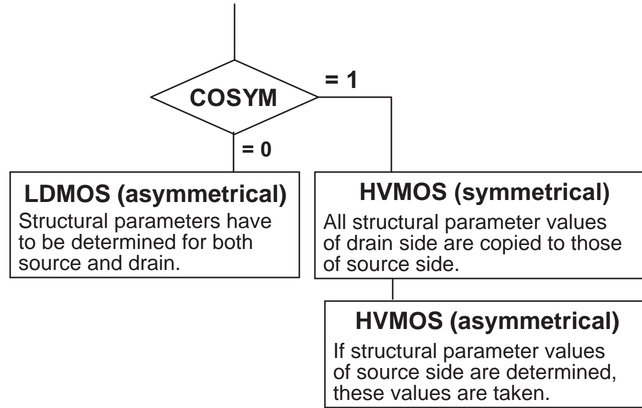

Fig. 3: Device parameters of HiSIM_HV.

HiSIM_HV 2.4.2 includes the substrate node V_{sub} as schematically shown in Fig. 4, where model parameters **DDRIFT** and **NSUBSUB** are newly introduced for D_{drift} and N_{subsub}, respectively. The node inclusion is done by selecting Flag **COSUBNODE**=1 as the 5th node.

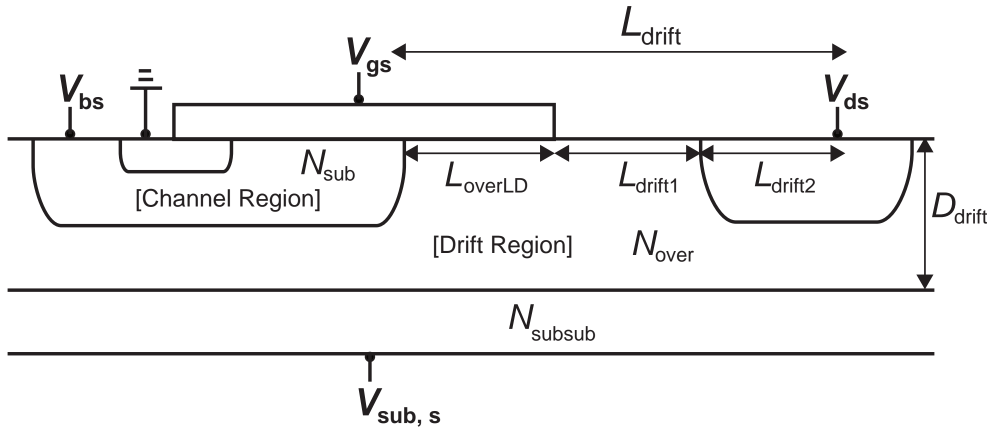

Fig. 4: Schematic of a LDMOS with the substrate node $V_{\mathrm{sub,s}}$.

Table 1: HiSIM_HV 2.4.2 model parameters introduced.

	structure	source	drain
COSYM=0	**LDMOS**	**LOVERS** **RS**	**LOVERLD** **LDRIFT1** **LDRIFT2** **NOVER** **RD** **RDRDJUNC**
COSYM=1	**symmetrical HVMOS**		**LOVERLD** **LDRIFT1** **LDRIFT2** **NOVER** **RD** **RDRDJUNC**
COSYM=1	**asymmetrical HVMOS**	**LOVERS** **LDRIFT1S** **LDRIFT2S** **NOVERS** **RS** **RDRSJUNC**	**LOVERLD** **LDRIFT1** **LDRIFT2** **NOVER** **RD** **RDRDJUNC**

The HiSIM_HV model parameters introduced in section 1 are summarized in Table 2.

Table 2: HiSIM_HV 2.4.2 model parameters introduced in section 1 of this manual.

LOVER	overlap length at source side for **LOVERS**
LOVERLD	overlap length at drain, and at source, if **COSYM**=1
LDRIFT1	length of lightly doped drift region at drain, and at source, if **COSYM**=1
LDRIFT2	length of heavily doped drift region at drain, and at source, if **COSYM**=1
NOVER	impurity concentration of **LOVERLD** at drain, and at source, if **COSYM**=1
LOVERS	overlap length at source
LDRIFT1S	length of lightly doped drift region at source, if **COSYM**=1 and the value is determined
LDRIFT2S	length of heavily doped drift region at source, if **COSYM**=1 and the value is determined
NOVERS	impurity concentration of **LOVERS** at source, if **COSYM**=1 and the value is determined
VBSMIN	minimum $V_{\rm bs}$ voltage applied: No need and inactivated.
DDRIFT	depth of the drift region
NSUBSUB	impurity concentration of the substrate required for $V_{\rm sub}$ dependence

2 Basic Concept

HiSIM_HV solves the potential distribution along the surface by solving the Poisson equation iteratively including the resistance effect in the drift region, where the bias dependence of the resistance is considered. The HiSIM compact model determines the complete potential distribution along the device including the surface potential at the source side ϕ_{S0}, the potential at the pinch-off point ϕ_{SL}, the potential at the channel/drain junction, $\phi_S(\Delta L)$, and the final potential value at the drain contact $\phi_{S0} + V_{ds}$ as shown in Fig. 5. The potential V_{dseff} is the potential value which mostly determines the device characteristics. This potential node is considered explicitly in addition to the node potential of V_{ds}. Advanced version concealing the internal node to speed up the simulation has been developed in parallel [6].

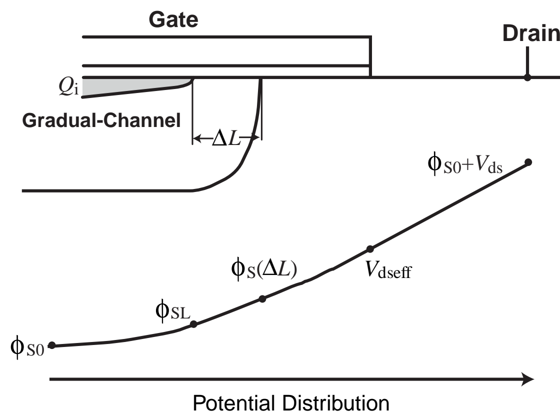

Fig. 5: Schematic of the surface potential distribution in the channel at the drain side of the LDMOS device structure.

3 Definition of Device Size

The effective channel length L_{eff} and width W_{eff} are calculated from the gate length L_{gate} and width W_{gate}, where L_{gate} and width W_{gate} deviate from the gate drawn length and width

$$L_{\text{gate}} = L_{\text{drawn}} + \mathbf{XL} \tag{1}$$

$$W_{\text{gate}} = \frac{W_{\text{drawn}}}{\mathbf{NF}} + \mathbf{XW} \tag{2}$$

$$L_{\text{poly}} = L_{\text{gate}} - 2 \cdot \frac{\mathbf{LL}}{(L_{\text{gate}} + \mathbf{LLD})^{\mathbf{LLN}}} \tag{3}$$

$$W_{\text{poly}} = W_{\text{gate}} - 2 \cdot \frac{\mathbf{WL}}{(W_{\text{gate}} + \mathbf{WLD})^{\mathbf{WLN}}} \tag{4}$$

$$L_{\text{eff}} = L_{\text{poly}} - \mathbf{XLD} - \mathbf{XLDLD} \tag{5}$$

$$W_{\text{eff}} = W_{\text{poly}} - 2 \cdot \mathbf{XWD} \tag{6}$$

$$W_{\text{eff,LD}} = W_{\text{poly}} - 2 \cdot \mathbf{XWDLD} \tag{7}$$

$$W_{\text{effc}} = W_{\text{poly}} - 2 \cdot \mathbf{XWDC} \tag{8}$$

$$\tag{9}$$

where **XLD**/**XLDLD** and **XWD** account for the overlaps of source/drain contact and the gate oxide as shown in Fig. 6. Widening of W_{eff} due to the extension of electric-force line of the drift region is considered by **XWDLD**. The model parameter **XWDC** is introduced to describe the different width dependence of capacitacnes from currents. If the value is not given, the same value as **XWD** is taken. **LL**, **LLD**, **LLN**, **WL**, **WLD**, and **WLN** are further model parameters for including L_{gate} or W_{gate} dependencies on L_{eff} and W_{eff}.

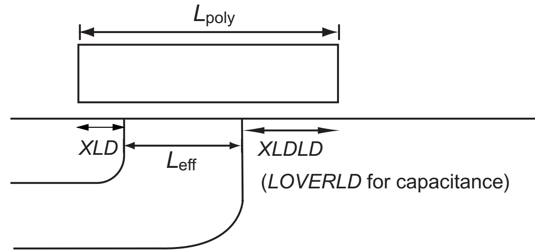

Fig. 6: Cross section of the device.

The HiSIM model parameters introduced in section 3 are summarized in Table 3.

Table 3: HiSIM model parameters introduced in section 3 of this manual. $*$ and # indicate minor parameters and # an instance parameter, respectively.

#NF	number of gate fingers
XL	difference between real and drawn gate length
XW	difference between real and drawn gate width
XLD	gate-overlap in length at source side
XLDLD	gate-overlap in length at drain side
XWD	gate-overlap in width
XWDLD	widening of drift width
XWDC	gate-overlap in width for capacitance calculation
LL	coefficient of gate length modification
LLD	coefficient of gate length modification
LLN	coefficient of gate length modification
WL	coefficient of gate width modification
WLD	coefficient of gate width modification
WLN	coefficient of gate width modification

4 Charges

By applying the Gauss law, the charge density induced in the channel is derived from the Poisson equation [7]:

$$
\begin{aligned}
-(Q_{\mathrm{B}} + Q_{\mathrm{I}}) &= C_{\mathrm{ox}}\big(V'_{\mathrm{G}} - \phi_{\mathrm{S}}(y)\big) \\
&= \sqrt{\frac{2\epsilon_{\mathrm{Si}} q N_{\mathrm{sub}}}{\beta}} \Big[\exp\big\{-\beta(\phi_{\mathrm{S}}(y) - V_{\mathrm{bs}})\big\} + \beta(\phi_{\mathrm{S}}(y) - V_{\mathrm{bs}}) - 1 \\
&\quad + \frac{n_{\mathrm{p0}}}{p_{\mathrm{p0}}}\Big\{\exp\big(\beta(\phi_{\mathrm{S}}(y) - \phi_{\mathrm{f}}(y))\big) - \exp\big(\beta(V_{\mathrm{bs}} - \phi_{\mathrm{f}}(y))\big)\Big\}\Big]^{\frac{1}{2}}
\end{aligned}
$$

$$C_{\mathrm{ox}} = \frac{\epsilon_0 \mathbf{KAPPA}}{\mathbf{TOX}} \tag{10}$$

$$V'_{\mathrm{G}} = V_{\mathrm{gs}} - \mathbf{VFBC} + \Delta V_{\mathrm{th}} \tag{11}$$

$$\beta = \frac{q}{kT} \tag{12}$$

where **VFBC** is the flat-band voltage, **TOX** is the physical gate-oxide thickness, and ΔV_{th} is the threshold voltage shift in comparison to the threshold voltage of a long-channel transistor [11]. ϵ_0 and **KAPPA** are permittivities in vacuum and in the gate dielectric, respectively. The electron charge is denoted by q, and ϵ_{Si} and N_{sub} are the silicon permittivity and the substrate impurity concentration, respectively. The Boltzmann constant and the lattice temperature in Kelvin are k and T, respectively. The quasi-Fermi potential $\phi_{\mathrm{f}}(y)$ preserves the following relationship:

$$\phi_{\mathrm{f}}(L_{\mathrm{eff}}) - \phi_{\mathrm{f}}(0) = V_{\mathrm{ds,eff}} \tag{13}$$

where $V_{\mathrm{ds,eff}}$ is introduced to fit measured transition characteristics of the channel conductance g_{ds} between the linear region and the saturation region to compensate for insufficiencies of the charge-sheet approximation as

$$V_{\mathrm{ds,eff}} = \frac{V_{\mathrm{ds}}}{\left[1 + \left(\frac{V_{\mathrm{ds}}}{V_{\mathrm{ds,sat}}}\right)^{\Delta}\right]^{\frac{1}{\Delta}}} \tag{14}$$

where

CODDLT=0 :

$$\Delta = \frac{\mathbf{DDLTMAX} \cdot T1}{\mathbf{DDLTMAX} + T1} + 1 \tag{15}$$

$$T1 = \mathbf{DDLTSLP} \cdot L_{\mathrm{gate}} \cdot 10^6 + \mathbf{DDLTICT} \tag{16}$$

CODDLT=1 (default) :

$$\Delta = \frac{\mathbf{DDLTMAX} \cdot T1}{\mathbf{DDLTMAX} + T1} + \mathbf{DDLTICT} \tag{17}$$

$$T1 = \mathbf{DDLTSLP} \cdot L_{\mathrm{gate}} \cdot 10^6 \tag{18}$$

If higher-order derivatives become non-smooth, please increase the **DDLTICT** value. It could be happened for short-channel length, depends on parameter values.
And $V_{\mathrm{ds,sat}}$ is calculated by solving the Poisson equation analytically by neglecting the inversion carrier density [1].

$$V_{\mathrm{ds,sat}} = \left[V'_{\mathrm{G}} + \frac{qN_{\mathrm{sub}}\epsilon_{\mathrm{Si}}}{{C_{\mathrm{ox}}}^2} \{ 1 - \sqrt{1 + 2\frac{{C_{\mathrm{ox}}}^2}{qN_{\mathrm{sub}}\epsilon_{\mathrm{Si}}} \{ V'_{\mathrm{G}} - \frac{1}{\beta} - V_{\mathrm{bs}} \}} \} \right] \tag{19}$$

The electron concentration at equilibrium condition n_{p0} is

$$n_{\mathrm{p0}} = \frac{n_{\mathrm{i}}^2}{p_{\mathrm{p0}}} \tag{20}$$

where the intrinsic carrier concentration n_{i} is

$$n_{\mathrm{i}} = n_{\mathrm{i0}} T^{\frac{3}{2}} \exp\left(-\frac{E_{\mathrm{g}}}{2q}\beta \right) \tag{21}$$

p_{p0} is approximated to be N_{sub}, and E_{g} describes the temperature dependence of the bandgap (see section 14).

Analytical equations for Q_{B} and Q_{I} are derived as a function of ϕ_{S0} and ϕ_{SL}. The final equations for Q_{B}, Q_{I}, and Q_{D} are given in Eqs. (22)- (24).

$$\begin{aligned} Q_{\mathrm{B}} = &- \frac{\mu(W_{\mathrm{eff}} \cdot \mathbf{NF})^2}{I_{\mathrm{ds}}} \Bigg[const0\, C_{\mathrm{ox}} (V_{\mathrm{G}} - \mathbf{VFBC}) \frac{1}{\beta}\frac{2}{3} \Big[\{ \beta(\phi_{\mathrm{S}} - V_{\mathrm{bs}}) - 1 \}^{\frac{3}{2}} \Big]_{\phi_{\mathrm{S0}}}^{\phi_{\mathrm{SL}}} \\ &- const0\, C_{\mathrm{ox}} \frac{1}{\beta}\frac{2}{3} \Big[\phi_{\mathrm{S}} \{ \beta(\phi_{\mathrm{S}} - V_{\mathrm{bs}}) - 1 \}^{\frac{3}{2}} \Big]_{\phi_{\mathrm{S0}}}^{\phi_{\mathrm{SL}}} + const0\, C_{\mathrm{ox}} \frac{1}{\beta}\frac{2}{3}\frac{1}{\beta}\frac{2}{5} \Big[\{ \beta(\phi_{\mathrm{S}} - V_{\mathrm{bs}}) - 1 \}^{\frac{5}{2}} \Big]_{\phi_{\mathrm{S0}}}^{\phi_{\mathrm{SL}}} \\ &- const0^2 \frac{1}{\beta}\frac{1}{2} \big[\beta^2(\phi_{\mathrm{SL}} - V_{\mathrm{bs}})^2 - 2\beta(\phi_{\mathrm{SL}} - V_{\mathrm{bs}}) + 1 - \beta^2(\phi_{\mathrm{S0}} - V_{\mathrm{bs}})^2 + 2\beta(\phi_{\mathrm{S0}} - V_{\mathrm{bs}}) - 1 \big] \Bigg] \\ &- \frac{1}{\beta} \frac{\mu(W_{\mathrm{eff}} \cdot \mathbf{NF})^2}{I_{\mathrm{ds}}} \Big[const0\, C_{\mathrm{ox}} \frac{1}{\beta}\frac{2}{3} \{ \beta(\phi_{\mathrm{S}} - V_{\mathrm{bs}}) - 1 \}^{\frac{3}{2}} + \frac{1}{2} const0^2 \beta \phi_{\mathrm{S}} \Big]_{\phi_{\mathrm{S0}}}^{\phi_{\mathrm{SL}}} \end{aligned} \tag{22}$$

Here $const0$ is defined as

$$const0 = \sqrt{\frac{2\epsilon_{\mathrm{Si}} q N_{\mathrm{sub}}}{\beta}}$$

while μ and I_{ds} are the carrier mobility and the drain current, respectively [8, 9].

$$Q_{\mathrm{I}} = - WLC_{\mathrm{ox}}(VgVt)\frac{2}{3}\left(\frac{1 + \alpha + \alpha^2}{1 + \alpha} \right) \tag{23}$$

$$Q_{\mathrm{D}} = Q_{\mathrm{I}} \left(\frac{3}{5} - \frac{1}{5} \frac{1 + 2\alpha}{(1 + \alpha)(1 + \alpha + \alpha^2)} \right) \tag{24}$$

where the surface-potential-based description derives

$$\alpha = 1 - \frac{(1+\delta)(\phi_{\rm SL} - \phi_{\rm S0})}{VgVt} \tag{25}$$

$$VgVt = V_{\rm gs} - \left(\mathbf{VFBC} + \phi_{\rm S0} + \frac{const0}{C_{\rm ox}} BPS0^{\frac{1}{2}} \right) \tag{26}$$

$$\delta = C0Cox \frac{4}{3} \frac{1}{\beta} \frac{(BPSL^{\frac{3}{2}} - BPS0^{\frac{3}{2}})}{(\phi_{\rm SL} - \phi_{\rm S0})^2} - C0Cox \frac{2}{\beta} \frac{(BPSL^{\frac{1}{2}} - BPS0^{\frac{1}{2}})}{(\phi_{\rm SL} - \phi_{\rm S0})^2} - 2C0Cox \frac{BPS0^{\frac{1}{2}}}{(\phi_{\rm SL} - \phi_{\rm S0})} \tag{27}$$

and

$$\begin{aligned}
C0Cox &= \frac{const0}{C_{\rm ox}} \\
BPSL^{\frac{1}{2}} &= \sqrt{\beta(\phi_{\rm SL} - V_{\rm bs}) - 1} \\
BPS0^{\frac{1}{2}} &= \sqrt{\beta(\phi_{\rm S0} - V_{\rm bs}) - 1} \\
BPSL^{\frac{3}{2}} &= (BPSL^{\frac{1}{2}})^3 \\
BPS0^{\frac{3}{2}} &= (BPS0^{\frac{1}{2}})^3
\end{aligned} \tag{28}$$

The HiSIM model parameters introduced in section 4 are summarized in Table 4.

Table 4: HiSIM model parameters introduced in section 4 of this manual. $*$ indicates minor parameters.

VFBC	flat-band voltage
VBI	built-in potentail
TOX	physical gate-oxide thickness
KAPPA	dielectric constant of gate dielectric
***DDLTMAX**	smoothing coefficient for $V_{\rm ds}$
***DDLTSLP**	$L_{\rm gate}$ dependence of smoothing coefficient
***DDLTICT**	$L_{\rm gate}$ dependence of smoothing coefficient

5 Drain Current

Under the gradual-channel approximation together with approximations of an idealized gate structure and uniform channel doping, the equation for the drain current $I_{\rm ds}$ is written [7, 10]

$$I_{\rm ds} = \frac{W_{\rm eff} \cdot \mathbf{NF}}{L_{\rm eff}} \cdot \mu \cdot \frac{I_{\rm dd}}{\beta} \tag{29}$$

$$\begin{aligned} I_{\rm dd} = & \; C_{\rm ox}(\beta V'_{\rm G} + 1)(\phi_{\rm SL} - \phi_{\rm S0}) - \frac{\beta}{2} C_{\rm ox}(\phi_{\rm SL}^2 - \phi_{\rm S0}^2) \\ & - \frac{2}{3} const0 \Big[\big\{\beta(\phi_{\rm SL} - V_{\rm bs}) - 1\big\}^{\frac{3}{2}} - \big\{\beta(\phi_{\rm S0} - V_{\rm bs}) - 1\big\}^{\frac{3}{2}} \Big] \\ & + const0 \Big[\big\{\beta(\phi_{\rm SL} - V_{\rm bs}) - 1\big\}^{\frac{1}{2}} - \big\{\beta(\phi_{\rm S0} - V_{\rm bs}) - 1\big\}^{\frac{1}{2}} \Big] \end{aligned} \tag{30}$$

The above description includes the further approximation that the mobility μ is independent of position along the channel y.

6 Threshold Voltage Shift

Different from the drift approximation, the drift-diffusion approximation does not require a threshold voltage parameter $V_{\rm th}$ for describing device performances. The MOSFET device parameters such as the oxide thickness $T_{\rm ox}$ and the substrate doping concentration $N_{\rm subc}$ determine the complete MOSFET behavior including the subthreshold characteristics automatically and consistently. However, HiSIM derives many detailed informations on the MOSFET fabrication technology with the $V_{\rm th}$ changes from a long-channel transistor ($\Delta V_{\rm th}$) as a function of gate length ($L_{\rm gate}$). The modeled $\Delta V_{\rm th}$ is incorporated in the $\phi_{\rm S}$ iteration as can be seen in Eq. (11), and can be viewed as consisting of two main effects or components:

(I) the short-channel effect: $\Delta V_{\rm th,SC}$

(II) the reverse-short-channel effect: $\Delta V_{\rm th,R}$ and $\Delta V_{\rm th,P}$

The separation into these two components ($\Delta V_{\rm th} = \Delta V_{\rm th,SC} + \Delta V_{\rm th,R}$ (or $\Delta V_{\rm th,P}$)) is schematically shown in Fig. 7.

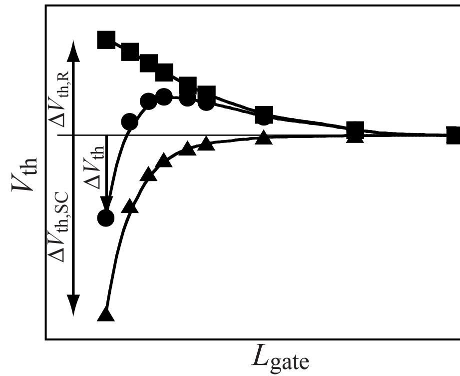

Fig. 7: Schematic plot of the separation of $V_{\rm th}$ into the contributions of the short-channel and the reverse-short-channel effect.

6.1 (I) Short-Channel Effects

All observed phenomena are caused by the lateral-electric-field contribution in the MOSFET channel, which is important even at threshold condition with small $V_{\rm ds}$. Thus $\Delta V_{\rm th,SC}$ can be written as a function of the lateral electric field E_y by applying the Gauss law. A parabolic potential distribution along the channel is approximated, which results in a position independent gradient of the lateral electric field $\frac{dE_y}{dy}$ [11]

$$\Delta V_{\rm th,SC} = \frac{\epsilon_{\rm Si}}{C_{\rm ox}} W_{\rm d} \frac{dE_y}{dy} \tag{31}$$

where $W_{\rm d}$ is the depletion-layer thickness written as

$$W_{\rm d} = \sqrt{\frac{2\epsilon_{\rm Si}(2\Phi_{\rm B} - V_{\rm bs})}{qN_{\rm sub}}} \tag{32}$$

$$2\Phi_{\rm B} = \frac{2}{\beta} \ln\left(\frac{N_{\rm sub}}{n_{\rm i}}\right) \tag{33}$$

where $n_{\rm i}$ is the intrinsic carrier density. $\frac{dE_y}{dy}$ is derived with model parameters in the form

$$\frac{dE_y}{dy} = \frac{2(\mathbf{VBI} - 2\Phi_{\rm B})}{(L_{\rm gate} - \mathbf{PARL2})^2}\left(\mathbf{SC1} + \mathbf{SC2} \cdot V_{\rm ds} \cdot \{1 + \mathbf{SC4} \cdot (2\Phi_{\rm B} - V_{\rm bs})\} + \mathbf{SC3} \cdot \frac{2\Phi_{\rm B} - V_{\rm bs}}{L_{\rm gate}}\right) \tag{34}$$

VBI and **PARL2** represent the built-in potential and the depletion width of the junction vertical to the channel, respectively. $V'_{\rm G}$ and $const0$ were defined in Eqs. (11) and (23), respectively. The model parameter **SC1** determines the threshold voltage shift for small $V_{\rm ds}$ and $V_{\rm bs}$, and is expected to be unity. If measured $V_{\rm th}$ is plotted as a function of $V_{\rm ds}$, it shows nearly a linear dependence. The gradient is proportional to **SC2**. **SC3** implements a correction of the charge-sheet approximation as well as the impurity-profile gradient along the vertical direction, and is expected to be small. **PTHROU**, describing the increase of the subthreshold swing for short-channel transistors, was deleted and was modeled as the punchthrough effect.

6.2 (II) Reverse-Short-Channel Effects

The reverse-short-channel effect is categorized into resulting from two physical MOSFET properties:

(i) Impurity concentration inhomogeneity in the direction vertical to the channel (vertical channel inhomogeneity)
(obvious in the retrograded implantation): $\Delta V_{\rm th,R}$

(ii) Impurity concentration inhomogeneity in the direction parallel to the channel (lateral channel inhomogeneity)
(obvious in the pocket implantation): $\Delta V_{\rm th,P}$

(i) Impurity concentration inhomogeneity in the direction vertical to the channel (Retrograded Implantation)

The above model parameters **SC3** and **SCP3** (see in 6.2. (ii)) can be successfully used, if the inhomogeneity is not extremely large.
For cases where the inhomogeneity is large or where positive $V_{\rm bs}$ is applied, deviation from the linearity of $V_{\rm th}$ as a function of $\sqrt{2\Phi_{\rm B} - V_{\rm bs}}$ is modeled with two fitting parameters **BS1** and **BS2** as

$$Q_{\rm Bmod} = \sqrt{2q \cdot N_{\rm sub} \cdot \epsilon_{Si} \cdot \left(2\Phi_{\rm B} - V_{\rm bs} - \frac{\mathbf{BS1}}{\mathbf{BS2} - V_{\rm bs}}\right)} \tag{35}$$

where **BS1** represents the strength of the deviation and **BS2** is the starting value of $V_{\rm bs}$ where the deviation becomes visible. This $Q_{\rm Bmod}$ is incorporated into the $\Delta V_{\rm th}$ desription as be seen in Eq. (37).

(ii) Impurity concentration inhomogeneity in the lateral direction parallel to the channel (Pocket Implantation)

The model equations for the $V_{\rm th}$ shift due to the pocket implant are:

$$\Delta V_{\rm th,P} = (V_{\rm th,R} - V_{\rm th0})\frac{\epsilon_{\rm Si}}{C_{\rm ox}} W_{\rm d} \frac{dE_{y,\rm P}}{dy} \tag{36}$$

$$V_{\rm th,R} = \mathbf{VFBC} + 2\Phi_{\rm B} + \frac{Q_{\rm Bmod}}{C_{\rm ox}} + \frac{1}{\beta}\log\left(\frac{N_{\rm subb}}{N_{\rm subc}}\right) \tag{37}$$

$$V_{\rm th0} = \mathbf{VFBC} + 2\Phi_{\rm BC} + \frac{\sqrt{2qN_{\rm subc}\epsilon_{\rm Si}(2\Phi_{\rm BC} - V_{\rm bs})}}{C_{\rm ox}} \tag{38}$$

$$\frac{dE_{y,\rm P}}{dy} = \frac{2(\mathbf{VBI} - 2\Phi_{\rm B})}{\mathbf{LP}^2}\left(\mathbf{SCP1} + \mathbf{SCP2}\cdot V_{\rm ds} + \mathbf{SCP3}\cdot\frac{2\Phi_{\rm B} - V_{\rm bs}}{\mathbf{LP}}\right) \tag{39}$$

$$N_{\rm subb} = 2\cdot\mathbf{NSUBP} - \frac{(\mathbf{NSUBP} - N_{\rm subc})\cdot L_{\rm gate}}{\mathbf{LP}} - N_{\rm subc} \tag{40}$$

where $N_{\rm subc}$ is the substrate impurity concentration as defined in Eq. (79). The parameters **SCP1 - SCP3** describe the short-channel effect caused by the potential minimum at the higher impurity concentration of the pocket. $2\Phi_{\rm BC}$ is the potential giving threshold condition with $N_{\rm subc}$ and $2\Phi_{\rm B}$ is the equivalent potential with $N_{\rm sub}$

$$\Phi_{\rm BC} = \frac{2}{\beta}\ln\left(\frac{N_{\rm subc}}{n_{\rm i}}\right) \tag{41}$$

$$\Phi_{\rm B} = \frac{2}{\beta}\ln\left(\frac{N_{\rm sub}}{n_{\rm i}}\right) \tag{42}$$

$$N_{\rm sub} = \frac{N_{\rm subc}(L_{\rm gate} - \mathbf{LP}) + \mathbf{NSUBP}\cdot\mathbf{LP}}{L_{\rm gate}} \tag{43}$$

As defined in Eq. (43), $N_{\rm sub}$ is replaced to the averaged impurity concentration in the channel and $N_{\rm subb}$ is introduced, beginning from channel lengths where pockets at source and drain start to overlap.
As $V_{\rm ds}$ approaches zero, the $V_{\rm th}$ dependence on $V_{\rm ds}$ deviates from linearity and $V_{\rm th}$ increases drastically as shown schematically in Fig. 8. This is modeled with two model parameters **SCP21** and **SCP22** as

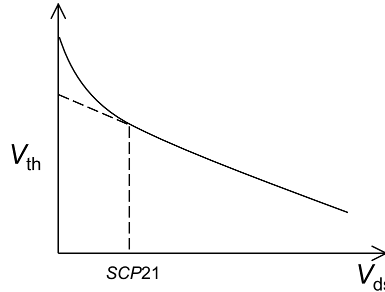

Fig. 8: Threshold voltage as a function of $V_{\rm ds}$. The deviation from linearity for small $V_{\rm ds}$ is modeled with parameters **SCP21** and **SCP22**.

$$\Delta V_{\rm th,P} = \Delta V_{\rm th,P} - \frac{\mathbf{SCP22}}{(\mathbf{SCP21} + V_{\rm ds})^2} \tag{44}$$

where **SCP21** determines the $V_{\rm ds}$ value at which $V_{\rm th}$ starts to deviate from linearity as a function of $V_{\rm ds}$. The parameter **SCP22** determines the gradient of this deviation.

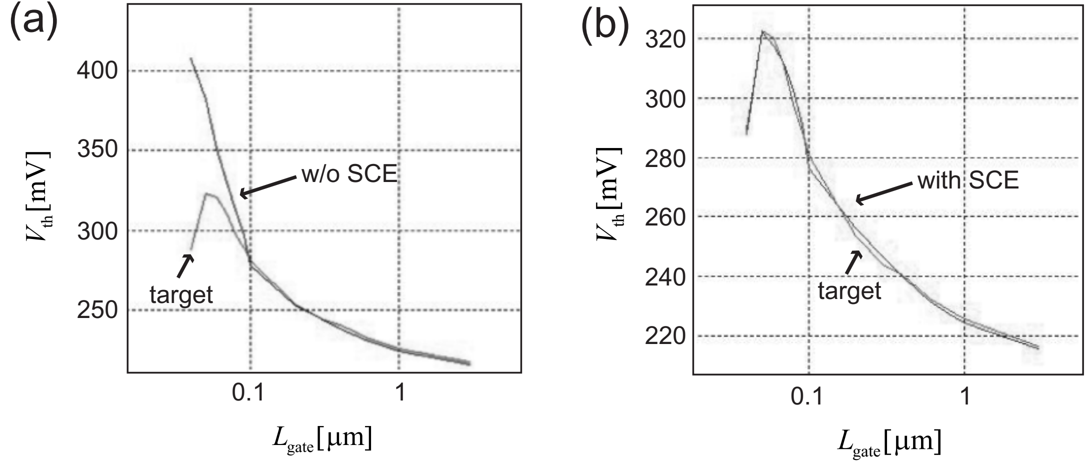

Fig. 9: Comparison of measurements and pocket-implant model for $V_{\rm th}$ as a function of $L_{\rm gate}$. Results (a) with and (b) without short-channel effects (SCE) are shown.

$V_{\rm th,R}$ and $V_{\rm th0}$, defined in Eqs. (37) and (38), are the threshold voltages for the cases with and without pocket-implant, respectively. The overlap start of source and drain pockets causes a steep increase of $V_{\rm th}$ as a function of decreasing $L_{\rm gate}$. This effect enables to extract **LP** from measurements. Fig. 9 compares the $V_{\rm th}$-$L_{\rm gate}$ characteristics of the developed pocket-implant model with and without inclusion of the short-channel effects (SCE). The steep increase at $L_{\rm gate}$=0.1μm in Fig. 9a means the starting of the pocket overlap, where **LP**=0.05μm.

In some cases the pocket profile cannot be described by the single linearly decreasing form, but provides extensive tails as schematically shown in Fig. 10. Therefore, two model parameters **NPEXT** and **LPEXT** are introduced to model the pocket tails as

$$N_{\rm sub} = N_{\rm sub} + \frac{\mathbf{NPEXT} - N_{\rm subc}}{\left(\frac{1}{\mathbf{xx}} + \frac{1}{\mathbf{LPEXT}}\right) L_{\rm gate}} \tag{45}$$

where

$$\mathbf{xx} = 0.5 \cdot L_{\rm gate} - \mathbf{LP}\ . \tag{46}$$

NPEXT is the maximum concentration of the pocket tail and **LPEXT** describes the tail extension characteristics. Usually strong pocket implantation induces a vertical impurity distribution at the same time. For fitting the measured results in such cases it is recommended to use the parameter **SCP3** together with parameters **BS1** and **BS2**.

The HiSIM model parameters introduced in section 6 are summarized in Table 5.

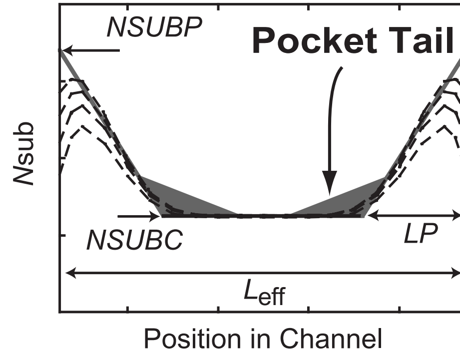

Fig. 10: Modeled pocket tail with **NPEXT** and **LPEXT**.

Table 5: HiSIM model parameters introduced in section 6 of this manual. ∗ indicates minor parameters.

VBI	built-in potential
PARL2	depletion width of channel/contact junction
SC1	magnitude of short-channel effect
SC2	V_{ds} dependence of short-channel effect
∗**SC3**	V_{bs} dependence of short-channel effect
∗**SC4**	V_{bs} dependence of short-channel effect
NSUBP	maximum pocket concentration
LP	pocket penetration length
∗**BS1**	body-coefficient modification due to impurity profile
∗**BS2**	body-coefficient modification due to impurity profile
SCP1	magnitude of short-channel effect due to pocket
SCP2	V_{ds} dependence of short-channel due to pocket
∗**SCP3**	V_{bs} dependence of short-channel effect due to pocket
∗**SCP21**	short-channel-effect modification for small V_{ds}
∗**SCP22**	short-channel-effect modification for small V_{ds}
∗**NPEXT**	maximum concentration of pocket tail
∗**LPEXT**	extension length of pocket tail

7 Short-Channel Effects

7.1 Punchthrough Effect

The origin of the punchthrough effect is the bipolar effect through source, substrate, and drain.The effect is described by a power function of the potential difference

$$POTENTIAL = (\mathbf{VBI} - \phi_{\mathrm{S0}})^{\mathbf{PTP}} \tag{47}$$

The final drain current I_{ds} is written

$$\begin{aligned} I_{\mathrm{ds}} &= I_{\mathrm{ds}} + PUNCH \\ PUNCH &= \frac{W_{\mathrm{eff}} \cdot \mathbf{NF}}{L_{\mathrm{eff}}} \frac{\mu}{\beta} \cdot (\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}) \\ &\left\{ C_{\mathrm{ox}} \cdot \beta \frac{\mathbf{PTL}}{(L_{\mathrm{gate}} \cdot 10^6)^{\mathbf{PTLP}}} \cdot POTENTIAL \cdot \left(1 + \mathbf{PT2} \cdot V_{\mathrm{ds}} + \frac{\mathbf{PT4} \cdot (\phi_{\mathrm{S0}} - V_{\mathrm{bs}})}{(L_{\mathrm{gate}} \cdot 10^6)^{\mathbf{PT4P}}} \right) \right\} \end{aligned} \tag{48}$$

where model parameters $\mathbf{PTL}, \mathbf{PTLP}, \mathbf{PT2}$, $\mathbf{PT4}$, and $\mathbf{PT4P}$ are introduced.

7.2 Channel Conductance

The high field under the saturation condition causes the pinch-off region and the current flows away from the surface. This effect is considered as the lateral-field-induced charge for the capacitacne (see section 16). The simplified formulation is applied to consider the effect as

$$\begin{aligned} I_{\mathrm{ds}} &= I_{\mathrm{ds}} + \frac{W_{\mathrm{eff}} \cdot \mathbf{NF}}{L_{\mathrm{eff}}} \frac{\mu}{\beta} \cdot (\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}) \cdot CONDUCTANCE \\ CONDUCTANCE &= C_{\mathrm{ox}} \cdot \beta \frac{\mathbf{GDL}}{(L_{\mathrm{gate}} \cdot 10^6 + \mathbf{GDLD} \cdot 10^6)^{\mathbf{GDLP}}} \cdot V_{\mathrm{ds}} \end{aligned} \tag{49}$$

The HiSIM model parameters introduced in section 7 are summarized in Table 6.

Table 6: HiSIM model parameters introduced in section 7 of this manual. $*$ indicates minor parameters.

$*$**PTL**	strength of punchthrough effect
$*$**PTLP**	channel-length dependence of punchthrough effect
$*$**PTP**	strength of punchthrough effect
$*$**PT2**	V_{ds} dependence of punchthrough effect
$*$**PT4**	V_{bs} dependence of punchthrough effect
$*$**PT4P**	V_{bs} dependence of punchthrough effect
$*$**GDL**	strength of high-field effect
$*$**GDLP**	channel-length dependence of high-field effect
$*$**GDLD**	channel-length dependence of high-field effect

8 Depletion Effect of the Gate Poly-Si

Carrier depletion in the gate poly-Si near the gate-oxide interface starts after the formation of the inversion layer in the substrate as shown in Fig. 11.

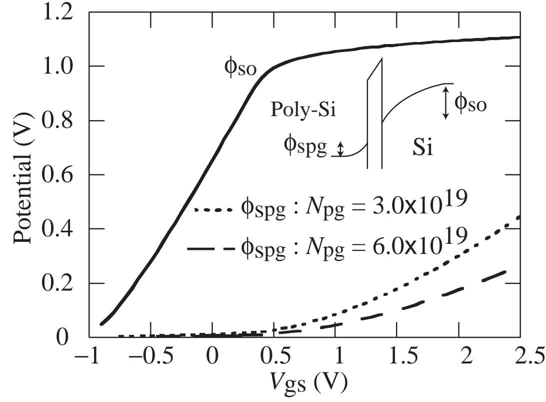

Fig. 11: Simulated surface potential at the source side (ϕ_{S0}) as a function of V_{gs}. The poly-depletion potential is also shown for two doping concentrations N_{pg} in the poly-Si.

To eliminate the necessary iteration procedure for the circuit-simulation application, the potential drop within the poly-Si ϕ_{Spg} is approximated as a function of V_{gs} and V_{ds} by the simple formula of Eq. (50), and is included in the ΔV_{th} calculation as a potential drop of V_{gs}.

$$\phi_{Spg} = \mathbf{PGD1}\left(1 + \frac{1}{L_{gate} \cdot 10^6}\right)^{\mathbf{PGD4}} \exp\left(\frac{V_{gs} - \mathbf{PGD2}}{V}\right) \tag{50}$$

The HiSIM model parameters introduced in section 8 are summarized in Table 7.

Table 7: HiSIM model parameters introduced in section 8 of this manual. $*$ indicates a minor parameter.

Parameter	Description
PGD1	strength of poly depletion
PGD2	threshold voltage of poly depletion
$*$**PGD4**	L_{gate} dependence of poly depletion

9 Quantum-Mechanical Effects

The main quantum-mechanical phenomenon, which has to be included into a MOSFET model for circuit simulation, is the repulsion of the channel's carrier-density peak into the substrate away from the surface. This can be described phenomenologically by an increased effective oxide thickness $T_{\rm ox}$ [21, 22]. The calculated $\Delta T_{\rm ox}$-$V_{\rm gs}$ characteristics is shown in Fig. 12. Equations implemented into HiSIM for the reproduction of quantum mechanical effects are:

$$T_{\rm ox} = \mathbf{TOX} + \Delta T_{\rm ox} \tag{51}$$

$$\Delta T_{\rm ox} = \frac{\mathbf{QME1}}{V_{\rm gs} - V_{\rm th}(T_{\rm ox} = \mathbf{TOX}) + \mathbf{QME2}} + \mathbf{QME3} \tag{52}$$

where **QME1**, **QME2**, and **QME3** are the quantum-effect model parameters. A limiting function is introduced in the source code to avoid unreasonable $\Delta T_{\rm ox}$ increase below the threshold voltage.

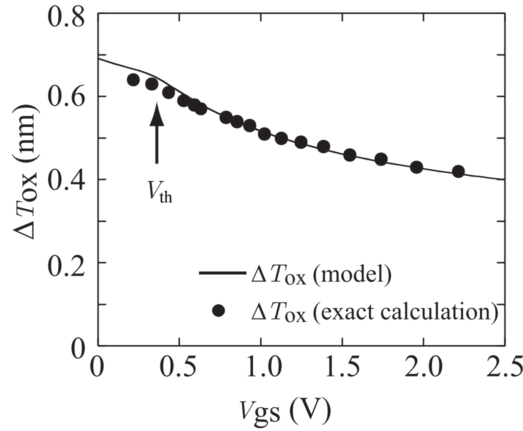

Fig. 12: Calculated $T_{\rm ox}$ increase by the quantum mechanical effect. The solid line shows model results with Eqs. (51) and (52). Symbols are exact calculation results by solving the Poisson equation and the Schrödinger equation simultaneously.

The HiSIM model parameters introduced in section 9 are summarized in Table 8.

Table 8: HiSIM model parameters introduced in section 9 of this manual.

QME1	$V_{\rm gs}$ dependence
QME2	$V_{\rm gs}$ dependence
QME3	minimum $T_{\rm ox}$ modification

10 Mobility Model

The low-field mobility is described with the following expressions and includes the three independent mechanisms of Coulomb, phonon and surface-roughness scattering [23]:

$$\frac{1}{\mu_0} = \frac{1}{\mu_{\mathrm{CB}}} + \frac{1}{\mu_{\mathrm{PH}}} + \frac{1}{\mu_{\mathrm{SR}}} \tag{53}$$

$$\mu_{\mathrm{CB}}(\mathrm{Coulomb}) = \mathbf{MUECB0} + \mathbf{MUECB1}\frac{Q_{\mathrm{i}}}{q \cdot 10^{11}} \tag{54}$$

$$\mu_{\mathrm{PH}}(\mathrm{phonon}) = \frac{M_{\mathrm{uephonon}}}{E_{\mathrm{eff}}^{\mathbf{MUEPH0}}} \tag{55}$$

$$\mu_{\mathrm{SR}}(\mathrm{surface\ roughness}) = \frac{\mathbf{MUESR1}}{E_{\mathrm{eff}}^{M_{\mathrm{uesurface}}}} \tag{56}$$

where $\mu_{\mathrm{PH}}(\mathrm{phonon})$ is temperature dependent as modeled in section 14.
Here E_{eff} is the effective field normal to the surface. The field are written as

$$E_{\mathrm{eff}} = E_{\mathrm{eff0}} \cdot (1 + \mathbf{MUEEFB} \cdot V_{\mathrm{bs}}) \tag{57}$$

$$E_{\mathrm{eff0}} = \frac{1}{\epsilon_{\mathrm{Si}}} \left(N_{\mathrm{dep}} \cdot Q_{\mathrm{b}} + \mathbf{NINV} \cdot Q_{\mathrm{i}}\right) \cdot f(\phi_{\mathrm{S}}) \tag{58}$$

$$f(\phi_{\mathrm{S}}) = \frac{1}{1 + (\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}) \cdot N_{\mathrm{invd}}} \tag{59}$$

$$\tag{60}$$

where N_{dep} and N_{invd} consider the gate length (L_{gate}) dependence as

$$N_{\mathrm{dep}} = \frac{\mathbf{NDEP}}{1 + \frac{\mathbf{NDEPL}}{\left(\frac{L_{\mathrm{gate}}}{10^{-6}}\right)^{\mathbf{NDEPLP}}}} \tag{61}$$

$$N_{\mathrm{invd}} = \mathbf{NINVD} \cdot \left(1 + \frac{\mathbf{NINVDL}}{\left(\frac{L_{\mathrm{gate}}}{10^{-6}}\right)^{\mathbf{NINVDLP}}}\right) \tag{62}$$

For the gate width (W_{gate}) dependence, see Section 12 Narrow-Channel Effects.
The mobility universality preserves following conditions [24, 25]

$$\mathbf{MUEPH0} \simeq 0.3 \tag{63}$$

$$M_{\mathrm{uesurface}} = 2.0 \tag{64}$$

$$\mathbf{NDEP} = 1.0 \tag{65}$$

$$\mathbf{NINV} = 0.5 \tag{66}$$

However, these parameters can be used for fitting purposes [26], if it is necessary.

The L_{gate} dependence of the mobility is considered as

$$M_{\mathrm{uephonon}} = \mathbf{MUEPH1} \cdot \left(1 + \frac{\mathbf{MUEPHL}}{\left(\frac{L_{\mathrm{gate}}}{10^{-6}}\right)^{\mathbf{MUEPLP}}} \right) \tag{67}$$

$$M_{\mathrm{uesurface}} = \mathbf{MUESR0} \cdot \left(1 + \frac{\mathbf{MUESRL}}{\left(\frac{L_{\mathrm{gate}}}{10^{-6}}\right)^{\mathbf{MUESLP}}} \right) \tag{68}$$

The high-field mobility is modeled as [27]

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_{\mathrm{y}}}{V_{\mathrm{max}}}\right)^{\mathbf{BB}}\right)^{\frac{1}{\mathbf{BB}}}} \tag{69}$$

The velocity overshoot is included in the mobility model in the following manner

$$V_{\mathrm{max}} = \mathbf{VMAX} \cdot \left(1 + \frac{\mathbf{VOVER}}{\left(\frac{L_{\mathrm{gate}}}{10^{-6}}\right)^{\mathbf{VOVERP}}} \right) \tag{70}$$

The HiSIM model parameters introduced in section 10 are summarized in Table 9.

Table 9: HiSIM model parameters introduced in section 10 of this manual. ∗ indicates minor parameters.

MUECB0	Coulomb scattering
MUECB1	Coulomb scattering
MUEPH0	phonon scattering
MUEPH1	phonon scattering
∗**MUEEFB**	Vbs dependence of phonon mobility
∗**MUEPHL**	length dependence of phonon mobility reduction
∗**MUEPLP**	length dependence of phonon mobility reduction
MUESR0	surface-roughness scattering
MUESR1	surface-roughness scattering
∗**MUESRL**	length dependence of surface roughness mobility reduction
∗**MUESLP**	length dependence of surface roughness mobility reduction
NDEP	depletion charge contribution on effective-electric field
***NDEPL**	modification of depletion charge contribution for short-channel case
***NDEPLP**	modification of depletion charge contribution for short-channel case
NINV	inversion charge contribution on effective-electric field
***NINVD**	reduced resistance effect for small V_{ds}
BB	high-field-mobility degradation
VMAX	maximum saturation velocity
VOVER	velocity overshoot effect
VOVERP	L_{eff} dependence of velocity overshoot

11 Channel-Length Modulation

The gradual-channel approximation is applied to derive analytical equations for describing device characteristics. However, this approximation is not valid for large V_{ds} causing the pinch-off phenomenon in the channel. To include the pinch-off phenomenon in HiSIM, we apply the conventional method of modeling the pinch-off region (ΔL) separately from the rest of the channel as depicted in Fig. 13 [29].

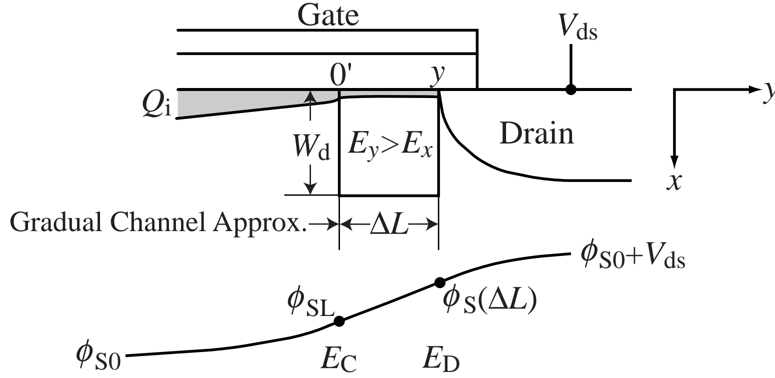

Fig. 13: Schematic showing the correlation among physical quantities in the pinch-off region.

The potential value at the end of the channel ($\phi_{\mathrm{S}}(\Delta L)$) lies between ϕ_{SL} and $\phi_{\mathrm{S0}} + V_{\mathrm{ds}}$. The exact value is dependent on the junction profile between the channel and the drain contact. This dependence is modeled with the parameter **CLM1** as

$$\phi_{\mathrm{S}}(\Delta L) = (1 - \mathbf{CLM1}) \cdot \phi_{\mathrm{SL}} + \mathbf{CLM1} \cdot (\phi_{\mathrm{S0}} + V_{\mathrm{ds}}) \tag{71}$$

where **CLM1** can be interpreted to represent the hardness of the junction and must be in the range $0 \leq \mathbf{CLM1} \leq 1$. Here $\mathbf{CLM1} = 1$ means that the contact profile is abrupt and the complete potential increase occurs in the ΔL region, whereas $\mathbf{CLM1} = 0$ corresponds to the opposite condition and there is no potential increase in the ΔL region.

The final ΔL is derived as

$$\begin{aligned}\Delta L =& \frac{1}{2}\left[-\frac{1}{L_{eff}}\left(2\frac{I_{\mathrm{dd}}}{\beta Q_{\mathrm{i}}}z + 2\frac{qN_{\mathrm{sub}}}{\epsilon_{Si}}(\phi_s(\Delta L) - \phi_{SL})z^2 + E_0 z^2\right)\right.\\ &\left. + \sqrt{\frac{1}{L_{eff}^2}\left(2\frac{I_{\mathrm{dd}}}{\beta Q_{\mathrm{i}}}z + 2\frac{qN_{\mathrm{sub}}}{\epsilon_{Si}}(\phi_s(\Delta L) - \phi_{SL})z^2 + E_0 z^2\right)^2 + 4\left(2\frac{qN_{\mathrm{sub}}}{\epsilon_{Si}}(\phi_s(\Delta L) - \phi_{SL})z^2 + E_0 z^2\right)}\,\right]\end{aligned} \tag{72}$$

where E_0 is fixed to 10^5 and

$$z = \frac{\epsilon_{Si} \cdot W_{\mathrm{d}}}{\mathbf{CLM2} \cdot Q_b + \mathbf{CLM3} \cdot Q_i} \tag{73}$$

Two model parameters **CLM2** and **CLM3** are introduced to consider the uncertainty of Q_{i} in the pinch-off region and to counterbalance the two contributions from Q_{b} ($= qN_{\mathrm{sub}}W_{\mathrm{d}}$) and Q_{i}. It has to be notified that ΔL is equal to zero, when **CLM1**=0.

Additional contributions on CLM such as the pocket effect is modeled as

$$\Delta L = \Delta L \left(1 + \mathbf{CLM6} \cdot (L_{\rm gate} \cdot 10^6)^{\mathbf{CLM5}}\right) \tag{74}$$

It can be happen that $L_{\rm eff} - \Delta L$ becomes negative, if extracted **CLM5** and **CLM6** values are out of acceptable ranges. In this case HiSIM gives "warning" and fixes $L_{\rm eff} - \Delta L$ to $1nm$.

The HiSIM model parameters introduced in section 11 are summarized in Table 10.

Table 10: HiSIM model parameters introduced in section 11 of this manual.

CLM1	hardness coefficient of channel/contact junction
CLM2	coefficient for $Q_{\rm B}$ contribution
CLM3	coefficient for $Q_{\rm I}$ contribution
***CLM5**	effect of pocket implantation
***CLM6**	effect of pocket implantation

12 Narrow-Channel Effects

12.1 Threshold Voltage Modification

The fringing capacitances C_{ef} at the edge of the isolation is modeled [9] as

$$\Delta V_{\mathrm{th,W}} = \left(\frac{1}{C_{\mathrm{ox}}} - \frac{1}{C_{\mathrm{ox}} + 2C_{\mathrm{ef}}/(L_{\mathrm{eff}} W_{\mathrm{eff}})}\right) q N_{\mathrm{sub}} W_{\mathrm{d}} + \frac{\mathbf{WVTH0}}{W_{\mathrm{gate}} \cdot 10^6} \tag{75}$$

where **WVTH0** is the parameter for including the basic width dependence and

$$C_{\mathrm{ef}} = \frac{2\epsilon_{\mathrm{ox}}}{\pi} L_{\mathrm{eff}} \ln\left(\frac{2T_{\mathrm{fox}}}{T_{\mathrm{ox}}}\right) = \frac{\mathbf{WFC}}{2} L_{\mathrm{eff}} \tag{76}$$

Here, T_{fox} is the thickness of the oxide at the trench edge, and **WFC** is the model parameter for including the edge-fringing-capacitance effects. The final ΔV_{th} of Eq. (11), under inclusion of the shallow-trench-isolation effects, becomes:

$$\Delta V_{\mathrm{th}} = \Delta V_{\mathrm{th,SC}} + \Delta V_{\mathrm{th,R}} + \Delta V_{\mathrm{th,P}} + \Delta V_{\mathrm{th,W}} - \phi_{\mathrm{Spg}} \tag{77}$$

The width dependence of the pocket impurity concentration is modeled as

$$N_{\mathrm{subp}} = \mathbf{NSUBP} \cdot \left(1 + \frac{\mathbf{NSUBP0}}{(W_{\mathrm{gate}} \cdot 10^6)^{\mathbf{NSUBWP}}}\right) \tag{78}$$

The width dependence of the substrate impurity concentration N_{subc} is also considered as

$$N_{\mathrm{subc}} = \mathbf{NSUBC} \cdot \left(1 + \frac{\mathbf{NSUBCW}}{(W_{\mathrm{gate}} \cdot 10^6)^{\mathbf{NSUBCWP}}}\right) \tag{79}$$

12.2 Mobility Change

A reduction of $I_{\mathrm{ds,sat}}$ with reduced W_{gate} as indicated by curve C1 in Fig. 14 [31] is modeled by a decreasing phonon mobility with two model parameters **MUEPHW** and **MUEPWP** as

$$M_{\mathrm{uephonon}} = M_{\mathrm{uephonon}} \cdot \left(1 + \frac{\mathbf{MUEPHW}}{(W_{\mathrm{gate}} \cdot 10^6)^{\mathbf{MUEPWP}}}\right) \tag{80}$$

A start to increase for narrower W_{gate} as denoted by curve C2 is modeled as a change of the surface-roughness contribution caused by a carrier flow in increasing distance from the surface as

$$M_{\mathrm{uesurface}} = M_{\mathrm{uesurface}} \cdot \left(1 + \frac{\mathbf{MUESRW}}{(W_{\mathrm{gate}} \cdot 10^6)^{\mathbf{MUESWP}}}\right) \tag{81}$$

Further width dependences are included as

$$N_{\mathrm{invd}} = N_{\mathrm{invd}} \cdot \left(1 + \frac{\mathbf{NINVDW}}{(W_{\mathrm{gate}} \cdot 10^6)^{\mathbf{NINVDWP}}}\right) \tag{82}$$

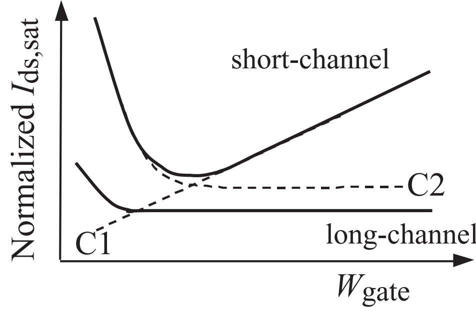

Fig. 14: Schematic of the normalized saturation current $I_{\mathrm{ds,sat}}$ as a function of the gate width W_{gate} for two different gate lengths L_{gate}.

12.3 Transistor Leakage due to Shallow Trench Isolation (STI): Hump in I_{ds}

The surface potential of the leakage regions at the trench edges can be derived analytically as [32]

$$\phi_{\mathrm{S,STI}} = V'_{\mathrm{gs,STI}} + \frac{\epsilon_{\mathrm{Si}} Q_{\mathrm{N,STI}}}{C'^{2}_{\mathrm{ox}}} \left[1 - \sqrt{1 + \frac{2C'^{2}_{\mathrm{ox}}}{\epsilon_{\mathrm{Si}} Q_{\mathrm{N,STI}}} \left(V'_{\mathrm{gs,STI}} - V_{\mathrm{bs}} - \frac{1}{\beta} \right)} \right] \tag{83}$$

where

$$Q_{\mathrm{N,STI}} = q \cdot \mathbf{NSTI} \tag{84}$$

$$V'_{\mathrm{gs,STI}} = V_{\mathrm{gs}} - \mathbf{VFBC} + V_{\mathrm{thSTI}} + \Delta V_{\mathrm{th,SCSTI}} \tag{85}$$

where

$$V_{\mathrm{thSTI}} = \mathbf{VTHSTI} - \mathbf{VDSTI} \cdot V_{\mathrm{ds}} \tag{86}$$

and

$$\Delta V_{\mathrm{th,SCSTI}} = \frac{\epsilon_{\mathrm{Si}}}{C_{\mathrm{ox}}} W_{\mathrm{d,STI}} \frac{dE_y}{dy} \tag{87}$$

The threshold voltage for the STI effect **VTHSTI** includes features of STI such as **NSTI** which are diferent from the substrate. The depletion-layer thickness $W_{\mathrm{d,STI}}$ is written as

$$W_{\mathrm{d,STI}} = \sqrt{\frac{2\epsilon_{\mathrm{Si}}(2\Phi_{\mathrm{B,STI}} - V_{\mathrm{bs}})}{q\mathbf{NSTI}}}. \tag{88}$$

$\frac{dE_y}{dy}$ is described with model parameters in the same form as in section 6.1 on short-channel effects

$$\frac{dE_y}{dy} = \frac{2(\mathbf{VBI} - 2\Phi_{\mathrm{B,STI}})}{(L_{\mathrm{gate,sm}} - \mathbf{PARL2})^2} (\mathbf{SCSTI1} + \mathbf{SCSTI2} \cdot V_{\mathrm{ds}}) \tag{89}$$

where

$$L_{\mathrm{gate,sm}} = L_{\mathrm{gate}} + \frac{\mathbf{WL1}}{wl^{\mathbf{WL1P}}} \tag{90}$$

$$wl = (W_{\rm gate} \cdot 10^6) \times (L_{\rm gate} \cdot 10^6) \tag{91}$$

The modeling of the transistor leakage for STI technologies is based on the idea that the current in the subthreshold region is governed only by the diffusion term. The carrier concentration $Q_{\rm i,STI}$ is calculated analytically for the subthreshold region, where the STI effect is obvious [1]. The final leakage current equation is written as

$$I_{\rm ds,STI} = 2\frac{W_{\rm STI}}{L_{\rm eff} - \Delta L}\mu\frac{Q_{\rm i,STI}}{\beta}\left[1 - \exp(-\beta V_{\rm ds})\right] \tag{92}$$

where $W_{\rm STI}$ determines the width of the high-field region. The gate length dependence of $W_{\rm STI}$ is included as

$$W_{\rm STI} = \mathbf{WSTI}\left(1 + \frac{\mathbf{WSTIL}}{(L_{\rm gate,sm} \cdot 10^6)^{\mathbf{WSTILP}}}\right)\left(1 + \frac{\mathbf{WSTIW}}{(W_{\rm gate,sm} \cdot 10^6)^{\mathbf{WSTIWP}}}\right) \tag{93}$$

12.4 Small Geometry

Small size devices do not show the same scaling characteristic as long-channel or wide-channel devices, but rather deviate significantly. The reason is mainly due to the resolution inaccuracy of the lithography. The small geometry effects are modeled first as the threshold voltage shift

$$\Delta V_{\rm th} = \Delta V_{\rm th,SC} + \Delta V_{\rm th,R} + \Delta V_{\rm th,P} + \Delta V_{\rm th,W} + \Delta V_{\rm th,sm} - \phi_{\rm Spg} \tag{94}$$

where

$$\Delta V_{\rm th,sm} = \frac{\mathbf{WL2}}{wl^{\mathbf{WL2P}}} \tag{95}$$

The mobility modification due to the small device geometry is also modeled in the phonon scattering as

$$M_{\rm uephonon} = M_{\rm uephonon} \cdot \left(1 + \frac{\mathbf{MUEPHS}}{wl^{\mathbf{MUEPSP}}}\right) \tag{96}$$

$$V_{\rm max} = V_{\rm max} \cdot \left(1 + \frac{\mathbf{VOVERS}}{wl^{\mathbf{VOVERSP}}}\right) \tag{97}$$

The HiSIM model parameters introduced in section 12 are summarized in Table 11.

Table 11: HiSIM model parameters introduced in section 12 of this manual. * indicates minor parameters.

Parameter	Description
WFC	threshold voltage change due to capacitance change
***WVTH0**	threshold voltage shift
NSUBC	substrate-impurity concentration
***NSUBCW**	width dependence of substrate-impurity concentration
***NSUBCWP**	width dependence of substrate-impurity concentration
***NSUBP0**	modification of pocket concentration for narrow width
***NSUBWP**	modification of pocket concentration for narrow width
***MUEPHW**	phonon related mobility reduction
***MUEPWP**	phonon related mobility reduction
***MUESRW**	change of surface roughness related mobility
***MUESWP**	change of surface roughness related mobility
***NINVDW**	width dependence on high field mobility
***NINVDWP**	width dependence on high field mobility
***VTHSTI**	threshold voltage shift due to STI
***VDSTI**	threshold voltage shift dependence on $V_{\rm ds}$ due to STI
***SCSTI1**	the same effect as **SC1** but at STI edge
***SCSTI2**	the same effect as **SC2** but at STI edge
NSTI	substrate-impurity concentration at the STI edge
WSTI	width of the high-field region at STI edge
***WSTIL**	channel-length dependence of **WSTI**
***WSTILP**	channel-length dependence of **WSTI**
***WSTIW**	channel-width dependence of **WSTI**
***WSTIWP**	channel-width dependence of **WSTI**
WL1	threshold volatge shift of STI leakage due to small size effect
WL1P	threshold voltage shift of STI leakage due to small size effect
WL2	threshold volatge shift due to small size effect
WL2P	threshold voltage shift due to small size effect
***MUEPHS**	mobility modification due to small size
***MUEPSP**	mobility modification due to small size
***VOVERS**	modification of maximum velocity due to small size
***VOVERSP**	modification of maximum velocity due to small size

13 Effects of the Source/Drain Diffusion Length for Shallow Trench Isolation (STI) Technologies

The diffusion length, L_{od} between MOSFET gate and STI edge affects the MOSFET characteristics. The influence is observed mainly in V_{th} and in the saturation current. The V_{th} change is attributed to a change of the pocket impurity concentration and modeled as

$$N_{\mathrm{substi}} = \frac{1 + T1 \cdot T2}{1 + T1 \cdot T3} \tag{98}$$

where

$$\begin{aligned} T1 &= \frac{1}{1 + \mathbf{NSUBPSTI2}} \\ T2 &= \frac{\mathbf{NSUBPSTI1}}{L_{\mathrm{od_half}}}^{\mathbf{NSUBPSTI3}} \\ T3 &= \frac{\mathbf{NSUBPSTI1}}{L_{\mathrm{od_half_ref}}}^{\mathbf{NSUBPSTI3}} \end{aligned} \tag{99}$$

which is used to modify the pocket concentration N_{subp} as

$$N_{\mathrm{subp}} = N_{\mathrm{subp}} \cdot N_{\mathrm{substi}}. \tag{100}$$

The saturation-current change is attributed to a change of the mobility and modeled as

$$M_{\mathrm{uesti}} = \frac{1 + T1 \cdot T2}{1 + T1 \cdot T3} \tag{101}$$

where

$$\begin{aligned} T1 &= \frac{1}{1 + \mathbf{MUESTI2}} \\ T2 &= \frac{\mathbf{MUESTI1}}{L_{\mathrm{od_half}}}^{\mathbf{MUESTI3}} \\ T3 &= \frac{\mathbf{MUESTI1}}{L_{\mathrm{od_half_eff}}}^{\mathbf{MUESTI3}} \end{aligned} \tag{102}$$

which is used to modify the phonon mobility parameter M_{uephonon} as

$$M_{\mathrm{uephonon}} = M_{\mathrm{uephonon}} \cdot M_{\mathrm{uesti}} \tag{103}$$

where $L_{\mathrm{od_half}}$ and $L_{\mathrm{od_half_eff}}$ are determined in the same way as BSIM4.6.0 with model parameters **SAREF** and **SBREF** and instance parameters **SA**, **SB**, and **SD**.

The HiSIM model parameters introduced in section 13 are summarized in Table 12.

Table 12: HiSIM model parameters introduced in section 13 of this manual. # indicates instance parameters.

NSUBPSTI1	pocket concentration change due to diffusion-region length between gate and STI
NSUBPSTI2	pocket concentration change due to diffusion-region length between gate and STI
NSUBPSTI3	pocket concentration change due to diffusion-region length between gate and STI
MUESTI1	mobility change due to diffusion-region length between gate and STI
MUESTI2	mobility change due to diffusion-region length between gate and STI
MUESTI3	mobility change due to diffusion-region length between gate and STI
SAREF	length of diffusion between gate and STI
SBREF	length of diffusion between gate and STI
#**SA**	length of diffusion between gate and STI
#**SB**	length of diffusion between gate and STI
#**SD**	length of diffusion between gate and gate

14 Temperature Dependences

In HiSIM_HV **TEMP** is treated as a simulation option, and temperature $T0$ is determined as

$$T0 = \mathbf{TEMP} + \mathbf{DTEMP} \tag{104}$$

where **DTEMP** is an instance parameter describing the temperature increase from **TEMP**, thus $T0$ is the given temperature. Whereas the temperature including the self heating effect is distinguished by T

$$T = T0 + \delta T \tag{105}$$

where δT is the temperature increase by the self-heating effect. The temperature dependence is included automatically in the surface potentials through β, which is the inverse of the thermal voltage. Additionally the bandgap, the intrinsic carrier concentration, the carrier mobility, and the carrier saturation velocity are also temperature dependent. The temperature dependence of the bandgap determines the temperature dependence of $V_{\rm th}$ [33] and is modeled as

$$E_{\rm g} = E_{\rm gnom} - \mathbf{BGTMP1} \cdot (T - \mathbf{TNOM}) - \mathbf{BGTMP2} \cdot (T - \mathbf{TNOM})^2 \tag{106}$$

$$E_{\rm gnom} = \mathbf{EG0} - 90.25 \cdot 10^{-6} \cdot \mathbf{TNOM} - 1.0 \cdot 10^{-7} \cdot \mathbf{TNOM}^2 \tag{107}$$

where T is the given temperature. The temperature dependence of the intrinsic carrier concentration is given by

$$n_{\rm i} = n_{\rm i0} \cdot T^{\frac{3}{2}} \cdot \exp\left(-\frac{E_{\rm g}}{2q}\beta\right) \tag{108}$$

The temperature dependence of the mobility and the temperature dependence of the saturation velocity have a major influence on the temperature dependence of the $I_{\rm ds}$-$V_{\rm ds}$ characteristics under the on-current condition. They are modeled as [27]:

$$\mu_{\rm PH}(\text{phonon}) = \frac{M_{\rm uephonon}}{(T/\mathbf{TNOM})^{\mathbf{MUETMP}} \cdot E_{\rm eff}^{\mathbf{MUEPH0}}} \tag{109}$$

$$V_{\rm max} = \frac{\mathbf{VMAX}}{1.8 + 0.4(T/\mathbf{TNOM}) + 0.1(T/\mathbf{TNOM})^2 - \mathbf{VTMP} \cdot (1 - T/\mathbf{TNOM})} \tag{110}$$

$$\mu_{\rm PHdep}(\text{phonon}) = \frac{DEP_{\rm muephonon}}{(T/\mathbf{TNOM})^{\mathbf{DEPMUETMP}} \cdot E_{\rm eff}^{\mathbf{DEPMUEPH0}}} \tag{111}$$

$$DEP_{\rm vmax} = \frac{\mathbf{DEPVMAX}}{1.8 + 0.4(T/\mathbf{TNOM}) + 0.1(T/\mathbf{TNOM})^2 - \mathbf{DEPVTMP} \cdot (1 - T/\mathbf{TNOM})} \tag{112}$$

The temperature dependence of the gate current is modeled by modifying the bandgap specific for the gate current as

$$E_{\rm gp} = E_{\rm g0} + \mathbf{EGIG} + \mathbf{IGTEMP2}\left(\frac{1}{T} - \frac{1}{\mathbf{TNOM}}\right) + \mathbf{IGTEMP3}\left(\frac{1}{T^2} - \frac{1}{\mathbf{TNOM}^2}\right) \tag{113}$$

where E_{g0} is the bandgap at **TNOM**.

In addition to the temperature dependence of the physical quantities considered, resistances include the temperature dependence, which is modeled with the given temperature to avoid complication in parameter extraction.

CORDRIFT=1: default

$$\mu_{\mathrm{drift0,temp}} = \frac{\mathbf{RDRMUE}}{(T/\mathbf{TNOM})^{\mathbf{RDRMUETMP}}} \tag{114}$$

$$V_{\mathrm{max_drift,temp}} = \frac{\mathbf{RDRVMAX}}{1.8 + 0.4(T/\mathbf{TNOM})\ + 0.1(T/\mathbf{TNOM})^2 - \mathbf{RDRVTMP}\cdot(1 - T/\mathbf{TNOM})} \tag{115}$$

where $V_{\mathrm{max}}\,(T)$, V_{over} and V_{overp} are temperature dependence of **VMAX**, **VOVER** and **VOVERP** in Section 10.

In addition to the temperature dependence of the physical quantities considered, resistances include the temperature dependence, which is modeled with the given temperature to avoid complication in parameter extraction.

$$tempm = \frac{1}{(T/\mathbf{TNOM})^{\mathbf{RDRMUETMP}}} \tag{116}$$

$$\mu_{\mathrm{drift0,tempm}} = tempm\cdot\mathbf{RDRMUE} \tag{117}$$

$$\mu_{\mathrm{source0,temp}} = tempm\cdot\mathbf{RDRMUES} \tag{118}$$

$$tempv = \frac{1}{1.8 + 0.4(T/\mathbf{TNOM})\ + 0.1(T/\mathbf{TNOM})^2 - \mathbf{RDRVTMP}\cdot(1 - T/\mathbf{TNOM})} \tag{119}$$

$$V_{\mathrm{rmax_drift,temp}} = tempv\cdot\mathbf{RDRVMAX} \tag{120}$$

$$V_{\mathrm{rmax_source,temp}} = tempv\cdot\mathbf{RDRVMAXS} \tag{121}$$

$$R_{\mathrm{drbb}} = \mathbf{RDRBB} + \mathbf{RDRBBTMP}(T - \mathbf{TNOM}) \tag{122}$$

CORDRIFT=0: old model

$$R_{\mathrm{d0,temp}} = \mathbf{RDTEMP1}\cdot(T0 - \mathbf{TNOM}) + \mathbf{RDTEMP2}\cdot(T0^2 - \mathbf{TNOM}^2) \tag{123}$$

$$R_{\mathrm{dvd,temp}} = \mathbf{RDVDTEMP1}\cdot(T0 - \mathbf{TNOM}) + \mathbf{RDVDTEMP2}\cdot(T0^2 - \mathbf{TNOM}^2) \tag{124}$$

Additional temperature dependences are also included with the given temperature in case they are needed.

CORDRIFT=1,0

$$V_{\mathrm{max}} = V_{\mathrm{MAX}}\cdot\left(1 + \mathbf{VMAXT1}\cdot(T0 - \mathbf{TNOM}) + \mathbf{VMAXT2}\cdot(T0^2 - \mathbf{TNOM}^2)\right) \tag{125}$$

$$N_{\mathrm{invd}} = N_{\mathrm{invd}}\cdot\left(1 + \mathbf{NINVDT1}\cdot(T0 - \mathbf{TNOM}) + \mathbf{NINVDT2}\cdot(T0^2 - \mathbf{TNOM}^2)\right) \tag{126}$$

where $T0$ in the above four equations can be replaced by T including the temperature increase due to the self-heating effect by selecting Flag **COTEMP** (see in section 28).
Furthermore, when aging simulation is performed (**CODEG**=1), temperature dependence of the trap density , $N_{\rm tA}$, is considered in the following manner:

$$N_{\rm tA}(T) = N_{\rm tA}(\textbf{TNOM}) \cdot \big(1 + \textbf{TRAPTEMP1} \cdot (T0 - \textbf{TNOM}) + \textbf{TRAPTEMP2} \cdot (T0^2 - \textbf{TNOM}^2\big) \tag{127}$$

The HiSIM model parameters introduced in section 14 are summarized in Table 13.

Table 13: HiSIM model parameters introduced in section 14 of this manual. ∗ indicates minor parameters. # indicates an instance parameter.

EG0	bandgap
BGTMP1	temperature dependence of bandgap
BGTMP2	temperature dependence of bandgap
MUETMP	temperature dependence of phonon scattering
TNOM	temperature selected as nominal temperature value
#**DTEMP**	temperature increase from the given temperature
∗**VTMP**	temperature dependence of the saturation velocity
EGIG	bandgap of gate current
IGTEMP2	temperature dependence of gate current
IGTEMP3	temperature dependence of gate current
RDRMUE	field dependent mobility in the drift region
RDRMUETMP	temperature dependence of resistance
RDRVTMP	temperature dependence of resistance
RDRBBTMP	temperature dependence of resistance
RDRVMAX	saturaion velocity in the drift region
RDTEMP1	temperature dependence of resistance for **CORDRIFT**=0
RDTEMP2	temperature dependence of resistance for **CORDRIFT**=0
RDVDTEMP1	temperature dependence of resistance
RDVDTEMP2	temperature dependence of resistance
NINVDT1	temperature dependence of univerisal mobility model
NINVDT2	temperature dependence of univerisal mobility model
VMAXT1	temperature dependence of velocity
VMAXT2	temperature dependence of velocity
TRAPTEMP1	temperture dependence of trap density (**CODEG**=1)
TRAPTEMP2	temperture dependence of trap density (**CODEG**=1)

15 Resistances

Specific features of LDMOS/HVMOS originate from its highly resistive source and drift regions, sustaining high voltages applied to the MOSFETs. HiSIM_HV 2.0.0 provides two options for modeling the drift region resistance R_{drift} enabled by the choice of the flag **CORDRIFT**. The resistance model selection is enabled as depicted in Fig. 15. With **CORDRIFT**=0, the legacy resistance model of HiSIM_HV 1 is activated, and the new model [56] added in HiSIM_HV 2 is selected by **CORDRIFT**=1. To switch off the resistance effect completely, the flag **CORDRIFT** together with that of **CORSRD** must be set to zero. Alternatively, when **CORDRIFT**=1, the flags **CORS** and/or **CORD** can be set to zero for switching off the resistance model on source and/or drain side respectively. Note **CORSRD** is inactive when **CORDRIFT**=1.

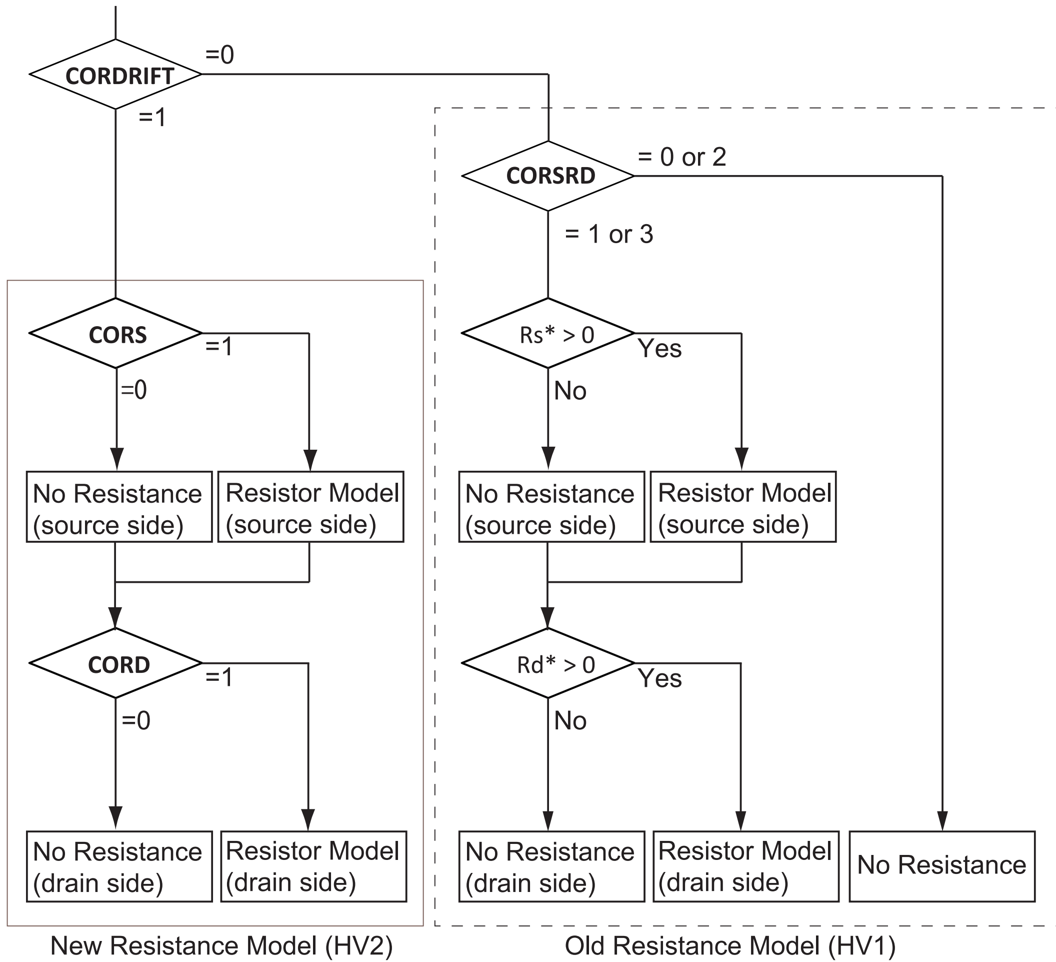

Fig. 15: Resistance model selection. The flag **CORDRIFT** selects either of the legacy HV1 resistance model (**CORDRIFT**=0) or the HV2 resistance model (**CORDRIFT**=1). For **CORDRIFT**=1, the flags **CORS** and **CORD** can be used for activation of the resistance model on source side and drain side respectively. For the use of **CORSRD**, refer to Fig. 17. Rd^* represents an estimator that consists of bias-indepentent part of the drain-side resistance expression and reduces to zero when drain resisitance becomes zero irrespective of bias and tempeture. Rs^* represents the estimator to this effect for the source-side resistance.

15.1 CORDRIFT=1 (default): Diffused Resistor Model

Figure 16 shows a schematic feature of the device. The potential drops V_{ssp} and V_{ddp} are calculated by SPICE iteratively.

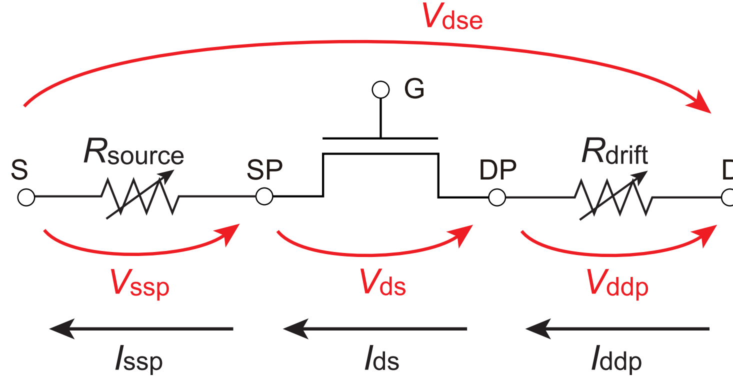

Fig. 16: Model concept

15.1.1 Drain side

The drain side resistance R_{drift} is written with the current flowing in the drift region I_{ddp} as

$$R_{\mathrm{drift}} = \left(\frac{V_{\mathrm{ddp}}}{I_{\mathrm{ddp}}} \cdot T_{\mathrm{drift}} + \mathbf{RSH} \cdot \mathbf{NRD} \right) \tag{128}$$

If $\mathbf{COSYM} = 0$

$$T_{\mathrm{drift}} = \begin{cases} \left(\frac{L_{\mathrm{drift}}}{\mathbf{DDRIFT} - W_{\mathrm{dep,sub}}}\right) & \text{(if substrate terminal is activated)} \\ 1 & \text{(if substrate terminal is not activated)} \end{cases} \tag{129}$$

If $\mathbf{COSYM} = 1$

$$T_{\mathrm{drift}} = \begin{cases} \left(\frac{L_{\mathrm{drift}}}{\mathbf{DDRIFT} - W_{\mathrm{dep,sub}}}\right) & \text{(if substrate terminal is activated)} \\ 1 & \text{(if substrate terminal is not activated)} \end{cases} \tag{130}$$

where **NRD** is an instance parameter describing the number of squares of the drain diffusion, and **RSH** is its the sheet resistance of the square. The first terms of the right hand side of Eq. (128) considers the resistance in the drift region, and the second term is the that in the diffusion region, which are layout dependent.

$$I_{\rm ddp} = W_{\rm eff,LD} \cdot \mathbf{NF} \cdot X_{\rm ov} \cdot q \cdot N_{\rm drift} \cdot \mu_{\rm drift} \frac{V_{\rm ddp}}{L_{\rm drift} + \mathbf{RDRDL1}} \tag{131}$$

$$W_{\rm dep,sub} = \sqrt{\frac{2\epsilon_{\rm Si}\left(\mathbf{VBISUB} - (\mathbf{RDVDSUB} \cdot V_{\rm ds} + \mathbf{RDVSUB} \cdot V_{\rm sub,s})\right)}{q}} \cdot \sqrt{\frac{\mathbf{NSUBSUB}}{\mathbf{NOVER} \cdot (\mathbf{NSUBSUB} + \mathbf{NOVER})}} \tag{132}$$

where

$$L_{\rm drift} = \mathbf{LDRIFT1} + \mathbf{LDRIFT2} \tag{133}$$

$$\mu_{\rm drift} = \frac{\mu_{\rm drift0}}{\left[1 + \left(\frac{\mu_{\rm drift0}}{V_{\rm max_drift}} \cdot \frac{V_{\rm ddp}}{L_{\rm drift}}\right)^{R_{\rm drbb}}\right]^{\frac{1}{R_{\rm drbb}}}} \tag{134}$$

$$\mu_{\rm drift0} = \mu_{\rm drift0,temp} \left(1 + \frac{\mathbf{RDRMUEL}}{(L_{\rm gate} \cdot 10^6)^{\mathbf{RDRMUELP}}}\right) \tag{135}$$

$$V_{\rm max_drift} = V_{\rm max_drift,temp} \left(1 + \frac{\mathbf{RDRVMAXL}}{(L_{\rm gate} \cdot 10^6)^{\mathbf{RDRVMAXLP}}}\right) \left(1 + \frac{\mathbf{RDRVMAXW}}{(W_{\rm gate} \cdot 10^6)^{\mathbf{RDRVMAXWP}}}\right) \tag{136}$$

$$X_{\rm ov} = W_0 - \mathbf{RDRCX} \cdot \left(\frac{W_0}{\mathbf{RDRDJUNC}} W_{\rm dep} + \frac{W_0}{\mathbf{XLDLD}} W_{\rm junc}\right) \tag{137}$$

$$W_0 = \sqrt{\mathbf{XLDLD}^2 + \mathbf{RDRDJUNC}^2} \tag{138}$$

$$W_{\rm dep} = \sqrt{\frac{2\epsilon_{\rm Si}\left(-\phi_{\rm s,over}\right)}{q \cdot \mathbf{NOVER}}} \tag{139}$$

$$W_{\rm junc} = \sqrt{\frac{2\epsilon_{\rm Si}\left(V_{\rm dps} - V_{\rm bs} + V_{\rm bi}\right)}{q} \cdot \frac{N_{\rm sub}}{\mathbf{NOVER}\left(N_{\rm sub} + \mathbf{NOVER}\right)}} \tag{140}$$

$$N_{\rm drift} = \mathbf{NOVER} \left\{1 + \mathbf{RDRCAR}\left(\frac{V_{\rm ddp}}{L_{\rm drft} - \mathbf{RDRDL2}}\right)\left(1 - \frac{1}{1 + \frac{\mu_{\rm drift0}}{V_{\rm max_drift}} \cdot \frac{V_{\rm ddp}}{L_{\rm drift}}}\right)\right\} + \left(\mathbf{RDRQOVER} \frac{-Q'_{\rm over}}{q}\right) \tag{141}$$

The potential value of $V_{\rm ddp}$, the difference between the internal node DP and the drain node is calculated by circuit simulator.

15.1.2 Source side

The source-side resistance $R_{\rm source}$ is written with the current flowing in the drift region $I_{\rm ssp}$ as

$$R_{\rm source} = \left(\frac{V_{\rm ssp}}{I_{\rm ssp}} \cdot T_{\rm drifts} + \mathbf{RSH} \cdot \mathbf{NRS}\right) \tag{142}$$

$$T_{\rm drifts} = \frac{L_{\rm drifts}}{\mathbf{RDRDJUNC}} \tag{143}$$

where **NRS** is an instance parameter describing the number of squares of the source diffusion, and **RSH** is its sheet resistance of the square. The first terms of the right hand side of Eq. (142) considers the

resistance in the source drift region, and the second term is the that in the source diffusion region, which is layout dependent.

$$I_{\rm ssp} = W_{\rm eff,LD} \cdot \mathbf{NF} \cdot X_{\rm ov} \cdot q \cdot \mathbf{NOVERS} \cdot \mu_{\rm source} \frac{V_{\rm ssp}}{\mathbf{LDRIFTS}} \tag{144}$$

where

$$\mu_{\rm source} = \frac{\mu_{\rm source0}}{\left[1 + \left(\frac{\mu_{\rm source0}}{V_{\rm max_source}} \cdot \frac{V_{\rm ssp}}{\mathbf{LDRIFTS}}\right)^{R_{\rm srbb}}\right]^{\frac{1}{R_{\rm srbb}}}} \tag{145}$$

$$\mu_{\rm source0} = \mu_{\rm drift0,temp} \left(1 + \frac{\mathbf{RDRMUEL}}{(L_{\rm gate} \cdot 10^6)^{\mathbf{RDRMUELP}}}\right) \tag{146}$$

$$V_{\rm max_source} = V_{\rm max_drift,temp} \left(1 + \frac{\mathbf{RDRVMAXL}}{(L_{\rm gate} \cdot 10^6)^{\mathbf{RDRVMAXLP}}}\right) \left(1 + \frac{\mathbf{RDRVMAXW}}{(W_{\rm gate} \cdot 10^6)^{\mathbf{RDRVMAXWP}}}\right) \tag{147}$$

The potential value of $V_{\rm ssp}$, the difference between the internal node SP and the drain node is calculated by circuit simulator.

15.2 CORDRIFT=0: old model provided in HiSIM_HV 1

The voltage drops are in principle calculated iteratively for applied voltages to keep consistency among all device performances. However, a simple analytical description is also provided. Thus, the parasitic source and drain resistances, $R_{\rm s}$ and $R_{\rm drift}$, can be considered by different optional approaches. Flag **CORSRD** is provided for the selection of one of the possible approaches. **CORSRD** = 0, 1, 2, 3 means "no resistance", "external", "analytical", "external + analytical", respectively. Options to be selected by Flag **CORSRD** are summarized in Fig. 17.

The source and the drain resistances $R_{\rm s}$ and $R_{\rm d}$ cause a voltage drop from the applied voltage biases and the effective voltages are expressed as:

$$V_{\rm gs,eff} = V_{\rm gs} - I_{\rm ds} \cdot R_{\rm s} \tag{148}$$

$$V_{\rm ds,eff} = V_{\rm ds} - I_{\rm ds} \cdot (R_{\rm s} + R_{\rm drift}) \tag{149}$$

$$V_{\rm bs,eff} = V_{\rm bs} - I_{\rm ds} \cdot R_{\rm s} \tag{150}$$

for the DC condition, where the effective voltages are referred as internal node potential $V_{\rm dp}$.
The source side resistance is written as

$$R_{\rm s} = \frac{\mathbf{RS}}{W_{\rm eff,LD} \cdot \mathbf{NF}} + \mathbf{NRS} \cdot \mathbf{RSH} \tag{151}$$

where **NRS** is an instance parameter describing the number of squares of the source diffusion, and **RSH** is its the sheet resistance of the square. The first term of the right hand side of Eq. (151) considers

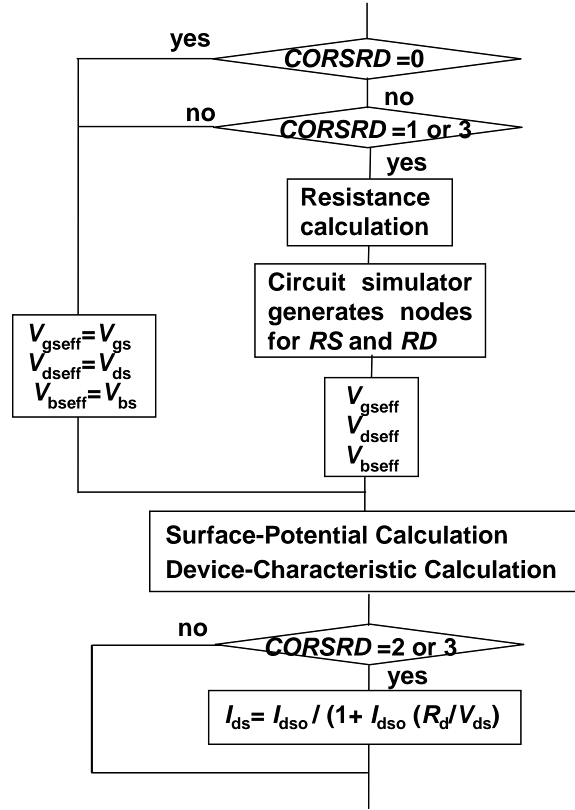

Fig. 17: Model options provided in HiSIM-LDMOS/HV for the resistance models, which are selected by Flag **CORSRD**.

the resistance in the LDD region, and the second term is that in the diffusion region, which is layout dependent.

CORSRD=2 considered only the resistance effect on the drain current as

$$I_{\rm ds} = \frac{I_{\rm ds0}}{1 + I_{\rm ds0}\frac{R_{\rm d}}{V_{\rm ds}}} \tag{152}$$

where $I_{\rm ds0}$ is the drain current without the resistance effect and

$$R_{\rm d} = \frac{1}{W_{\rm eff}}\left(R'_{\rm d} \cdot V_{\rm ds}^{\mathbf{RD21}} + V_{\rm bs} \cdot V_{\rm ds}^{\mathbf{RD22D}} \cdot \mathbf{RD22}\right) \tag{153}$$

$$RD23' \leq R'_{\rm d} \leq RD23'(1 + \mathbf{RD20}) \tag{154}$$

where

$$RD23' = \mathbf{RD23} \cdot \exp\left(-\mathbf{RD23L} \cdot (L_{\rm gate} \cdot 10^6)^{\mathbf{RD23LP}}\right)\left(1 + \frac{\mathbf{RD23S}}{(W_{\rm gate} \cdot 10^6 \cdot L_{\rm gate} \cdot 10^6)^{\mathbf{RD23SP}}}\right) \tag{155}$$

The $V_{\rm gs}$ dependence of $R'_{\rm d}$ is considered

$$R'_{\rm d} = \mathbf{RD24}\,(V_{\rm gs} - \mathbf{RD25}) \tag{156}$$

The resistance effect for the case **CORSRD**=1 is described here. However, in case if it is necessary, both resistance models (internal-node approach and anlytical approach) can be applied with **CORSRD**=3.

$$R_{\text{drift}} = (R_{\text{d}} + V_{\text{ds}} \cdot R_{\text{DVD}}) \left(1 + \mathbf{RDVG11} - \frac{\mathbf{RDVG11}}{\mathbf{RDVG12}} \cdot V_{\text{gs}}\right) \cdot (1 - V_{\text{bs}} \cdot \mathbf{RDVB}) \cdot T_{\text{drift}} \tag{157}$$

where T_{drift} is written in Eq. (129).

$$R_{\text{d}} = \frac{R_{\text{d0}}}{W_{\text{eff,LD}} \cdot \mathbf{NF}} \left(1 + \frac{\mathbf{RDS}}{(W_{\text{gate}} \cdot 10^6 \cdot L_{\text{gate}} \cdot 10^6)^{\mathbf{RDSP}}}\right) \tag{158}$$

$$R_{\text{d0}} = (\mathbf{RD} + R_{\text{d0,temp}})\, f_1 \cdot f_2 \tag{159}$$

$$R_{\text{DVD}} = \frac{\mathbf{RDVD} + R_{\text{dvd,temp}}}{W_{\text{eff}}} \cdot \exp\left(-\mathbf{RDVDL} \cdot (L_{\text{gate}} \cdot 10^6)^{\mathbf{RDVDLP}}\right) \cdot \left(1 + \frac{\mathbf{RDVDS}}{(W_{\text{gate}} \cdot 10^6 \cdot L_{\text{gate}} \cdot 10^6)^{\mathbf{RDVDSP}}}\right) \cdot f_1 \cdot f_2 \cdot f_3 \tag{160}$$

$$f_1(L_{\text{drift1}}) = \frac{\mathbf{LDRIFT1}}{1\mu m} \cdot \mathbf{RDSLP1} + \mathbf{RDICT1} \tag{161}$$

$$f_2(L_{\text{drift2}}) = \frac{\mathbf{LDRIFT2}}{1\mu m} \cdot \mathbf{RDSLP2} + \mathbf{RDICT2} \tag{162}$$

$$f_3(L_{\text{over}})^* = 1 + \left(\mathbf{RDOV11} - \frac{\mathbf{RDOV11}}{\mathbf{RDOV12}}\right) \cdot \frac{\mathbf{LOVERLD}}{1\mu m} + (1 - \mathbf{RDOV13}) \cdot \frac{\mathbf{LOVERLD}}{1\mu m} \tag{163}$$

LDRIFT1 and **LDRIFT2** are model parameters denoting lengths of different parts of the drift region. The source resistance in the LDMOS case does not consider a drift region and has therefore no drift length parameters. It is expected that either the second term of Eq. (163) or the third term is selected. For HiSIM_HV1.0 versions, **RDOV13** must be fixed to unity to select the second term. To select the third term **RDOV11** must be zero.

The final drift resistance R_{drift} is written as

$$R_{\text{drift}} = R_{\text{drift}} + \mathbf{RSH} \cdot \mathbf{NRD} \tag{164}$$

where **NRD** is an instance parameter describing the number of squares of the drain diffusion, and **RSH** is its the sheet resistance of the square. The first terms of the right hand side of the equation considers the resistance in the drift region, and the second term is the that in the diffusion region, which are layout dependent.

Here summarizes the selection of the resistance model for **CORDRIFT** = 0:

CORSRD = 0 : no resistance

CORSRD = 1 : solved by circuit siumlator with external nodes

All model parameters included in Eq. (151), Eq. (157)–Eq. (163) are used.

Model parameters are:

RS, **NRS**, **RSH**

RDVG11, **RDVG12**, **RDVB**, **RDS**, **RDSP**, **NRD**

RD, **RDVD**, **RDVDL**, **RDVDLP**, **RDVDS**, **RDVDSP**

RDSLP1, **RDICT1**, **RDSLP2**, **RDICT2**, **RDOV11**, **RDOV12**, **RDOV13**

RDVDSUB, **RDVSUB**, **VBISUB**, **DDRIFT**, **NSUBSUB**

CORSRD = 2 : solved with the analytical equations of Eq. (152)–Eq. (156)

Model parameters are:

RD21, **RD22**, **RD22D**, **RD23**, **RD23L**, **RD23LP**

RD23S, **RD23SP**, **RD24**, **RD25**, **RD20**

CORSRD = 3 : Both **CORSRD** = 1 and **CORSRD** = 2 are considered.

At the starting of the parameter extraction, following model parameters are suggested to set to zero:

RDVG11, **RDVB**, **RDVD**

RDTEMP1, **RDTEMP2**, **RDVDTEMP1**, **RDVDTEMP2**

The above condition refers to the bias independent resistance.

Table 14 summaizes the minimum resistance parameters to be determined.

Table 14: HiSIM_HV 1.2.0 resistance parameters introduced. If **RS** is not determined for the asymmetrical case, **RD** is taken.

	structure	source	drain
COSYM=0	**LDMOS**	**RS**(bias independent)	**RD**
COSYM=1	**symmetrical HVMOS**		**RD**
COSYM=1	**asymmetrical HVMOS**	**RS**	**RD**

15.3 Other resistances

The gate resistance becomes large as the gate width becomes large, which is the case for many RF circuits. The equation for the gate-resistance calculation is taken from the BSIM4 [34] description as

$$R_{\mathrm{g}} = \frac{\mathbf{RSHG} \cdot \left(\mathbf{XGW} + \frac{W_{\mathrm{eff}}}{3 \cdot \mathbf{NGCON}}\right)}{\mathbf{NGCON} \cdot (L_{\mathrm{drawn}} - \mathbf{XGL}) \cdot \mathbf{NF}} \tag{165}$$

where **RSHG** is the gate sheet resistance, and others are instance parameters dependent on the layout. The flag **CORG** is provided for the inclusion of gate resistance. **CORG** = 0,1 means "no", "external" gate resistance, respectively.

Model parameters for the same substrate resistance network as BSIM4 (**RBPB**, **RBPD**, **RBPS**) are included in the model parameter list, which are also treated as instance parameters.

The HiSIM model parameters introduced in section 15 are summarized in Table 15.

Table 15: HiSIM model parameters introduced in section 15 of this manual. # indicates instance parameters. $*$ indicates minor parameters.

RSH	sheet resistance of diffusion region (drain side)
RSHG	gate sheet resistance
RBPB	substrate resistance network
RBPD	substrate resistance network
RBPS	substrate resistance network
#NRS	number of source squares
#NRD	number of drain squares
#XGW	distance from the gate contact to the channel edge
#XGL	offset of the gate length
#NF	number of fingers
#NGCON	number of gate contacts
	CORDRIFT=1
RDRDL1	effective L_{drift} of current in drift region
RDRDL2	pinch-off length in drift region
RDRCX	exude of current flow from X_{ov}
RDRCAR	high field injection in drift region
RDRDJUNC	junction depth at channel/drift region (drain side)
RDRBB	high field mobility in drift region (drain side)
RDRBBS	high field mobility in drift region (source side)
RDRMUE	mobility in drift region (drain side)
RDRMUES	mobility in drift region (source side)
RDRVMAX	saturation velocity in drift region (drain side)
RDRVMAXS	saturation velocity in drift region (source side)
RDRVMAXL	saturation velocity L_{gate} dependence
RDRVMAXLP	saturation velocity L_{gate} dependence
RDRVMAXW	saturation velocity W_{gate} dependence
RDRVMAXWP	saturation velocity W_{gate} dependence
RDRMUEL	mobility in drift region L_{gate} dependence
RDRMUELP	moblity in drift region L_{gate} dependence
RDRQOVER	inclusion of the overlap charge into R_{drift} (drain side)
RDRQOVERS	inclusion of the overlap charge into R_{drift} (source side)
VBISUB	built-in potential at the drift/P-substrate junction
RDVDSUB	V_{ds} dependence of depletion width
RDVSUB	V_{sub} dependence of depletion width
DDRIFT	depth of the drift region
NSUBSUB	impurity concentration of the substrate required for V_{sub} dependence

RD20	**RD23** boundary for **CORSRD**=2,3
RD21	V_{ds} dependence of **RD** for **CORSRD**=2,3
RD22	V_{bs} dependence of **RD** for **CORSRD**=2,3
RD22D	V_{bs} dependence of **RD** for **CORSRD**=2,3 with large V_{ds}
RD23	modification of **RD** for **CORSRD**=2,3
***RD23L**	L_{gate} dependence of **RD23** boundary for **CORSRD**=2,3
***RD23LP**	L_{gate} dependence of **RD23** boundary for **CORSRD**=2,3
***RD23S**	small size dependence of **RD23** for **CORSRD**=2,3
***RD23SP**	small size dependence of **RD23** for **CORSRD**=2,3
***RD24**	V_{gs} dependence of **RD** for **CORSRD**=2,3
***RD25**	V_{gs} dependence of **RD** for **CORSRD**=2,3
VBISUB	built-in potential at the drift/substrate junction
RDVDSUB	V_{ds} dependence of depletion width
RDVSUB	V_{sub} dependence of depletion width
DDRIFT	depth of the drift region
NSUBSUB	impurity concentration of the substrate required for V_{sub} dependence

16 Capacitances

16.1 Intrinsic Capacitances

The intrinsic capacitances are derivatives of the node charges determined as

$$\begin{aligned} C_{jk} &= \delta \frac{\partial Q_j}{\partial V_k} \\ \delta = -1 \quad &\text{for} \quad j \neq k \\ \delta = \quad 1 \quad &\text{for} \quad j = k \end{aligned} \tag{166}$$

HiSIM uses analytical solutions for all 9 independent intrinsic capacitances, derived from the charges as explicit functions of the surface potentials. Therefore, there are no extra model parameters for the intrinsic capacitances except the width reduction parameter **XWDC** different from that of current **XWD**, namely W_{effc} for the total capacitance calculation instead of W_{eff}, if it is necessary.
The lateral electric field along the channel induces a capacitance C_{Q_y} which significantly affects the gate capacitance in saturation [35]. The induced charge associated with C_{Q_y} is described with the surface potential values as

$$Q_y = \epsilon_{\mathrm{Si}} W_{\mathrm{eff}} \cdot \mathbf{NF} W_{\mathrm{d}} \left(\frac{\phi_{\mathrm{S0}} + V_{\mathrm{ds}} - \phi_{\mathrm{S}}(\Delta L)}{\mathbf{XQY}} \right) + \frac{\mathbf{XQY1}}{L_{\mathrm{gate}}^{\mathbf{XQY2}}} V_{\mathrm{bs}} \tag{167}$$

introducing **XQY**, a parameter determining the maximum field at the channel/drain junction independent of L_{gate}. For **XQY**=0 the charge Q_{y} is fixed to zero.

16.2 Overlap Capacitances

The overlap capacitance includes three options as summarized in Fig. 18 for the drain side and Fig. 19 for the source side. If Flags **COOVLP**=**COOVLPS**=0, the overlap capacitances are treated to be constant. If **CGSO** and **CGDO** are determined, these values are taken. If they are not determined, the values are calculated with the overlap length and oxide capacitance.
If Flags **COOVLP**=**COOVLPS**=1, the bias dependent overlap capacitances are considered. Here two models are provided: One is the surface-potential-based model and the other describes with a simple V_{gs} dependence. If **NOVER** (impurity concentration of the overlap region) is given, the surface-potential-based model is selected. If **NOVER** is set to zero, the simplified bias-dependent model is selected. In addition to the bias-dependent capacitances, **CGSO** and **CGDO** can be also added, if they are determined.

The description is focussed on the drain side. For the source side the same calculation is performed with V_{ds}=0. Two bias-dependent models are described below.

i) Surface-Potential-Based Model

The surface potential $\phi_{\mathrm{s,over}}$ is calculated in the overlap region in the same manner as in the channel region, and only the polarity is inverted from the channel. The final overlap charge equation is written with the calculated ϕ_{SLD}

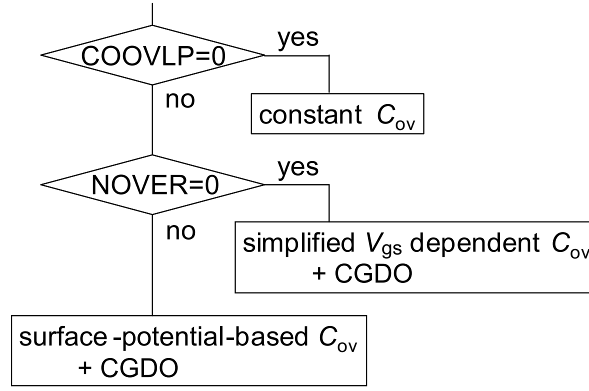

Fig. 18: Model options of the overlap capacitance at the drain side are summarized.

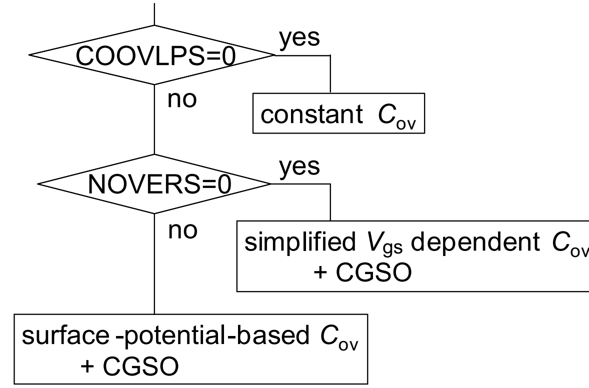

Fig. 19: Model options of the overlap capacitance at the soruce side are summarized.

a) under the depletion and the accumulation conditions

$$Q'_{\text{over}} = \left(\sqrt{\frac{2\epsilon_{\text{Si}} q \mathbf{NOVER}}{\beta}} \sqrt{\beta\phi_{\text{s,over}} - 1} \right)$$
$$Q_{\text{over}} = W_{\text{eff}} \cdot \mathbf{NF} \cdot L_{\text{overLD,mod}} \cdot Q'_{\text{over}} \tag{168}$$

b) under the inversion condition

$$Q_{\text{over}} = W_{\text{eff}} \cdot \mathbf{NF} \cdot L_{\text{overLD,mod}} \cdot C_{\text{ox}}(V_{\text{gs}} - \mathbf{VFBOVER} - \phi_{\text{s,over}}) \tag{169}$$

where $L_{\text{overLD,mod}}$ is the length of the overlap region of the gate over drain, **NOVER** is the impurity concentration in the drift region, and **VFBOVER** is the flat-band voltage in the overlap region. This model is selected, if **NOVER** is not equal to zero.

The potential distribution occurs in the drain side of the drift region underneath the gate overlap before the strong inversion is created. This induces additional charge and the overlap capacitance at the same time. This effect is modeled as

$$Q_{\text{over,d}} = Q_{\text{over}} + W_{\text{eff}} \cdot \mathbf{NF} \cdot \mathbf{QOVADD} \cdot L_{\text{overLD,mod}} \cdot (V_{\text{dp}} - V_{\text{ch}}) \tag{170}$$

$$V_{\text{ch}} = \phi_{\text{SL}} - \phi_{\text{S0}} \tag{171}$$

Three options are provided to calculate ϕ_s, which is selected by the flag **COQOVSM**:

COQOVSM=0: with an analytical equation excluding inversion charge

COQOVSM=1: with iterative procedure

COQOVSM=2: with an analytical equation including inversion charge

The potential value not only at the internal channel/drift junction but also that at the external node can be considered for the overlap capacitance calculation. The model parameter **CVDSOVER** has been introduced to determine the ratio of these two potential contributions as

$$C_{\text{ov}} = (1 - \mathbf{CVDSOVER}) \cdot C_{\text{ov}}(int) + \mathbf{CVDSOVER} \cdot C_{\text{ov}}(ext) \tag{172}$$

where $C_{\text{ov}}(int)$ is the overlap capacitance value calculated with the potential value at the channel/drift junction and $C_{\text{ov}}(ext)$ is that with the external potential value.

$$D_{\text{DRIFT,mod}} = \mathbf{DDRIFT} - \begin{cases} W_{\text{dep,sub}} & \text{(if substrate terminal is activated)} \\ W_{\text{junc,ov}} & \text{(if substrate terminal is not activated)} \end{cases} \tag{173}$$

$$W_{\text{junc,ov}} = \mathbf{QOVJUNC} \cdot \sqrt{\frac{2\epsilon_{\text{Si}}\left(-\phi_{\text{s,over}} + V_{\text{bi}}\right)}{q} \cdot \frac{N_{\text{sub}}}{\mathbf{NOVER}\left(N_{\text{sub}} + \mathbf{NOVER}\right)}} \tag{174}$$

where $W_{\text{dep,sub}}$ is written in Eq. (132). $D_{\text{DRIFT,mod}}$ describes the depletion extension from the surface to the bottom with in the overlap region. The model parameter **QOVJUNC** is introduced to model the modification of **LOVERLD** (see Fig. 20).

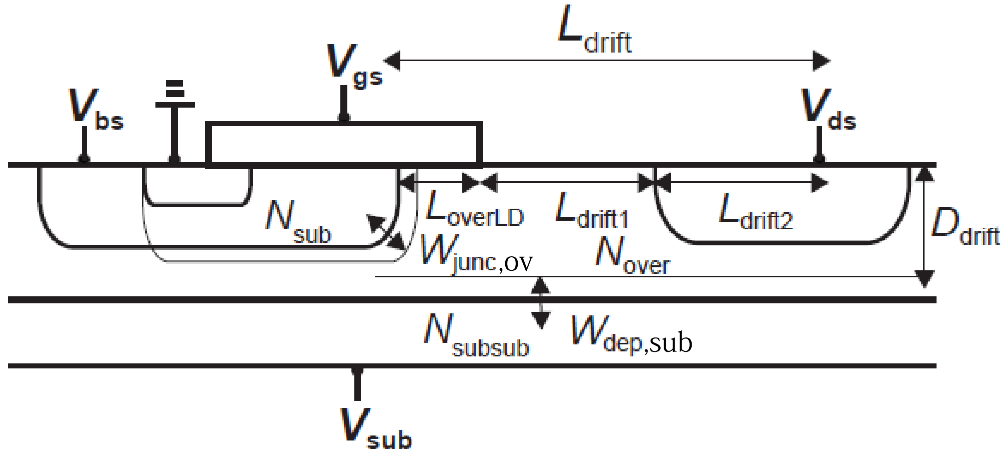

Fig. 20: Schematic of a LDMOS with the substrate node $V_{\text{sub,s}}$

ii) Simplified Bias-Dependent Model

If **LOVERLD** > 0 and the flag **COOVLP** $= 1$, the overlap charge is modeled as

$$Q_{\text{god}} = W_{\text{eff}} \cdot \mathbf{NF} \cdot C_{\text{ox}} \left[(V_{\text{gs}} - V_{\text{ds}}) \mathbf{LOVERLD} - \mathbf{OVSLP} \cdot (1.2 - (\phi_{\text{SL}} - V_{\text{ds}})) \cdot (\mathbf{OVMAG} + (V_{\text{gs}} - V_{\text{ds}})) \right] \tag{175}$$

The overlap capacitance Flags (**COOVLP** = **COOVLPS** = 0) calculates bias-independent overlap capacitances. User-defined values can be specified using the input parameters **CGDO** and **CGSO**. If these values are not specified, the overlap capacitances are calculated using

$$C_{\text{ov}} = -\frac{\epsilon_{\text{ox}}}{\mathbf{TOX}}\mathbf{LOVERLD} \cdot W_{\text{eff}} \cdot \mathbf{NF} \tag{176}$$

The gate-to-bulk overlap capacitance $C_{\text{gbo_loc}}$ is calculated only with a user-defined value **CGBO** using

$$C_{\text{gbo_loc}} = -\mathbf{CGBO} \cdot L_{\text{gate}} \tag{177}$$

independent of the model Flags **COOVLP** and **COOVLPS**.

16.3 Bias-dependent overlap length

$L_{\text{overLD,mod}}$ in Eqs. (168) and (169) can be bias-dependent due to a lateral extension of the depletion region across the channel and drift-region pn-junction.

$$L_{\text{overLD,mod}} = \mathbf{LOVERLD} - W_{\text{junc,ov}} \tag{178}$$

$$W_{\text{junc,ov}} = \mathbf{QOVJUNC} \cdot \sqrt{\frac{2\epsilon_{\text{Si}}\left(V_{\text{x}} + V_{\text{bi}}\right)}{q} \cdot \frac{N_{\text{sub}}}{\mathbf{NOVER}\left(N_{\text{sub}} + \mathbf{NOVER}\right)}} \tag{179}$$

where

$$V_{\text{x}} = \begin{cases} -\phi_{\text{s,over}} & (\mathbf{COOVJUNC}{=}0 \text{ (default)}) \\ V_{\text{db}} & (\mathbf{COOVJUNC}{=}1 \text{ (more reasonable implementation)}) \end{cases} \tag{180}$$

This effect can be easily turned off by setting **QOVJUNC**=0.

16.4 Extrinsic Capacitances

The outer fringing capacitance is modeled as [37]

$$C_{\text{f}} = \frac{\epsilon_{\text{ox}}}{\pi/2} W_{\text{gate}} \cdot \mathbf{NF} \cdot \ln\left(1 + \frac{\mathbf{TPOLY}}{T_{\text{ox}}}\right) \tag{181}$$

where **TPOLY** is the gate-poly thickness. This capacitance is bias independent.

16.5 Trench Overlap Capacitance

The depletion-extension at the channel/overlap junction along the trench overlap region is modeled. To consider the effect, **COTRENCH** must be set to 1. The overlap charge, Q_{over} can be calculated in the same way as in (168) and (169), with the remaining overlap length $L_{\text{overLD,mod}}$ given below.
The modified overlap length along the trench gate is, instead of Eqs. (178) and (179),

$$L_{\text{overLD,mod}} = \mathbf{LOVERLD} + \mathbf{WTRENCH} - W_{\text{junc,ov}} \tag{182}$$

where

$$W_{\text{junc,ov}} = \mathbf{QOVJUNC} \cdot \sqrt{\frac{2\epsilon_{\text{Si}}\left(V_{\text{xdb}} + \mathbf{VBI}\right)}{q} \cdot \frac{N_{\text{sub}}}{\mathbf{NOVER}\left(N_{\text{sub}} + \mathbf{NOVER}\right)}} \tag{183}$$

where **QOVJUNC** describes the modification of the depletion-width extension at the junction due to the $V_{\rm gs}$ control. To obtain a smooth charge storage at the capacitor, $V_{\rm xdb}$ is introduced for an effective voltage difference at the junction calculated by voltage drop $V_{\rm db}$ between the drain and the bulk as:

$$V_{\rm xdb} = \frac{V_{\rm db}}{\left(1 + \left(\frac{V_{\rm db}}{V_{\rm dblim}}\right)^{\bf OLMDLT}\right)^{\frac{1}{\bf OLMDLT}}} \tag{184}$$

$$V_{\rm dblim} = \frac{{\bf LOVERLD}^2}{kjunc} - {\bf VBI} \tag{185}$$

$$kjunc = \frac{2\epsilon_{\rm Si}}{q} \cdot \frac{N_{\rm sub}}{{\bf NOVER}\,(N_{\rm sub} + {\bf NOVER})} \tag{186}$$

The overlap length along the trench bottom side could be different from that of $L_{\rm overLD,mod}$. The modification of **WTRENCH** is done by the model parameter **OLMDLT**. The **OLMDLT** value is fixed, but, it could be reduced in case negative capacitance occurrs.
For trench-gate structures, **CVDSOVER** must be set to zero.

The HiSIM model parameters introduced in section 16 are summarized in Table 16.

Table 16: HiSIM model parameters introduced in section 16 of this manual.

XQY	distance from drain junction to maximum electric field point
***XQY1**	$V_{\rm bs}$ dependence of $Q_{\rm y}$
***XQY2**	$L_{\rm gate}$ dependence of $Q_{\rm y}$
LOVERLD	overlap length of the drift region
LOVERS	overlap length of the source region
LOVER	overlap length of the source region, if **LOVERS** is not determined.
VFBOVER	flat-band voltage in overlap region
***QOVADD**	additional overlap capacitance
QOVJUNC	$W_{\rm junc}$ coefficient for the $L_{\rm overLD}$ modification
***CVDSOVER**	modification of the $C_{\rm gg}$ peak for $V_{\rm ds} \neq 0$ (for **COTRENCH**=0 only)
OVSLP	coefficient for overlap capacitance
OVMAG	coefficient for overlap capacitance
CGSO	gate-to-source overlap capacitance
CGDO	gate-to-drain overlap capacitance
CGBO	gate-to-bulk overlap capacitance
TPOLY	height of the gate poly-Si
CGBO	gate-to-bulk overlap capacitance
TPOLY	height of the gate poly-Si
COTRENCH	model flag for trench-gate capacitance
WTRENCH	trench length (**COTRENCH**=1)
OLMDLT	smoothing exponent for voltage across channel/drift-region pn junction (**COTRENCH**=1)

* indicates minor parameters.

17 Leakage Currents

17.1 Substrate Current

The substrate current is modeled as

$$I_{\mathrm{sub}} = X_{\mathrm{sub1}} \cdot P_{\mathrm{sisubsat}} \cdot I_{\mathrm{ds}} \cdot \exp\left(-\frac{X_{\mathrm{sub2}}}{P_{\mathrm{sisubsat}}}\right) \tag{187}$$

where

$$X_{\mathrm{sub1}} = \mathbf{SUB1} \cdot \left(1 + \frac{\mathbf{SUB1L}}{L_{\mathrm{gate}}^{\mathbf{SUB1LP}}}\right) \cdot X_{\mathrm{subTmp}} \tag{188}$$

$$X_{\mathrm{sub2}} = \mathbf{SUB2} \cdot \left(1 + \frac{\mathbf{SUB2L}}{L_{\mathrm{gate}}}\right) \cdot \frac{1}{X_{\mathrm{subTmp}}} \tag{189}$$

$$P_{\mathrm{sisubsat}} = \mathbf{SVDS} \cdot V_{\mathrm{ds}} + \phi_{\mathrm{S0}} - \frac{L_{\mathrm{gate}} \cdot P_{\mathrm{sislsat}}}{X_{\mathrm{gate}} + L_{\mathrm{gate}}} \tag{190}$$

$$X_{\mathrm{gate}} = \mathbf{SLG} \cdot \left(1 + \frac{\mathbf{SLGL}}{L_{\mathrm{gate}}^{\mathbf{SLGLP}}}\right) \tag{191}$$

$$P_{\mathrm{sislsat}} = V_{\mathrm{g2}} + \frac{q \cdot \epsilon_{\mathrm{Si}} \cdot N_{\mathrm{sub}}}{C_{\mathrm{ox}}^2} \cdot \left\{1 - \sqrt{1 + \frac{2C_{\mathrm{ox}}^2}{q \cdot \epsilon_{\mathrm{Si}} \cdot N_{\mathrm{sub}}} \cdot \left(V_{\mathrm{g2}} - \frac{1}{\beta} - X_{\mathrm{vbs}} \cdot V_{\mathrm{bs}}\right)}\right\} \tag{192}$$

$$X_{\mathrm{vbs}} = \mathbf{SVBS} \cdot \left(1 + \frac{\mathbf{SVBSL}}{L_{\mathrm{gate}}^{\mathbf{SVBSLP}}}\right) \tag{193}$$

$$V_{\mathrm{g2}} = \mathbf{SVGS} \cdot \left(1 + \frac{\mathbf{SVGSL}}{L_{\mathrm{gate}}^{\mathbf{SVGSLP}}}\right) \cdot \frac{W_{\mathrm{gate}}^{\mathbf{SVGSWP}}}{W_{\mathrm{gate}}^{\mathbf{SVGSWP}} + \mathbf{SVGSW}} \cdot V'_{\mathrm{G}} \tag{194}$$

X_{subTmp} is tempetature dependent as following equation

$$X_{\mathrm{subTmp}} = 1.0 + \mathbf{SUBTMP} \cdot (T - \mathbf{TNOM}) \tag{195}$$

17.1.1 Impact-Ionization Induced Bulk Potential Change

The impact ionization induces electron and hole pairs, which is the origin of the substrate current. However, not only the leakage current but also the charge distribtuion in the bulk is changed. This induced charge redistribution affects as the bulk potential change. This is modeled in a simple way as

$$\Delta I_{\rm ds} = \frac{2}{3}\sqrt{\frac{2\epsilon_{\rm Si}qN_{\rm sub}}{\beta}}\Big[\big\{\beta(\phi_{\rm SL}-V_{\rm bs})-1\big\}^{\frac{3}{2}}\frac{3}{2}\frac{\beta\Delta V_{\rm bulk}}{\beta(\phi_{\rm SL}-V_{\rm bs})-1} - \big\{\beta(\phi_{\rm S0}-V_{\rm bs})-1\big\}^{\frac{3}{2}}\frac{3}{2}\frac{\beta\Delta V_{\rm bulk}}{\beta(\phi_{\rm S0}-V_{\rm bs})-1}\Big] - \sqrt{\frac{2\epsilon_{\rm Si}qN_{\rm sub}}{\beta}}\Big[\big\{\beta(\phi_{\rm SL}-V_{\rm bs})-1\big\}^{\frac{1}{2}}\frac{1}{2}\frac{\beta\Delta V_{\rm bulk}}{\beta(\phi_{\rm SL}-V_{\rm bs})-1} - \big\{\beta(\phi_{\rm S0}-V_{\rm bs})-1\big\}^{\frac{1}{2}}\frac{1}{2}\frac{\beta\Delta V_{\rm bulk}}{\beta(\phi_{\rm S0}-V_{\rm bs})-1}\Big] \quad (196)$$

where

$$\Delta V_{\rm bulk} = IBPC1 \cdot (1 + \mathbf{IBPC2} \cdot \Delta V_{\rm th}) \cdot I_{\rm sub} \quad (197)$$

where

$$IBPC1 = \mathbf{IBPC1} \cdot \left(1 + \frac{\mathbf{IBPC1L}}{(L_{\rm gate} \cdot 10^6)^{\mathbf{IBPC1LP}}}\right) \quad (198)$$

and **IBPC1**, **IBPC1L**, **IBPC1LP** and **IBPC2** are model parameters.

Impact-Ionization in Drift Region

With increased $V_{\rm gs}$ the impact ionization occurs in the drift region, which shows exponential characteristics as a function of $V_{\rm gs}$. This type of impact-ionization induced current is modeled as

$$I_{\rm subLD} = I_{\rm ds} \cdot SUBLD1 \cdot E_{\rm y} \cdot L_{\rm drift} \cdot \exp\left(\frac{-\mathbf{SUBLD2}}{E_{\rm y} \cdot f(V_{\rm g}V_{\rm t})}\right) \quad (199)$$

$$E_{\rm y} = \frac{V_{\rm ddp} - \Delta V}{L_{\rm drift}} \quad (200)$$

$$f(V_{\rm g}V_{\rm t}) = \sqrt{Q_{\rm I}/q} \quad (201)$$

$$L_{\rm drift} = \mathbf{LDRIFT1} + \mathbf{LDRIFT2} \quad (202)$$

where ΔV is the potential change due to the stored generated carriers in the overlap region, and is modeled as

$$\Delta V = \mathbf{XPDV} \cdot T0 \cdot \mathbf{XLDLD} \cdot \exp\left(-\frac{a}{T0}\right) \quad (203)$$

$$T0 = V_{\rm ddp} - \mathbf{XPVDTH} \cdot (1 + \mathbf{XPVDTHG} \cdot V_{\rm gs}) \quad (204)$$

where a is unity with voltage dimension. This $I_{\rm subLD}$ is added to the conventional $I_{\rm sub}$. The potential change ΔV is the origin of the expansion effect [57]. The parameter $SUBLD1$ provides the $L_{\rm gate}$ dependence

$$SUBLD1 = \mathbf{SUBLD1} \cdot \left(1 + \frac{\mathbf{SUBLD1L}}{(L_{\rm gate} \cdot 10^6)^{\mathbf{SUBLD1LP}}}\right) \quad (205)$$

17.2 Gate Current

All possible gate leakage currents are schematically shown in Fig. 21.

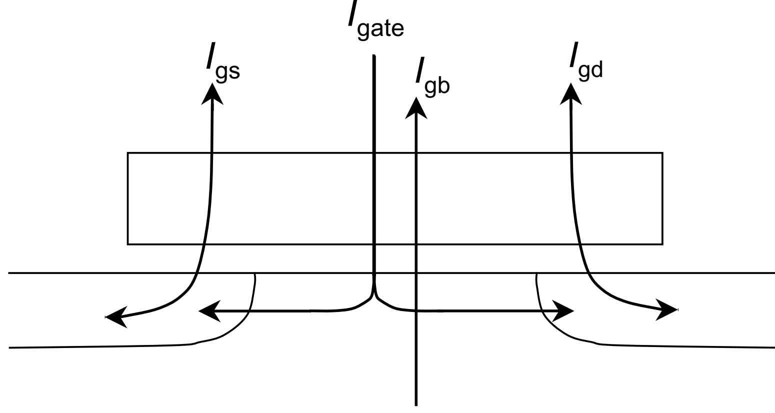

Fig. 21: Gate leakage currents considered.

(i) Between Gate and Channel, $I_{\rm gate}$

As for the current between gate and channel, ($I_{\rm gate}$) the direct-tunneling mechanism is considered [39]. Since measured $I_{\rm gate}$ shows nearly linear $L_{\rm gate}$ dependence, the tunneling is assumed to occur along the whole channel length. Thus the final description implemented in HiSIM is [40, 41]

$$I_{\rm gate} = q \cdot \mathbf{GLEAK1} \cdot \frac{E^2}{E_{\rm gp}^{\frac{1}{2}}} \cdot \exp\left(-\frac{E_{\rm gp}^{\frac{3}{2}} \cdot \mathbf{GLEAK2}}{E}\right) \cdot \sqrt{\frac{Q_{\rm i}}{const0}} \cdot W_{\rm eff} \cdot \mathbf{NF} \cdot L_{\rm eff}$$
$$\cdot \frac{\mathbf{GLEAK6}}{\mathbf{GLEAK6} + V_{\rm ds}} \cdot \frac{\mathbf{GLEAK7}}{\mathbf{GLEAK7} + W_{\rm eff} \cdot \mathbf{NF} \cdot L_{\rm eff}} \tag{206}$$

where

$$E = \frac{\{V_{\rm G} - \mathbf{GLEAK3} \cdot \phi_{\rm S}(\Delta L)\}^2}{T_{\rm ox}} \cdot \left(1 + \frac{E_{\rm y}}{\mathbf{GLEAK5}}\right) \tag{207}$$

$$V_{\rm G} = V_{\rm gs} - \mathbf{VFBC} + \mathbf{GLEAK4} \cdot \Delta V_{\rm th} \cdot L_{\rm eff} \tag{208}$$

$$\Delta V_{\rm th} = \Delta V_{\rm th,SC} + \Delta V_{\rm th,P} + \Delta V_{\rm th,W} - \phi_{\rm Spg} \tag{209}$$

GLEAK1 − 7 are model parameters, and $E_{\rm gp}$ describes the temperture dependent bandgap for the gate current. The gate-channel current $I_{\rm gate}$ is partitioned into two terminal currents with one model parameter in the following manner.

$$I_{\rm gate} = I_{\rm gate,s} + I_{\rm gate,d} \tag{210}$$

where

$$I_{\rm gate,s} = (1 - P_{\rm atition} \cdot I_{\rm gate}) \tag{211}$$

$$I_{\rm gate,d} = P_{\rm artition} \cdot I_{\rm gate} \tag{212}$$

where analytical description of $P_{\rm artition}$ is obtained by integrating the following equation

$$I_{\rm gate,d} = \int_0^{L_{\rm eff}} \frac{y}{L_{\rm eff}} I_{\rm gate}(y) dy = P_{\rm artition} I_{\rm gate} \tag{213}$$

The straightforward simulation result is shown in Fig. 22.

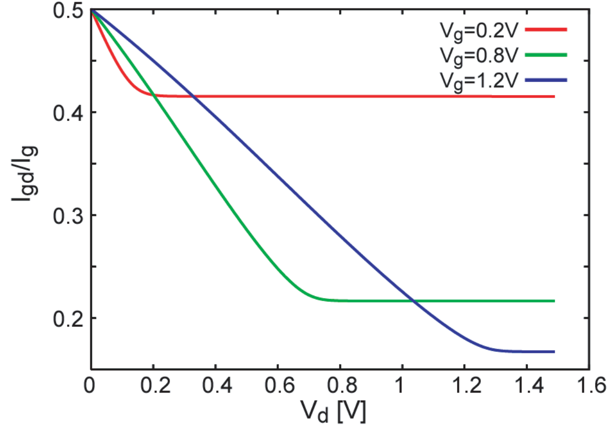

Fig. 22: Exact results of gate partitioning.

(ii) Between Gate and Bulk, I_{gb}

The I_{gb} current under the accumulation condition is modeled as

$$I_{\mathrm{gb}} = \mathbf{GLKB1} \cdot E_{\mathrm{gb}}^2 \cdot \exp\left(-\frac{\mathbf{GLKB2}}{E_{\mathrm{gb}}}\right) W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot L_{\mathrm{eff}} \tag{214}$$

$$E_{\mathrm{gb}} = -\frac{V_{\mathrm{gs}} - \mathbf{VFBC} + \mathbf{GLKB3}}{T_{\mathrm{ox}}} \tag{215}$$

The Fowler-Nordheim tunneling mechanism is also considered

$$I_{\mathrm{FN}} = \frac{q \cdot \mathbf{FN1} \cdot E_{\mathrm{FN}}^2}{E_{\mathrm{g12}}} \cdot \exp\left(-\frac{\mathbf{FN2} \cdot E_{\mathrm{g32}}}{E_{\mathrm{FN}}}\right) \cdot W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot L_{\mathrm{eff}} \tag{216}$$

where

$$E_{\mathrm{FN}} = -\frac{\mathbf{FVBS} \cdot V_{\mathrm{bs}} - (V_{\mathrm{gs}} - \Delta V_{\mathrm{th,SC}} - \Delta V_{\mathrm{th,P}}) - \mathbf{FN3}}{T_{\mathrm{OX}}} \tag{217}$$

$$E_{\mathrm{g32}} = E_{\mathrm{g}} \cdot E_{\mathrm{g12}} \tag{218}$$

$$E_{\mathrm{g12}} = \sqrt{E_{\mathrm{g}}} \tag{219}$$

Total substrate current is the sum of the two components as

$$I_{\mathrm{gb}} = I_{\mathrm{gb}} + I_{\mathrm{FN}} \tag{220}$$

(iii) Between Gate and Source/Drain, $I_{\mathrm{gs}}/I_{\mathrm{gd}}$

The tunneling current between the gate and the source/drain overlap region is modeled as

$$I_{\mathrm{gs}} = sign\mathbf{GLKSD1} \cdot E_{\mathrm{gs}}^2 \exp\left(T_{\mathrm{ox}}(-\mathbf{GLKSD2} \cdot V_{\mathrm{gs}} + \mathbf{GLKSD3})\right) W_{\mathrm{eff}} \cdot \mathbf{NF} \tag{221}$$

$$E_{\mathrm{gs}} = \frac{V_{\mathrm{gs}}}{T_{\mathrm{ox}}} \tag{222}$$

$$I_{\rm gd} = sign\mathbf{GLKSD1} \cdot E_{\rm gd}^2 \exp\left(T_{\rm ox}(\mathbf{GLKSD2} \cdot (-V_{\rm gs} + V_{\rm ds}) + \mathbf{GLKSD3})\right) W_{\rm eff} \cdot \mathbf{NF} \tag{223}$$

$$E_{\rm gd} = \frac{V_{\rm gs} - V_{\rm ds}}{T_{\rm ox}} \tag{224}$$

$$sign = +1 \quad \text{for} \quad E \leq 0$$
$$sign = -1 \quad \text{for} \quad E \geq 0$$

17.3 GIDL (Gate-Induced Drain Leakage)

The GIDL current is generated at the drain junction under the accumulation condition. The $V_{\rm ds}$ increase induces a very narrow potential well in the drain just under the gate, causing carrier generation. Therefore, the GIDL current is strongly dependent on $V_{\rm ds}$. At further reduced $V_{\rm gs}$ values the direct gate tunneling starts to dominate the $I_{\rm GIDL}$ measurements, resulting in $V_{\rm ds}$ independence. The $V_{\rm ds}$ dependent $I_{\rm GIDL}$ is modeled here. The generation mechanism is considered to be the direct tunneling between the above mentioned narrow potential well of length ΔY and the ordinary drain region.

$$I_{\rm GIDL} = \alpha I_{\rm ds} \Delta Y \tag{225}$$

The generation occurs only in this ΔY region at the drain. The final equation is

$$I_{\rm GIDL} = q \cdot \mathbf{GIDL1} \cdot \frac{E^2}{E_{\rm g}^{\frac{1}{2}}} \cdot \exp\left(-\mathbf{GIDL2} \cdot \frac{E_{\rm g}^{\frac{3}{2}}}{E}\right) \cdot W_{\rm eff} \cdot \mathbf{NF} \cdot A \tag{226}$$

where

$$E = \frac{\mathbf{GIDL3} \cdot (V_{\rm ds} + \mathbf{GIDL4}) - V_{\rm G}'}{T_{\rm ox}} \tag{227}$$

$$V_{\rm G}' = V_{\rm gs} + \Delta V_{\rm th} \cdot \mathbf{GIDL5} \tag{228}$$

and A is introduced after BSIM4 as

$$A = \left(\frac{V_{\rm db}^3}{V_{\rm db}^3 + 0.5}\right) \tag{229}$$

$$V_{\rm db} = V_{\rm ds} - V_{\rm bs} \tag{230}$$

Here $\Delta V_{\rm th}$ is defined as

$$\Delta V_{\rm th} = \Delta V_{\rm th,SC} + \Delta V_{\rm th,P} \tag{231}$$

The GISL current is calculated with the same equation as the GIDL current described above. The selection either $I_{\rm GIDL}$ or $I_{\rm GISL}$ is done by the polarity of the current flow.

The HiSIM model parameters introduced in section 17 are summarized in Table 17.

Table 17: HiSIM model parameters introduced in section 17 of this manual. $*$ indicates minor parameters.

SUB1	substrate current coefficient of magnitude
SUB1L	$L_{\rm gate}$ dependence **SUB1**
SUB1LP	$L_{\rm gate}$ dependence **SUB1**
SUB2	substrate current coefficient of exponential term
SUB2L	$L_{\rm gate}$ dependence of **SUB2**
SUBTMP	temperature dependence of Isub
SVDS	substrate current dependence on $V_{\rm ds}$
SLG	substrate current dependence on $L_{\rm gate}$
SLGL	substrate current dependence on $L_{\rm gate}$
SLGLP	substrate current dependence on $L_{\rm gate}$
SVBS	substrate current dependence on $V_{\rm bs}$
SVBSL	$L_{\rm gate}$ dependence of **SVBS**
SVBSLP	$L_{\rm gate}$ dependence of **SVBS**
SVGS	substrate current dependence on $V_{\rm gs}$
SVGSL	$L_{\rm gate}$ dependence of **SVGS**
SVGSLP	$L_{\rm gate}$ dependence of **SVGS**
SVGSW	$W_{\rm gate}$ dependence of **SVGS**
SVGSWP	$W_{\rm gate}$ dependence of **SVGS**
IBPC1	impact-ionization induced bulk potential change
IBPC1L	$L_{\rm gate}$ length dependence of impact-ionization induced bulk potential change
IBPC1LP	$L_{\rm gate}$ length dependence of impact-ionization induced bulk potential change
IBPC2	impact-ionization induced bulk potential change
SUBLD1	substrate current induced in $L_{\rm drift}$
SUBLD1L	$L_{\rm gate}$ length dependence of substrate current induced in $L_{\rm drift}$
SUBLD1LP	$L_{\rm gate}$ length dependence of substrate current induced in $L_{\rm drift}$
SUBLD2	substrate current induced in $L_{\rm drift}$
XPDV	potential change for expansion effect
XPVDTH	potential change for expansion effect
XPVDTHG	potential change for expansion effect
GLEAK1	gate to channel current coefficient
GLEAK2	gate to channel current coefficient
GLEAK3	gate to channel current coefficient
GLEAK4	gate to channel current coefficient
$*$**GLEAK5**	gate to channel current coefficient (short channel correction)
$*$**GLEAK6**	gate to channel current coefficient ($V_{\rm ds}$ dependence correction)
$*$**GLEAK7**	gate to channel current coefficient (gate length and width dependence correction)
$*$**EGIG**	bandgap of gate leakage
$*$**IGTEMP2**	temperature dependence of gate leakage
$*$**IGTEMP3**	temperature dependence of gate leakage
GLKB1	gate to bulk current coefficient
GLKB2	gate to bulk current coefficient
GLKB3	flat-band shift for gate to bulk current
GLKSD1	gate to source/drain current coefficient
GLKSD2	gate to source/drain current coefficient
GLKSD3	gate to source/drain current coefficient
GLPART1	partitioning ratio of gate leakage current
FN1	coefficient of Fowler-Nordheim-current contribution
FN2	coefficient of Fowler-Nordheim-current contribution
FN3	coefficient of Fowler-Nordheim-current contribution
FVBS	$V_{\rm bs}$ dependence of Fowler-Nordheim current
GIDL1	magnitude of the GIDL
GIDL2	field dependence of the GIDL
GIDL3	$V_{\rm ds}$ dependence of the GIDL
$*$**GIDL4**	threshold of $V_{\rm ds}$ dependence
$*$**GIDL5**	correction of high-field contribution

18 Source/Bulk and Drain/Bulk Diode Models

Four P/N junctions are available within the MOSFET structure and corresponding input voltages across the junctions are followings:

$$V_{\mathrm{bd}} = \mathrm{V(DB,D)} \tag{232}$$

$$V_{\mathrm{bdi}} = \mathrm{V(BP,DP)} \tag{233}$$

$$V_{\mathrm{bs}} = \mathrm{V(SB,S)} \tag{234}$$

$$V_{\mathrm{bsi}} = \mathrm{V(BP,SP)} \tag{235}$$

where the branch (DB,D) handles the drain-side outer diode, (BP,DP) the drain-side inner diode, (SB,S) the source-side outer diode, (BP,SP) the source-side inner diode.

18.1 Diode Current

The model equations for the source/bulk and drain/bulk diode currents are based on the concepts of BSIM3v3 [43], but include a number of modifications. The two regions denoted (a) and (b) in the schematic diagram of Fig. 23, are distinguished in the modeling and are treated separately.

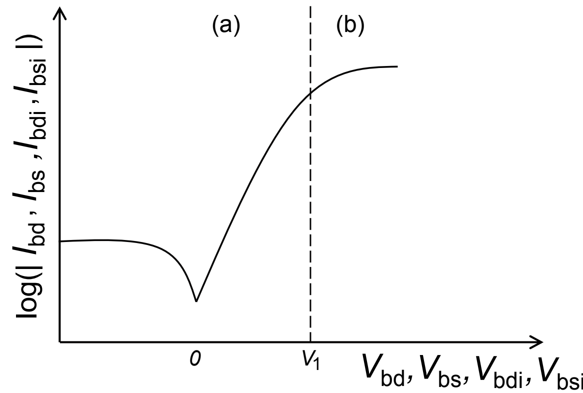

Fig. 23: The four I_{diode} currents (I_{bd}, I_{bs}, I_{bdi} and I_{bsi}) are modeled separately in the two different operating regions (a) and (b). Border of the two regions is V_1 which is written in (258).

Two model options: Conventional model (**CODIO** $= 0$) and the extended model (**CODIO** $= 1$) are available in the versions 2.4.0 and later.

The notations $\Theta = S,\ \theta = s$ (for source/bulk junction) and $\Theta = D,\ \theta = d$ (for drain/bulk junction) apply.

18.1.1 Conventional Model (CODIO $= 0$)

I_{bd} contributes to the drain-side outer branch (DB,D) and I_{bs} contributes to the source-side outer branch (SB,S). In this conventional option, the inner diode branches (BP,DP) and (BP,SP) are missing: $I_{\mathrm{bdi}} = 0$

and $I_{\mathrm{bsi}} = 0$. The resulting diode current equations for the outer diode branches (DB,D) and (SB,S) are derived separately in the 2 regions (a) and (b) as follows.

a) $V_{\mathrm{b}\theta} < V_1$ **(Original Equation)**

$$\begin{aligned} I_{\mathrm{b}\theta} =& I_{\mathrm{sb}\theta} \left\{ \exp\left(\frac{V_{\mathrm{b}\theta}}{N_{\mathrm{vtm}}}\right) - 1 \right\} \\ &+ I_{\mathrm{sb}\theta 2} \cdot C_{\mathrm{isb}} \cdot \left\{ \exp\left(- \frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\ &+ \mathbf{CISBK\Theta} \cdot \left\{ \exp\left(- \frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\ &+ \mathbf{DIVX\Theta} \cdot I_{\mathrm{sb}\theta 2} \cdot V_{\mathrm{b}\theta} \end{aligned} \tag{236}$$

b) $V_{\mathrm{b}\theta} \geq V_1$ **(Linearized Equation)**

$$\begin{aligned} I_{\mathrm{b}\theta} =& I_{\mathrm{sb}\theta} \left\{ \exp\left(\frac{V_1}{N_{\mathrm{vtm}}}\right) - 1 \right\} + \frac{I_{\mathrm{sb}\theta}}{N_{\mathrm{vtm}}} \exp\left(\frac{V_1}{N_{\mathrm{vtm}}}\right) (V_{\mathrm{b}\theta} - V_1) \\ &+ I_{\mathrm{sb}\theta 2} \cdot C_{\mathrm{isb}} \left\{ \exp\left(- \frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\ &+ \mathbf{CISBK\Theta} \left\{ \exp\left(- \frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\ &+ \mathbf{DIVX\Theta} \cdot I_{\mathrm{sb}\theta 2} \cdot V_{\mathrm{b}\theta} \end{aligned} \tag{237}$$

where $I_{\mathrm{sb}\theta}$ and $I_{\mathrm{sb}\theta 2}$ are written as

$$I_{\mathrm{sb}\theta} = A\Theta \cdot j_{\mathrm{s}} + P\Theta \cdot j_{\mathrm{ssw}} \tag{238}$$

$$I_{\mathrm{sb}\theta 2} = A\Theta \cdot j_{\mathrm{s2}} + P\Theta \cdot j_{\mathrm{ssw2}} \tag{239}$$

where $A\Theta$ is the area parameter and $P\Theta$ is the perimeter parameter of the drain or source region.

18.1.2 Extended Model (CODIO = 1)

$$I_{\mathrm{bd}} = I_{\mathrm{bd,btm}} + I_{\mathrm{bd,sws}} \quad \text{contributed to the outer branch (DB,D)} \tag{240}$$

$$I_{\mathrm{bdi}} = I_{\mathrm{bd,swg}} \quad \text{contributed to the inner branch (BP,DP)} \tag{241}$$

$$I_{\mathrm{bs}} = I_{\mathrm{bs,btm}} + I_{\mathrm{bs,sws}} \quad \text{contributed to the outer branch (SB,S)} \tag{242}$$

$$I_{\mathrm{bsi}} = I_{\mathrm{bs,swg}} \quad \text{contributed to the inner branch (BP,SP)} \tag{243}$$

a) $V_{\mathrm{b}\theta} < V_1$ **(Original Equations)**

$$\begin{aligned} I_{\mathrm{b}\theta,\mathrm{btm}} =& I_{\mathrm{sb}\theta,\mathrm{btm}} \left\{ \exp\left(\frac{V_{\mathrm{b}\theta}}{N_{\mathrm{vtm}}}\right) - 1 \right\} \\ &+ I_{\mathrm{sb}\theta 2,\mathrm{btm}} \cdot C_{\mathrm{isb}} \cdot \left\{ \exp\left(- \frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\ &+ \mathbf{CISBK\Theta} \cdot \left\{ \exp\left(- \frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\ &+ \mathbf{DIVX\Theta} \cdot I_{\mathrm{sb}\theta 2,\mathrm{btm}} \cdot V_{\mathrm{b}\theta} \end{aligned} \tag{244}$$

$$
\begin{aligned}
I_{\mathrm{b}\theta,\mathrm{sws}} =& I_{\mathrm{sb}\theta,\mathrm{sws}} \left\{ \exp\left(\frac{V_{\mathrm{b}\theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ I_{\mathrm{sb}\theta 2,\mathrm{sws}} \cdot C_{\mathrm{isb}} \cdot \left\{ \exp\left(-\frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ \mathbf{CISBK\Theta} \cdot \left\{ \exp\left(-\frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ \mathbf{DIVX\Theta} \cdot I_{\mathrm{sb}\theta 2,\mathrm{sws}} \cdot V_{\mathrm{b}\theta}
\end{aligned}
\tag{245}
$$

$$
\begin{aligned}
I_{\mathrm{b}\theta,\mathrm{swg}} =& I_{\mathrm{sb}\theta,\mathrm{swg}} \left\{ \exp\left(\frac{V_{\mathrm{b}\theta\mathrm{i}}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ I_{\mathrm{sb}\theta 2,\mathrm{swg}} \cdot C_{\mathrm{isb}} \cdot \left\{ \exp\left(-\frac{V_{\mathrm{b}\theta\mathrm{i}} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ \mathbf{CISBK\Theta} \cdot \left\{ \exp\left(-\frac{V_{\mathrm{b}\theta\mathrm{i}} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ \mathbf{DIVX\Theta} \cdot I_{\mathrm{sb}\theta 2,\mathrm{swg}} \cdot V_{\mathrm{b}\theta\mathrm{i}}
\end{aligned}
\tag{246}
$$

b) $V_{\mathrm{b}\theta} \geq V_1$ (Linearized Equations)

$$
\begin{aligned}
I_{\mathrm{b}\theta,\mathrm{btm}} =& I_{\mathrm{sb}\theta,\mathrm{btm}} \left\{ \exp\left(\frac{V_1}{N_{\mathrm{vtm}}} \right) - 1 \right\} + \frac{I_{\mathrm{sb}\theta,\mathrm{btm}}}{N_{\mathrm{vtm}}} \exp\left(\frac{V_1}{N_{\mathrm{vtm}}} \right) (V_{\mathrm{b}\theta} - V_1) \\
&+ I_{\mathrm{sb}\theta 2,\mathrm{btm}} \cdot C_{\mathrm{isb}} \left\{ \exp\left(-\frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ \mathbf{CISBK\Theta} \left\{ \exp\left(-\frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ \mathbf{DIVX\Theta} \cdot I_{\mathrm{sb}\theta 2,\mathrm{btm}} \cdot V_{\mathrm{b}\theta}
\end{aligned}
\tag{247}
$$

$$
\begin{aligned}
I_{\mathrm{b}\theta,\mathrm{sws}} =& I_{\mathrm{sb}\theta,\mathrm{sws}} \left\{ \exp\left(\frac{V_1}{N_{\mathrm{vtm}}} \right) - 1 \right\} + \frac{I_{\mathrm{sb}\theta,\mathrm{sws}}}{N_{\mathrm{vtm}}} \exp\left(\frac{V_1}{N_{\mathrm{vtm}}} \right) (V_{\mathrm{b}\theta} - V_1) \\
&+ I_{\mathrm{sb}\theta 2,\mathrm{sws}} \cdot C_{\mathrm{isb}} \left\{ \exp\left(-\frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ \mathbf{CISBK\Theta} \left\{ \exp\left(-\frac{V_{\mathrm{b}\theta} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ \mathbf{DIVX\Theta} \cdot I_{\mathrm{sb}\theta 2,\mathrm{sws}} \cdot V_{\mathrm{b}\theta}
\end{aligned}
\tag{248}
$$

$$
\begin{aligned}
I_{\mathrm{b}\theta,\mathrm{swg}} =& I_{\mathrm{sb}\theta,\mathrm{swg}} \left\{ \exp\left(\frac{V_1}{N_{\mathrm{vtm}}} \right) - 1 \right\} + \frac{I_{\mathrm{sb}\theta,\mathrm{swg}}}{N_{\mathrm{vtm}}} \exp\left(\frac{V_1}{N_{\mathrm{vtm}}} \right) (V_{\mathrm{b}\theta\mathrm{i}} - V_1) \\
&+ I_{\mathrm{sb}\theta 2,\mathrm{swg}} \cdot C_{\mathrm{isb}} \left\{ \exp\left(-\frac{V_{\mathrm{b}\theta\mathrm{i}} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ \mathbf{CISBK\Theta} \left\{ \exp\left(-\frac{V_{\mathrm{b}\theta\mathrm{i}} \cdot \mathbf{CVB\Theta}}{N_{\mathrm{vtm}}} \right) - 1 \right\} \\
&+ \mathbf{DIVX\Theta} \cdot I_{\mathrm{sb}\theta 2,\mathrm{swg}} \cdot V_{\mathrm{b}\theta\mathrm{i}}
\end{aligned}
\tag{249}
$$

where

$$
I_{\mathrm{sb}\theta} = I_{\mathrm{sb}\theta,\mathrm{btm}} + I_{\mathrm{sb}\theta,\mathrm{sws}} + I_{\mathrm{sb}\theta,\mathrm{swg}}
\tag{250}
$$

where

$$I_{\mathrm{sb}\theta,\mathrm{btm}} = A\Theta \cdot j_{\mathrm{s}} \tag{251}$$

$$I_{\mathrm{sb}\theta,\mathrm{sws}} = \begin{cases} (P\Theta - W_{\mathrm{eff}} \cdot \mathbf{NF}) \cdot j_{\mathrm{ssw}} & (P\Theta > W_{\mathrm{eff}} \cdot \mathbf{NF}) \\ 0 & (P\Theta \leq W_{\mathrm{eff}} \cdot \mathbf{NF}) \end{cases} \tag{252}$$

$$I_{\mathrm{sb}\theta,\mathrm{swg}} = \begin{cases} W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot j_{\mathrm{sswg}} & (P\Theta > W_{\mathrm{eff}} \cdot \mathbf{NF}) \\ P\Theta \cdot j_{\mathrm{sswg}} & (P\Theta \leq W_{\mathrm{eff}} \cdot \mathbf{NF}) \end{cases} \tag{253}$$

$$I_{\mathrm{sb}\theta 2,\mathrm{btm}} = A\Theta \cdot j_{\mathrm{s2}} \tag{254}$$

$$I_{\mathrm{sb}\theta 2,\mathrm{sws}} = \begin{cases} (P\Theta - W_{\mathrm{eff}} \cdot \mathbf{NF}) \cdot j_{\mathrm{ssw2}} & (P\Theta > W_{\mathrm{eff}} \cdot \mathbf{NF}) \\ 0 & (P\Theta \leq W_{\mathrm{eff}} \cdot \mathbf{NF}) \end{cases} \tag{255}$$

$$I_{\mathrm{sb}\theta 2,\mathrm{swg}} = \begin{cases} W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot j_{\mathrm{sswg2}} & (P\Theta > W_{\mathrm{eff}} \cdot \mathbf{NF}) \\ P\Theta \cdot j_{\mathrm{sswg2}} & (P\Theta \leq W_{\mathrm{eff}} \cdot \mathbf{NF}) \end{cases} \tag{256}$$

18.1.3 Common Equations to CODIO Options

$$N_{\mathrm{vtm}} = \frac{\mathbf{NJ\Theta}}{\beta} \tag{257}$$

$$V_1 = N_{\mathrm{vtm}} \cdot \log\left(\frac{V_{\mathrm{diffj}}}{I_{\mathrm{sb}\theta}} + 1\right) \tag{258}$$

$$V_{\mathrm{diffj}} = \mathbf{VDIFFJ\Theta} \cdot (T_{\mathrm{tnom}})^2 \tag{259}$$

$$C_{\mathrm{isb}} = \mathbf{CISB\Theta} \cdot \exp\left((T_{\mathrm{tnom}} - 1) \cdot \mathbf{CTEMP\Theta}\right) \tag{260}$$

The models for forward-biased current densities, describing the area and sidewall components of the source/drain regions, are given in Eqs. (262) and (263), respectively. The corresponding backward-biased current densities are given in Eqs. (265) and (266).

$$T_{\mathrm{tnom}} = \frac{T}{\mathbf{TNOM}} \tag{261}$$

$$j_{\mathrm{s}} = \mathbf{JS0\Theta} \cdot \exp\left(\frac{(E_{\mathrm{g}}(T = \mathbf{TNOM}) \cdot \beta(T = \mathbf{TNOM}) - E_{\mathrm{g}}\beta + \mathbf{XTI\Theta} \cdot \log(T_{\mathrm{tnom}}))}{\mathbf{NJ\Theta}}\right) \tag{262}$$

$$j_{\mathrm{ssw}} = \mathbf{JS0SW\Theta} \cdot \exp\left(\frac{(E_{\mathrm{g}}(T = \mathbf{TNOM}) \cdot \beta(T = \mathbf{TNOM}) - E_{\mathrm{g}}\beta + \mathbf{XTI\Theta} \cdot \log(T_{\mathrm{tnom}}))}{\mathbf{NJSW\Theta}}\right) \tag{263}$$

$$j_{\mathrm{sswg}} = \mathbf{JS0SWG\Theta} \cdot \exp\left(\frac{(E_{\mathrm{g}}(T = \mathbf{TNOM}) \cdot \beta(T = \mathbf{TNOM}) - E_{\mathrm{g}}\beta + \mathbf{XTI\Theta} \cdot \log(T_{\mathrm{tnom}}))}{\mathbf{NJSWG\Theta}}\right) \tag{264}$$

$$j_{\mathrm{s2}} = \mathbf{JS0\Theta} \cdot \exp\left(\frac{(E_{\mathrm{g}}(T = \mathbf{TNOM}) \cdot \beta(T = \mathbf{TNOM}) - E_{\mathrm{g}}\beta + \mathbf{XTI2\Theta} \cdot \log(T_{\mathrm{tnom}}))}{\mathbf{NJ\Theta}}\right) \tag{265}$$

$$j_{\mathrm{ssw2}} = \mathbf{JS0SW\Theta} \cdot \exp\left(\frac{(E_{\mathrm{g}}(T = \mathbf{TNOM}) \cdot \beta(T = \mathbf{TNOM}) - E_{\mathrm{g}}\beta + \mathbf{XTI2\Theta} \cdot \log(T_{\mathrm{tnom}}))}{\mathbf{NJSW\Theta}}\right) \tag{266}$$

$$j_{\mathrm{sswg2}} = \mathbf{JS0SWG\Theta} \cdot \exp\left(\frac{(E_{\mathrm{g}}(T = \mathbf{TNOM}) \cdot \beta(T = \mathbf{TNOM}) - E_{\mathrm{g}}\beta + \mathbf{XTI2\Theta} \cdot \log(T_{\mathrm{tnom}}))}{\mathbf{NJSWG\Theta}}\right) \tag{267}$$

18.2 Diode Capacitance

The diode capacitances of the source/bulk junction C_{apbs} and of the drain/bulk junction C_{apbd} are given by the following equations. These equations have the same basis as those used in BSIM3v3 [43], but include a number of minor modifications.

18.2.1 Conventional Model (CODIO = 0)

$$Q_{\mathrm{bd}} = Q_{\mathrm{bd,btm}}(V_{\mathrm{bd}}) + Q_{\mathrm{bd,sws}}(V_{\mathrm{bd}}) + Q_{\mathrm{bd,swg}}(V_{\mathrm{bd}}) \quad \text{to the branch (DB,D)} \tag{268}$$

$$Q_{\mathrm{bdi}} = 0 \quad \text{to the branch (BP,DP)} \tag{269}$$

$$Q_{\mathrm{bs}} = Q_{\mathrm{bs,btm}}(V_{\mathrm{bs}}) + Q_{\mathrm{bs,sws}}(V_{\mathrm{bs}}) + Q_{\mathrm{bs,swg}}(V_{\mathrm{bs}}) \quad \text{to the branch (SB,S)} \tag{270}$$

$$Q_{\mathrm{bsi}} = 0 \quad \text{to the branch (BP,SP)} \tag{271}$$

where the argument for each charge expression is referred to as V_{arg} in Subsubsection 18.2.3.

18.2.2 Extended Model (CODIO = 1)

$$Q_{\mathrm{bd}} = Q_{\mathrm{bd,btm}}(V_{\mathrm{bd}}) + Q_{\mathrm{bd,sws}}(V_{\mathrm{bd}}) \quad \text{to the branch (DB,D)} \tag{272}$$

$$Q_{\mathrm{bdi}} = Q_{\mathrm{bd,swg}}(V_{\mathrm{bdi}}) \quad \text{to the branch (BP,DP)} \tag{273}$$

$$Q_{\mathrm{bs}} = Q_{\mathrm{bs,btm}}(V_{\mathrm{bs}}) + Q_{\mathrm{bs,sws}}(V_{\mathrm{bs}}) \quad \text{to the branch (SB,S)} \tag{274}$$

$$Q_{\mathrm{bsi}} = Q_{\mathrm{bs,swg}}(V_{\mathrm{bsi}}) \quad \text{to the branch (BP,SP)} \tag{275}$$

where the argument for each charge expression is referred to as V_{arg} in Subsubsection 18.2.3.

18.2.3 Common Equations to CODIO Options

The notations $\Theta = S,\ \theta = s$ (for source/bulk junction) and
$\Theta = D,\ \theta = d$ (for drain/bulk junction) apply.

(i) $V_{\mathrm{arg}} < 0$

$$Q_{\mathrm{b}\theta,\mathrm{btm}}(V_{\mathrm{arg}}) = \frac{\mathbf{PB\Theta} \cdot c_{\mathrm{zb}\theta}\{1 - (1 - \frac{V_{\mathrm{arg}}}{\mathbf{PB\Theta}})^{1-\mathbf{MJ\Theta}}\}}{1 - \mathbf{MJ\Theta}} \tag{276}$$

$$Q_{\mathrm{b}\theta,\mathrm{sws}}(V_{\mathrm{arg}}) = \frac{\mathbf{PBSW\Theta} \cdot c_{\mathrm{zb}\theta\mathrm{sw}}\{1 - (1 - \frac{V_{\mathrm{arg}}}{\mathbf{PBSW\Theta}})^{1.0-\mathbf{MJSW\Theta}}\}}{1.0 - \mathbf{MJSW\Theta}} \tag{277}$$

$$Q_{\mathrm{b}\theta,\mathrm{swg}}(V_{\mathrm{arg}}) = \frac{\mathbf{PBSWG\Theta} \cdot c_{\mathrm{zb}\theta\mathrm{swg}}\{1 - (1 - \frac{V_{\mathrm{arg}}}{\mathbf{PBSWG\Theta}})^{1-\mathbf{MJSWG\Theta}}\}}{1 - \mathbf{MJSWG\Theta}} \tag{278}$$

(ii) $V_{\rm arg} \geq 0$

$$Q_{{\rm b}\theta,{\rm btm}}(V_{\rm arg}) = c_{{\rm zb}\theta} \cdot V_{\rm arg} + \frac{1}{2}\frac{c_{{\rm zb}\theta} \cdot \mathbf{MJ\Theta}}{\mathbf{PB\Theta}} \cdot V_{\rm arg}^2 \tag{279}$$

$$Q_{{\rm b}\theta,{\rm sws}}(V_{\rm arg}) = c_{{\rm zb}\theta{\rm sw}} \cdot V_{\rm arg} + \frac{1}{2}\frac{c_{{\rm zb}\theta{\rm sw}} \cdot \mathbf{MJSW\Theta}}{\mathbf{PBSW\Theta}} \cdot V_{\rm arg}^2 \tag{280}$$

$$Q_{{\rm b}\theta,{\rm swg}}(V_{\rm arg}) = c_{{\rm zb}\theta{\rm swg}} \cdot V_{\rm arg} + \frac{1}{2}\frac{c_{{\rm zb}\theta{\rm swg}} \cdot \mathbf{MJSWG\Theta}}{\mathbf{PBSWG\Theta}} \cdot V_{\rm arg}^2 \tag{281}$$

where

$$c_{{\rm zb}\theta} = \mathbf{CJ\Theta} \cdot A\Theta \tag{282}$$

$$c_{{\rm zb}\theta{\rm sw}} = \begin{cases} \mathbf{CJSW\Theta} \cdot (P\Theta - W_{\rm eff} \cdot \mathbf{NF}) & (P\Theta > W_{\rm eff} \cdot \mathbf{NF}) \\ 0 & (P\Theta \leq W_{\rm eff} \cdot \mathbf{NF}) \end{cases} \tag{283}$$

$$c_{{\rm zb}\theta{\rm swg}} = \begin{cases} \mathbf{CJSWG\Theta} \cdot W_{\rm eff} \cdot \mathbf{NF} & (P\Theta > W_{\rm eff} \cdot \mathbf{NF}) \\ \mathbf{CJSWG\Theta} \cdot P\Theta & (P\Theta \leq W_{\rm eff} \cdot \mathbf{NF}) \end{cases} \tag{284}$$

where

$$\mathbf{CJ\Theta} = \mathbf{CJ\Theta} \cdot (1 + \mathbf{TCJB\Theta} \cdot (T - \mathbf{TNOM})) \tag{285}$$

$$\mathbf{CJSW\Theta} = \mathbf{CJSW\Theta} \cdot (1 + \mathbf{TCJB\Theta SW} \cdot (T - \mathbf{TNOM})) \tag{286}$$

$$\mathbf{CJSWG\Theta} = \mathbf{CJSWG\Theta} \cdot (1 + \mathbf{TCJB\Theta SWG} \cdot (T - \mathbf{TNOM})) \tag{287}$$

The HiSIM model parameters introduced in section 18 are summarized in Table 18.

Table 18: HiSIM model parameters introduced in section 18 of this manual. # indicates instance parameters.

JS0	saturation current density
JS0D	saturation current density for drain junction
JS0S	saturation current density for source junction
JS0SW	sidewall saturation current density
JS0SWD	sidewall saturation current density for drain junction
JS0SWS	sidewall saturation current density for source junction
JS0SWG	gate-side saturation current density (**CODIO**=1)
JS0SWGD	gate-side saturation current density for drain junction (**CODIO**=1)
JS0SWGS	gate-side saturation current density for source junction (**CODIO**=1)
NJ	emission coefficient
NJD	emission coefficient for drain junction
NJS	emission coefficient for source junction
NJSW	sidewall emission coefficient
NJSWD	sidewall emission coefficient for drain junction
NJSWS	sidewall emission coefficient for source junction
NJSWG	gate sidewall emission coefficient
NJSWGD	gate sidewall emission coefficient for drain junction
NJSWGS	gate sidewall emission coefficient for source junction
XTI	temperature coefficient for forward-current densities
XTID	temperature coefficient for forward-current densities for drain junction
XTIS	temperature coefficient for forward-current densities for source junction
XTI2	temperature coefficient for reverse-current densities
XTI2D	temperature coefficient for reverse-current densities for drain junction
XTI2S	temperature coefficient for reverse-current densities for source junction
DIVX	reverse current coefficient
DIVXD	reverse current coefficient for drain junction
DIVXS	reverse current coefficient for source junction
CISB	reverse biased saturation current
CISBD	reverse biased saturation current for drain junction
CISBS	reverse biased saturation current for source junction
CVB	bias dependence coefficient of **CISB**
CVBD	bias dependence coefficient of **CISB** for drain junction
CVBS	bias dependence coefficient of **CISB** for source junction
CTEMP	temperature coefficient of reverse currents
CISBK	reverse biased saturation current (at low temperature)
CISBKD	reverse biased saturation current (at low temperature) for drain junction
CISBKS	reverse biased saturation current (at low temperature) for source junction
VDIFFJ	diode threshold voltage between source/drain and substrate
VDIFFJD	diode threshold voltage between drain and substrate
VDIFFJS	diode threshold voltage between source and substrate
CJ	bottom junction capacitance per unit area at zero bias
CJD	bottom junction capacitance per unit area at zero bias for drain junction
CJS	bottom junction capacitance per unit area at zero bias for source junction
CJSW	source/drain sidewall junction cap. grading coefficient per unit length at zero bias
CJSWD	drain sidewall junction cap. grading coefficient per unit length at zero bias
CJSWS	source sidewall junction cap. grading coefficient per unit length at zero bias
CJSWG	source/drain sidewall junction capacitance per unit length at zero bias
CJSWGD	drain sidewall junction capacitance per unit length at zero bias
CJSWGS	source sidewall junction capacitance per unit length at zero bias
MJ	bottom junction capacitance grading coefficient
MJD	bottom junction capacitance grading coefficient for drain junction
MJS	bottom junction capacitance grading coefficient for source junction
MJSW	source/drain sidewall junction capacitance grading coefficient
MJSWD	drain sidewall junction capacitance grading coefficient
MJSWS	source sidewall junction capacitance grading coefficient
MJSWG	source/drain gate sidewall junction capacitance grading coefficient

PB	bottom junction build-in potential
PBD	bottom junction build-in potential for drain junction
PBS	bottom junction build-in potential for source junction
PBSW	source/drain sidewall junction build-in potential
PBSWD	drain sidewall junction build-in potential
PBSWS	source sidewall junction build-in potential
PBSWG	source/drain gate sidewall junction build-in potential
PBSWGD	drain gate sidewall junction build-in potential
PBSWGS	source gate sidewall junction build-in potential
TCJBD	temperature dependence of drain-side diode capacitance
TCJBDSW	temperature dependence of drain-side diode capacitance
TCJBDSWG	temperature dependence of drain-side diode capacitance
TCJBS	temperature dependence of source-side diode capacitance
TCJBSSW	temperature dependence of source-side diode capacitance
TCJBSSWG	temperature dependence of source-side diode capacitance
#**AD**	junction area of the drain contact
#**PD**	junction periphery of the drain contact
#**AS**	junction area of the source contact
#**PS**	junction periphery of the source contact

19 Break Down Models

19.1 Hard Break Down Model

This model accounts for junction avalanche breakdown at drain.

$$I_{\mathrm{hbreak}} = \mathbf{HBDF} \cdot \exp(\beta \cdot (V_{\mathrm{dse}} - HB_{\mathrm{dv}})) \tag{288}$$

COHBD=1: refers to the monotonous increasing breakdown voltage with increased Vgs

$$HB_{\mathrm{dv}} = HBDC_{\mathrm{eff}} \qquad (\text{if } V_{\mathrm{gs}} < \mathbf{HBDB}) \tag{289}$$

$$HB_{\mathrm{dv}} = HB_{\mathrm{dv,base}} \qquad (\text{if } V_{\mathrm{gs}} \geq \mathbf{HBDB}) \tag{290}$$

COHBD=-1: refers to the monotonous decresing breakdown voltage with increased Vgs

$$HB_{\mathrm{dv}} = HB_{\mathrm{dv,base}} \qquad (\text{if } V_{\mathrm{gs}} \leq \mathbf{HBDB}) \tag{291}$$

$$HB_{\mathrm{dv}} = HBDC_{\mathrm{eff}} \qquad (\text{if } V_{\mathrm{gs}} > \mathbf{HBDB}) \tag{292}$$

$$HB_{\mathrm{dv,base}} = \mathbf{HBDA} \cdot (V_{\mathrm{gs}} - \mathbf{HBDB})^2 + HBDC_{\mathrm{eff}} \tag{293}$$

where HB_{dv} means hard break down voltage and **HBDA**, **HBDB**, and **HBDC** are model parameters. When **COHBD**=0, hard break down current is not calculated.

Tempetature dependence is considered in $HBDC_{\mathrm{eff}}$ in the following way as

$$HBDC_{\mathrm{eff}} = \mathbf{HBDC} + \mathbf{HBDCTMP} \cdot (T - \mathbf{TNOM}) \tag{294}$$

19.2 Snapback

As impact ionization in the channel-drain region intensifies with increased Vds, large amount of carriers flow to the substrate contact. This causes the potential build-up within the substrate. At the source junction, the potential build-up works as foward biasing of the pn junction and carrier injection to the source starts. This is observed as the parasitic bipolar current. The same amount of carriers flow to the drain-substrate junction, which experience again multiplication phenomenon. These behaviors are captured in the current-driven mode rather than the voltage-driven mode of simulation and/or measurement.
To simulate snapback, set the following flags: **COSNP** = 1 (mandatory), **COISUB** = 1 (mandatory), **CORBNET** = 1 and set an appropriate value to **RBPB**. Otherwise, supply an external resistor to the bulk terminal so that the bulk potential can rise toward forward biasing of the source junction.
The parasitic bipolar current, I_{bjt}, which flows the substrate, is expressed as:

$$I_{\mathrm{bjt}} = \left(1 + X_{\mathrm{sub1SNP}} \cdot P_{\mathrm{sisubsatSNP}} \cdot \exp\left(-\frac{X_{\mathrm{sub2SNP}}}{P_{\mathrm{sisubsatSNP}}}\right)\right) \cdot I_{\mathrm{bs}} \tag{295}$$

where I_{bs} represents the source/bulk junction diode current (Section 18.1).

In the above expression, the same equations for impact ionization (Section 17.1) are used except for the new parameters (**SUB1SNP**,**SUB2SNP**, and **SVDSSNP**) distinct from **SUB1**,**SUB2**, and **SVDS**, respectively, as follows:

$$X_{\mathrm{sub1SNP}} = \mathbf{SUB1SNP} \cdot \left(1 + \frac{\mathbf{SUB1L}}{L_{\mathrm{gate}}^{\mathbf{SUB1LP}}}\right) \cdot X_{\mathrm{subTmp}} \tag{296}$$

$$X_{\mathrm{sub2SNP}} = \mathbf{SUB2SNP} \cdot \left(1 + \frac{\mathbf{SUB2L}}{L_{\mathrm{gate}}}\right) \cdot \frac{1}{X_{\mathrm{subTmp}}} \tag{297}$$

$$P_{\mathrm{sisubsatSNP}} = \mathbf{SVDSSNP} \cdot V_{\mathrm{ds}} + \phi_{\mathrm{S0}} - \frac{L_{\mathrm{gate}} \cdot P_{\mathrm{sislsat}}}{X_{\mathrm{gate}} + L_{\mathrm{gate}}} \tag{298}$$

Those new parameters can be used for fitting a folded part of I-V characteristics during the current-driven measurement.

The HiSIM model parameters introduced in section 18 are summarized in Table 19.

Table 19: HiSIM model parameters introduced in section 19 of this manual. # indicates instance parameters.

HBDA	coeff. for hard break down voltage
HBDB	coeff. for hard break down voltage
HBDC	coeff. for hard break down voltage
HBDF	coeff. for hard break down voltage
HBDCTMP	tempetature dependence of **HBDC**
SUB1SNP	impact ionization parameter for snapback
SUB2SNP	impact ionization parameter for snapback
SVDSSNP	impact ionization parameter for snapback

20 Noise Models

20.1 $1/f$ Noise Model

The $1/f$ noise is caused by both the carrier fluctuation and the mobility fluctuation. The final description for the drift-diffusion model is [44]

$$S_{I_{\rm ds}} = \frac{I_{\rm ds}^2 \mathbf{NFTRP}}{\beta f (L_{\rm eff} - \Delta L) W_{\rm eff} \cdot \mathbf{NF}} \left[\frac{1}{(N_0 + N^*)(N_L + N^*)} + \frac{2\mu E_y \mathbf{NFALP}}{N_L - N_0} \ln\left(\frac{N_L + N^*}{N_0 + N^*}\right) + (\mu E_y \mathbf{NFALP})^2 \right] \tag{299}$$

where the parameters **NFALP** and **NFTRP** represent the contribution of the mobility fluctuation and the ratio of trap density to attenuation coefficient, respectively. N_0 and N_L are carrier densities at source side and drain side or pinch-off point, respectively, as calculated in HiSIM. N^* is written as

$$N^* = \frac{C_{\rm ox} + C_{\rm dep} + \mathbf{CIT}}{q\beta} \tag{300}$$

where $C_{\rm dep}$ is the depletion capacitance calculated with $\phi_{\rm S}$. **CIT** is the capacitance caused by the interface-trapped carriers and is normally fixed to be zero.

$$N_{\rm flick} = S_{I_{\rm ds}} \cdot f^{\mathbf{FALPH}} \tag{301}$$

is calculated in HiSIM, where **FALPH** has been introduced to model the deviation from the exact $1/f$ characteristic.

20.2 Thermal Noise Model

Van der Ziel derived the equation for the spectral density of the thermal drain-noise current at temperature T by integrating the transconductance along the channel direction y based on the Nyquist theorem [45]

$$S_{\rm id} = \frac{4kT}{L_{\rm eff}^2} \int g_{\rm ds}(y) dy = 4kT g_{\rm ds0} \gamma \tag{302}$$

Here k, $I_{\rm ds}$, $g_{\rm ds}(y)$, $g_{\rm ds0}$, γ are Boltzmann's constant, drain current, position-dependent channel conductance, channel conductance at $V_{\rm ds} = 0$, and drain-noise coefficient, respectively. In HiSIM the integration is performed with the surface potential $\phi_{\rm s}$ instead of the channel position as [46, 47]

$$S_{\rm id} = \frac{4kT}{L_{\rm eff}^2 I_{\rm ds}} \int g_{\rm ds}^2(\phi_{\rm s}) d\phi_{\rm s} \tag{303}$$

$$g_{\rm ds}(\phi_{\rm s}) = \frac{W_{\rm eff} \cdot \mathbf{NF}}{L_{\rm eff}} \beta \frac{d(\mu(\phi_{\rm s}) f(\phi_{\rm s}))}{d\phi_{\rm s}} \tag{304}$$

Here $f(\phi_{\rm s})$ is a characteristic function of HiSIM related to the carrier concentration [48]. The final equations for $S_{\rm id}$ in our compact-modeling approach, obtained after solving the integral of Eq. (303), become functions of the self-consistent surface potentials as well as the surface-potential derivatives at source and drain.

$$S_{\rm id} = 4kT \frac{W_{\rm eff} \cdot \mathbf{NF} C_{\rm ox}\, VgVt\, \mu}{(L_{\rm eff} - \Delta L)} \frac{(1 + 3\eta + 6\eta^2)\mu_{\rm d}^2 + (3 + 4\eta + 3\eta^2)\mu_{\rm d}\mu_{\rm s} + (6 + 3\eta + \eta^2)\mu_{\rm s}}{15(1+\eta)\mu_{\rm av}^2} \tag{305}$$

where $\mu_{\rm s}$, $\mu_{\rm d}$ and $\mu_{\rm av}$ are mobilities at the source side, the drain side, and averaged, respectively.

$$\eta = 1 - \frac{(\phi_{\rm SL} - \phi_{\rm S0}) + \chi(\phi_{\rm SL} - \phi_{\rm S0})}{V_{\rm g}V_{\rm t}} \tag{306}$$

$$\chi = 2\frac{cnst0}{C_{\rm ox}}\left[\left[\frac{2}{3}\frac{1}{\beta}\frac{\{\beta(\phi_{\rm SL} - V_{\rm bs}) - 1\}^{\frac{3}{2}} - \{\beta(\phi_{\rm S0} - V_{\rm bs}) - 1\}^{\frac{3}{2}}}{\phi_{\rm SL} - \phi_{\rm S0}}\right] - \sqrt{\beta(\phi_{\rm S0} - V_{\rm bs}) - 1}\right] \tag{307}$$

$VgVt$ is equal to the carrier density at the source side divided by the oxide capacitance.
Thus no additional model parameters are required for the thermal noise model.

$$N_{\rm thrml} = S_{\rm id}/4kT \tag{308}$$

is calculated in HiSIM.

20.3 Induced Gate Noise Model

No additional model parameters are required for the induced gate noise model.

$$N_{\rm igate} = S_{\rm igate}/f^2 \tag{309}$$

is calculated in HiSIM. Explicit model equation were presented at SISPAD in 2006 [49].

20.4 Coupling Noise Model

No additional model parameters are required for the coupling noise model.

$$N_{\rm cross} = \frac{S_{\rm igid}}{\sqrt{S_{\rm igate} \cdot S_{\rm id}}} \tag{310}$$

is calculated in HiSIM. Explicit model equation were presented at SISPAD in 2006 [49].

The HiSIM model parameters introduced in section 20 are summarized in Table 20.

Table 20: HiSIM model parameters introduced in section 20 of this manual. $*$ indicates a minor parameter.

NFTRP	ratio of trap density to attenuation coefficient
NFALP	contribution of the mobility fluctuation
$*$**CIT**	capacitance caused by the interface trapped carriers
FALPH	power of f describing deviation of $1/f$

21 Non-Quasi-Static (NQS) Model

21.1 Carrier Formation

To consider the carrier transit delay in HiSIM, the carrier formation is modeled as [50, 51, 52]

$$q(t_\mathrm{i}) = \frac{q(t_{\mathrm{i}-1}) + \frac{\Delta t}{\tau} Q(t_\mathrm{i})}{1 + \frac{\Delta t}{\tau}} \tag{311}$$

where $q(t_\mathrm{i})$ and $Q(t_\mathrm{i})$ represent the non-quasi-static and the quasi-static carrier density at time t_i, respectively, and $\Delta t = t_\mathrm{i} - t_{\mathrm{i}-1}$ is valid. The delay is determined by the carrier transit delay τ and the time interval in the circuit simulation Δt.

21.2 Delay Mechanisms

Up to weak inversion:

$$\tau_\mathrm{diff} = \mathbf{DLY1} \tag{312}$$

At strong inversion:

$$\tau_\mathrm{cond} = \mathbf{DLY2} \cdot \frac{Q_\mathrm{i}}{I_\mathrm{ds}} \tag{313}$$

$$\frac{1}{\tau} = \frac{1}{\tau_\mathrm{diff}} + \frac{1}{\tau_\mathrm{cond}} \tag{314}$$

For the formation of bulk carriers:

$$\tau_\mathrm{B} = \mathbf{DLY3} \cdot C_\mathrm{ox} \tag{315}$$

where **DLY3** is a constant coefficient and C_ox is the oxide capacitance. From the HiSIM_HV 1.1.0 version this NQS model is implemented in the newwork form as shown in Fig. 24.

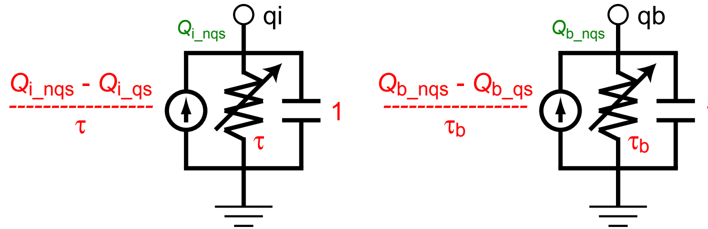

Fig. 24: NQS model implementation into circuit simulator.

21.3 Time-Domain Analysis

The total drain/source/bulk terminal currents are derived from the superposition of the transport current and the charging current. The transport current is a function of the instantaneous terminal voltages and is approximated by the steady-state solution. The source/drain/bulk charging currents are the time derivatives of the associated non-quasi-static charges, q_S, q_D, and q_B, respectively.

For LDMOS/HVMOS, carrier transit delay effect in the drift region is included as the RC delay. The resistance R and the capacitance C contributing the delay are taken calculated in HiSIM_HV. If the resistance in the drift region is large, the delay becomes automatically large.
The formation delay of the overlap charge Q_{over} is also modeled as

$$\tau_{\mathrm{LD}} = \mathbf{DLYOV} \cdot C_{\mathrm{ox0}} \cdot \phi_{\mathrm{s,LD}} \tag{316}$$

where $\phi_{\mathrm{s,LD}}$ represents the surface potential in the overlap region.

21.4 AC Analysis

The load file is rewritten from the HiSIM_HV 1.1.0 version so that the internal node is seen explicitly. Thus, the calculation procesure becomes different from the older versions, however, the formulae used for the calculation are the same.

The HiSIM model parameters introduced in section 21 are summarized in Table 21.

Table 21: HiSIM model parameters introduced in section 21 of this manual.

DLY1	coefficient for delay due to diffusion of carriers
DLY2	coefficient for delay due to conduction of carriers
DLY3	coefficient for RC delay of bulk carriers
DLYOV	coefficient for RC delay of overlap charge (**CONQSOV**=1)

22 Self-Heating Effect Model

The self-heating effect is modeled with the thermal network shown in Fig. 25. The flag **COSELFHEAT** must be equal to one and **RTH0** must not be equal to zero to activate the model. The temperature node must not be zero, if the self-heating effect is switched on. The self-heating effect should be switched on/off only with the model flag **COSELFHEAT**. To avoid unrealistic temperature increase during circuit simulation, clipping has been introduced. The clipping method can be also selected by the model flag **COSELFHEAT**:

=0 : no self-heating effect (default)

=1 : power clipping

=2 : temperature clipping

COSELFHEAT=2 is newly added from the present version. **COSELFHEAT**=2 is recommended.

The temperature node is automatically generated in circuit simulator for each device as other bias nodes. Fisrt, the model core (HiSIMhv.eval) is called to evaluate device characteristics without heating. Then, the temperature is updated considering the self-heating effect by creating the temperature node. The model core is called again to update the device characteristics with the calculated temperature T. Under the DC condition the temperature increase is calculated analytically as

$$T = T + R_{\mathrm{th}} \cdot I_{\mathrm{ds}} \cdot V_{\mathrm{ds}} \tag{317}$$

where R_{th} as well as C_{th} are a function of W_{eff} as

$$R_{\mathrm{th}} = \frac{R_{\mathrm{th0}}}{W_{\mathrm{eff}}} \cdot \left(\frac{1}{\mathbf{NF}^{\mathbf{RTH0NF}}}\right)\left(1 + \frac{\mathbf{RTH0L}}{(L_{\mathrm{gate}}/10^{-6})^{\mathbf{RTH0LP}}}\right)\left(1 + \frac{\mathbf{RTH0W}}{(W_{\mathrm{gate}}/10^{-6})^{\mathbf{RTH0WP}}}\right) \tag{318}$$

$$R_{\mathrm{th0}} = \mathbf{RTH0} + \mathbf{RTHTEMP1} \cdot (T0 - \mathbf{TNOM}) + \mathbf{RTHTEMP2} \cdot (T0^2 - \mathbf{TNOM}^2) \tag{319}$$

$$C_{\mathrm{th}} = \mathbf{CTH0} \cdot W_{\mathrm{eff}} \tag{320}$$

where $\left(L_{\mathrm{gate}}/10^{-6}\right)$ and $\left(W_{\mathrm{gate}}/10^{-6}\right)$ or equivalently, $\left(L_{\mathrm{gate}} \cdot 10^{6}\right)$ and $\left(W_{\mathrm{gate}} \cdot 10^{6}\right)$ intend normalization to a unitless quantity, the magnitude of which stays around the unity (=1).

The model parameter **RTH0** is fitted to measured DC data, and the model parameter **CTH0** is introduced for AC fitting.

The thermal dissipation is modeled as [55]

$$T = T + R_{\mathrm{th}} \cdot I_{\mathrm{ds}} \cdot V'_{\mathrm{ds}} \tag{321}$$

$$V'_{\mathrm{ds}} = V_{\mathrm{dsi}} + POW_{\mathrm{ratio}}(V_{\mathrm{ds}} - V_{\mathrm{dsi}}) \tag{322}$$

$$POW_{\mathrm{ratio}} = \mathbf{POWRAT} + \mathbf{PRATTEMP1} \cdot (T0 - \mathbf{TNOM}) + \mathbf{PRATTEMP2} \cdot (T0^2 - \mathbf{TNOM}^2) \tag{323}$$

where **POWRAT** is a model parameter. The external node potential is represented by V_{ds} and the internal node potential within the drift region at the channel/drift junction is by V_{dsi}, which is calculated during the SPICE simulation.

A limiter for the temperature increase due to the self-heating effect **SHEMAX** is introduced to avoid drastic artifical temperature increase during circuit simulations.

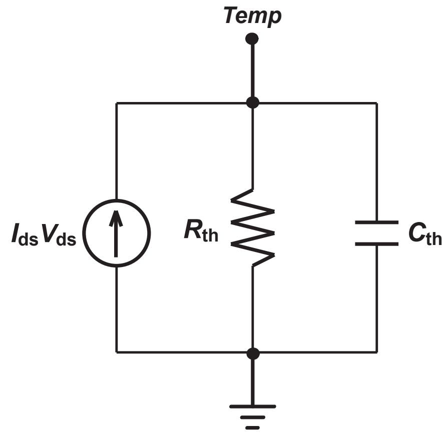

Fig. 25: Thermal Network applied for the self-heating effect.

Table 22: HiSIM model parameters introduced in section 22 of this manual.

RTH0	thermal resistance
RTHTEMP1	temperature dependence of thermal resistance
RTHTEMP2	temperature dependence of thermal resistance
CTH0	thermal capacitance
RTH0L	length dependence of thermal resistance
RTH0LP	length dependence of thermal resistance
RTH0W	width dependence of thermal resistance
RTH0WP	width dependence of thermal resistance
RTH0NF	number of finger dependence of thermal resistance
POWRAT	thermal dissipation
PRATTEMP1	tenperture dependence of thermal dissipation
PRATTEMP2	tenperture dependence of thermal dissipation
SHEMAX	maximum temperature increase

The HiSIM model parameters introduced in section 22 are summarized in Table 22.

23 Multiplication Factor

For the case of a multiple device construction the multiple factor **M** is introduced as an instance parameter. All device features such as currents and capacitances are multipled by **M**. Noises are also multiplied by **M**.

The HiSIM model parameters introduced in section 23 are summarized in Table 23.

Table 23: HiSIM model parameters introduced in section 23 of this manual. # indicates an instance parameter.

# **M**	multiplication factor

24 DFM Model

To support design for manufacturability (DFM) HiSIM introduces an option for considering the variation of device parameters.
Accurate prediction of device performance for a wide range of the substrate-impurity-concentration variations is secured by introducing an impurity concentration dependent mobility due to the phonon scattering as

$$M_{\rm uephonon} = \mathbf{MUEPH1}\,[\mathbf{MPHDFM}\{\ln(\mathbf{NSUBCDFM}) - \ln(N_{\rm subc})\} + 1]$$

$$\mathbf{NSUBP} = \mathbf{NSUBP} + (N_{\rm SUBCDFM} - N_{\rm subc}) \tag{324}$$

$$\mathbf{NEXT} = \mathbf{NEXT} + (\mathbf{NSUBCDFM} - N_{\rm subc}) \tag{325}$$

where **NSUBCDFM** is an instance parameter and **MPHDFM** is a model parameter describing the mobility reduction due to the increase of the substrate impurity concentration. This model is activated if the model flag **CODFM** = 1, and NSUBCDFM is also given.

The HiSIM model parameters introduced in section 24 are summarized in Table 24.

Table 24: HiSIM model parameters introduced in section 24 of this manual. # indicates an instance parameter.

Parameter	Description
#NSUBCDFM	substrate impurity concentration
MPHDFM	mobility dependence of $N_{\rm subc}$ due to $\mu_{\rm phonon}$

25 Depletion Mode Model Option

To support depletion mode MOSFET devices, an option for considering the structural feature is introduced in HiSIM. Modeling is done for the p-Si substrate, however, it is applicable for the n-Si substrate as well. This is done automatically by determing the device "type" in netlist.
In the depletion mode MOSFET, an n layer is constructed at the channel surface of conventional MOSFET devices as shown Fig. 26 where $N_{\rm dep}$ denotes the carrier concentration of the n layer, and $T_{\rm dep}$ denotes the thickness of the n layer.

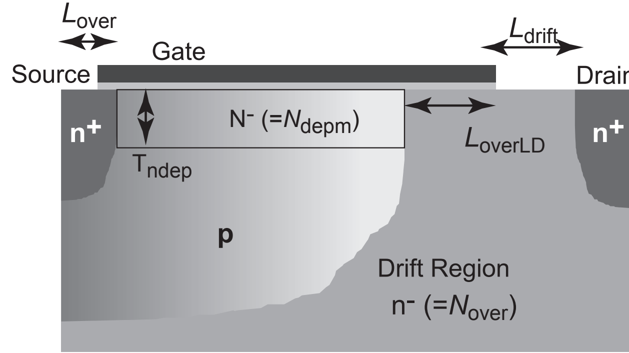

Fig. 26: Schematic of the typical depletion mode MOSFET structure and device parameters.

Fig. 27 depicts the potential and the electron carrier density distribution along the depth direction of a depletion mode device. The Poisson equation including all charges induced within the device is solved for calculating the accurate distributions under any bias conditions. $N_{\rm depm}$ takes the impurity concentration as

$$N_{\rm depm} = \mathbf{NDEPM} \cdot \left(1 + \frac{\mathbf{NDEPML}}{(L_{\rm gate} \cdot 10^{6})^{\mathbf{NDEPMLP}}}\right) \tag{326}$$

This model is activated if the model flag **CODEP** = 1 (old depletion model), 2 (old depletion model) and **CODEP** = 3 (new depletion mode). (default = 0 : no depletion mode)
Three model options are explained in the following. To use **CODEP**=3 is suggested for better derivative characteristics.

i) CODEP=1 :old model developed for Version 2.2.0

25.1 CODEP=1 : old model developed for Version 2.2.0

In the depletion mode MOSFET model, the quasi-Fermi potential($V_{\rm ds,eff}$) for the majority carrier is written in the same way as that of the minority carrier.

$$V_{\rm ds,eff} = \frac{V_{\rm ds}}{\left[1 + \left(\frac{V_{\rm ds}}{V_{\rm ds,sat}}\right)^{\Delta}\right]^{\frac{1}{\Delta}}} \tag{327}$$

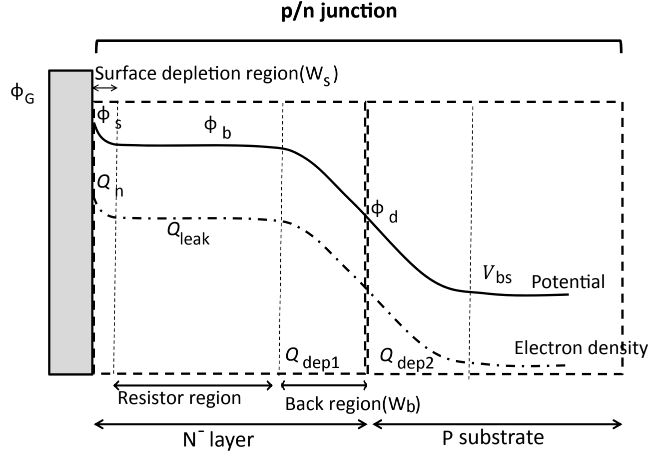

Fig. 27: Potential and electron carrier density distribution along the channel cross section of the depletion mode MOSFET.

where

CODDLT=0 :

$$\Delta = \frac{\mathbf{DDLTMAX} \cdot T1}{\mathbf{DDLTMAX} + T1} + 1 \tag{328}$$

$$T1 = \mathbf{DDLTSLP} \cdot L_{\text{gate}} \cdot 10^6 + \mathbf{DDLTICT} \tag{329}$$

CODDLT=1 (defualt) :

$$\Delta = \frac{\mathbf{DDLTMAX} \cdot T1}{\mathbf{DDLTMAX} + T1} + \mathbf{DDLTICT} \tag{330}$$

$$T1 = \mathbf{DDLTSLP} \cdot L_{\text{gate}} \cdot 10^6 \tag{331}$$

The saturation voltage is defined as

$$V_{\text{ds,sat}} = V'_{\text{G}} + \frac{qN_{\text{depm}}\epsilon_{\text{Si}}}{{C_{\text{ox}}}^2}\left\{1 - \sqrt{1 + 2\frac{{C_{\text{ox}}}^2}{qN_{\text{depm}}\epsilon_{\text{Si}}}\left(V'_{\text{G}} + 2 - \frac{1}{\beta} - V_{\text{bs}}\right)}\right\} \tag{332}$$

The total drain current I_{ds} is the sum of the accumulation current I_{dd} and that flowing in the resistor region I_{res} and that flowing in the back region I_{back} written as

$$I_{\text{ds}} = \frac{W_{\text{eff,nf}}}{L_{\text{ch}}} \cdot \frac{1}{\beta}\left(\mu \cdot I_{\text{dd}}\right) + I_{\text{ds,res}} + I_{\text{ds,back}} \tag{333}$$

where,

$$I_{\text{dd}} = -\beta\frac{(Q_{\text{n0}} + Q_{\text{nl}})}{2} \cdot (\phi_{\text{SL}} - \phi_{\text{S0}}) - Q_{\text{n0}} + Q_{\text{nl}} \tag{334}$$

$Q_{\rm n0}$ and $Q_{\rm nl}$ denote the accumulation charge in the n layor at the source side and the drain side, respectively. The threshold voltage shift $\Delta V_{\rm th}$ due to the short-channel effect (see Sec. 7) is modified by adding $V_{\rm ds}$ into the depletion width equation (see Eq. (32)) as

$$W_{\rm d} = \sqrt{2\epsilon_{\rm Si} \cdot (2\Phi_{\rm B} - V_{\rm bs} - \mathbf{DEPETA} \cdot V_{\rm ds})} \tag{335}$$

In the same way as for the inversion carrier, the carrier mobility model for $I_{\rm dd}$ is written as

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_{\rm y}}{V_{\rm max}}\right)^{\mathbf{BB}}\right)^{\frac{1}{\mathbf{BB}}}} \tag{336}$$

where

$$\frac{1}{\mu_0} = \frac{1}{\mu_{\rm CB}} + \frac{1}{\mu_{\rm PH}} + \frac{1}{\mu_{\rm SR}} \tag{337}$$

$$\mu_{\rm SR} = \frac{\mathbf{MUESR1}}{E_{\rm eff}{}^{M_{\rm uesurface]}}} \tag{338}$$

$$\mu_{\rm PH} = \frac{M_{\rm uephonon}}{E_{\rm eff}{}^{\mathbf{MUEPH0}}} \tag{339}$$

$$\mu_{\rm CB} = \mathbf{MUECB0} + \mathbf{MUECB1} \cdot \frac{-Q_{\rm n0}}{q \cdot 10^{11}} \tag{340}$$

$$E_{\rm eff} = \frac{\left(\frac{\mathbf{NINV}}{\epsilon_{\rm Si}}\right) \cdot (-Q_{\rm n0})}{1 + (\phi_{\rm SL} - \phi_{\rm S0}) \cdot N_{\rm invde}} \tag{341}$$

The resistor current and the back current are written as

$$I_{\rm ds,res} = W_{\rm eff,nf} \cdot Q_{\rm leak,resistor0} \cdot \mu_{\rm leak,res} \cdot \frac{V_{\rm ds,eff}}{L_{\rm ch}} \tag{342}$$

$$I_{\rm ds,back} = W_{\rm eff,nf} \cdot Q_{\rm leak,back0} \cdot \mu_{\rm leak,back} \cdot \frac{V_{\rm ds,eff}}{L_{\rm ch}} \tag{343}$$

$Q_{\rm leak,resistor0}$ denotes the charge in the resistor part at the source side. Furthermore, $Q_{\rm leak,back0}$ denotes the charge in the back part at the source side.

$$Q_{\rm leak,resistor0} = -q \cdot N_{\rm depm} \cdot (\mathbf{TNDEP} - W_{\rm s} - W_{\rm b}) \tag{344}$$

$$Q_{\rm leak,back0} = -q \cdot N_{\rm depm} \cdot \exp\{\beta\,(\phi_{\rm b0} - V_{\rm ds,eff})\} \cdot W_{\rm b} \tag{345}$$

$$W_{\rm b} = \sqrt{\frac{2\epsilon_{\rm Si}\epsilon_0 N_{\rm subc}}{qN_{\rm depm}\,(N_{\rm depm} + N_{\rm subc})} \cdot (\phi_{\rm bi} - V_{\rm bs})} \tag{346}$$

$$W_{\rm s} = \sqrt{\frac{2\epsilon_{\rm Si}\epsilon_0}{q \cdot N_{\rm depm}}\,(-\phi_{\rm s})} \tag{347}$$

$\phi_{\rm bi}$ denotes the built-in potential of P-N junction and is defined as follows

$$\phi_{\rm bi} = \frac{1}{\beta} \ln\left(\frac{N_{\rm subc} \cdot N_{\rm depm}}{n_{\rm i}{}^2}\right) \tag{348}$$

and $V_{\rm ds,res}$ denotes the effective potential at the drain side in the resistor part and is defined as follows

$$V_{\rm ds,res} = \frac{V_{\rm ds}}{\left[1+\left(\frac{V_{\rm ds}}{V_{\rm ds,sat}}\right)^{\Delta}\right]^{\frac{1}{\Delta}}} \tag{349}$$

where Δ is the same as that for the accumulation, and

$$V_{\rm ds,sat} = DEP_{\rm vdsef2} \cdot \left[V'_{\rm G} + DEP_{\rm vdsef1} + \frac{qN_{\rm depm}\epsilon_{\rm Si}}{{C_{\rm ox}}^2} \left\{1 - \sqrt{1 + 2\frac{{C_{\rm ox}}^2}{qN_{\rm depm}\epsilon_{\rm Si}}\left(V'_{\rm G} + DEP_{\rm vdsef1} - \frac{1}{\beta} - V_{\rm bs}\right)}\right\}\right] \tag{350}$$

where

$$DEP_{\rm vdsef1} = \textbf{DEPVDSEF1} \tag{351}$$

$$DEP_{\rm vdsef2} = \textbf{DEPVDSEF2} \tag{352}$$

The high field carrier mobility in the n layer is written as

$$\mu_{\rm leak,res} = \frac{\mu_{\rm 0leak,res}}{\left(1+\left(\frac{\mu_{\rm 0leak,res}E_{\rm y}}{DEP_{\rm vmax}}\right)^{\textbf{DEPBB}}\right)^{\frac{1}{\textbf{DEPBB}}}} \tag{353}$$

where

$$E_{\rm y} = \frac{V_{\rm ds,res}}{L_{\rm ch}} \tag{354}$$

$$\frac{1}{\mu_{\rm 0leak,res}} = \frac{1}{\mu_{\rm CB}} + \frac{1}{\mu_{\rm PH}} \tag{355}$$

$$\mu_{\rm PH} = \frac{DEP_{\rm muephonon}}{E_{\rm eff}{}^{\textbf{DEPMUEPH0}}} \tag{356}$$

$$\mu_{\rm CB} = DEP_{\rm mue0} + DEP_{\rm mue1} \cdot \frac{-Q_{\rm leak,resistor0}}{q \cdot 10^{11}} \tag{357}$$

$$E_{\rm eff} = \frac{-Q_{\rm leak,resistor0}}{\varepsilon_{\rm Si}} \cdot \frac{1}{1+(\phi_{\rm SL}-\phi_{\rm S0})\cdot N_{\rm invde}} \tag{358}$$

$$\tag{359}$$

$$\mu_{\rm leak,back} = \frac{\mu_{\rm 0leak,back}}{\left(1+\left(\frac{\mu_{\rm 0leak,back}E_{\rm y}}{DEP_{\rm vmax}}\right)^{\textbf{DEPBB}}\right)^{\frac{1}{\textbf{DEPBB}}}} \tag{360}$$

$$E_{\mathrm{y}} = \frac{V_{\mathrm{ds,res}}}{L_{\mathrm{ch}}} \tag{361}$$

$$\frac{1}{\mu_{\mathrm{0leak,back}}} = \frac{1}{\mu_{\mathrm{CB}}} + \frac{1}{\mu_{\mathrm{PH}}} \tag{362}$$

$$\mu_{\mathrm{PH}} = \frac{DEP_{\mathrm{muephonon}}}{E_{\mathrm{eff}}{}^{\mathbf{DEPMUEPH0}}} \tag{363}$$

$$\mu_{\mathrm{CB}} = DEP_{\mathrm{mueback}} + DEP_{\mathrm{mueback1}} \cdot \frac{-Q_{\mathrm{leak,back0}}}{q \cdot 10^{11}} \tag{364}$$

$$E_{\mathrm{eff}} = \frac{-Q_{\mathrm{leak,back0}}}{\varepsilon_{\mathrm{Si}}} \cdot \frac{1}{1 + (\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}) \cdot N_{\mathrm{invde}}} \tag{365}$$

DEP_{mue0}, DEP_{mue1}, DEP_{mueback}, DEP_{mueback1}, N_{invde} and DEP_{vmax} are

$$DEP_{\mathrm{mue0}} = \mathbf{DEPMUE0} \tag{366}$$

$$DEP_{\mathrm{mue1}} = \mathbf{DEPMUE1} \tag{367}$$

$$DEP_{\mathrm{mueback}} = \mathbf{DEPMUEBACK0} \tag{368}$$

$$DEP_{\mathrm{mueback1}} = \mathbf{DEPMUEBACK1} \tag{369}$$

$$DEP_{\mathrm{vmax}} = \mathbf{DEPVMAX} \cdot \left(1 + \frac{\mathbf{DEPVMAXL}}{(L_{\mathrm{gate}} \cdot 10^6)^{\mathbf{DEPVMAXLP}}}\right) \tag{370}$$

$$N_{\mathrm{invde}} = \mathbf{NINVD} \cdot \left(1 + \frac{\mathbf{NINVDW}}{(W_{\mathrm{gate}} \cdot 10^6)^{\mathbf{NINVDWP}}}\right) \tag{371}$$

25.2 CODEP=2 : old model

In the depletion mode MOSFET model, the quasi-Fermi potential($V_{\mathrm{ds,eff}}$) for the majority carrier is written in the same way as that of the minority carrier.

$$V_{\mathrm{ds,eff}} = \frac{V_{\mathrm{ds}}}{\left[1 + \left(\frac{V_{\mathrm{ds}}}{V_{\mathrm{ds,sat}}}\right)^{\Delta}\right]^{\frac{1}{\Delta}}} \tag{372}$$

where

CODDLT=0 :

$$\Delta = \frac{\mathbf{DDLTMAX} \cdot T1}{\mathbf{DDLTMAX} + T1} + 1 \tag{373}$$

$$T1 = \mathbf{DDLTSLP} \cdot L_{\mathrm{gate}} \cdot 10^6 + \mathbf{DDLTICT} \tag{374}$$

CODDLT=1 (defualt) :

$$\Delta = \frac{\mathbf{DDLTMAX} \cdot T1}{\mathbf{DDLTMAX} + T1} + \mathbf{DDLTICT} \tag{375}$$

$$T1 = \mathbf{DDLTSLP} \cdot L_{\mathrm{gate}} \cdot 10^6 \tag{376}$$

$$V_{\mathrm{ds,sat}} = \left[V'_{\mathrm{G}} + \frac{qN_{\mathrm{depm}}\epsilon_{\mathrm{Si}}}{{C_{\mathrm{ox}}}^2} \{1 - \sqrt{1 + 2\frac{{C_{\mathrm{ox}}}^2}{qN_{\mathrm{depm}}\epsilon_{\mathrm{Si}}}\{V'_{\mathrm{G}}\}}\} \right] \tag{377}$$

The total drain current I_{ds} is written as follows

$$I_{\mathrm{ds}} = \frac{W_{\mathrm{eff,nf}}}{L_{\mathrm{ch}}} \cdot \frac{1}{\beta} (\mu \cdot I_{\mathrm{dd}}) + I_{\mathrm{ds,res}} \tag{378}$$

where the accumulation current flowing at the surface is written as

$$I_{\mathrm{dd}} = -\beta \frac{(Q_{\mathrm{n0}} + Q_{\mathrm{nl}})}{2} \cdot (\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}) \tag{379}$$

Q_{n0} and Q_{nl} denote the accumlation charge in the n layor at the source side and the drain side, respectively. The threshold voltage shift ΔV_{th} due to the short-channel effect is modified by eliminating V_{bs} from the depletion width equation (see Eq. (32)) as

$$W_{\mathrm{d}} = \sqrt{\frac{2\epsilon_{\mathrm{Si}}\,(2\Phi_{\mathrm{B}})}{qN_{\mathrm{dep}}}} \tag{380}$$

In the same way as for the inversion carrier the carrier mobility model for the accumulation current is written as

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_{\mathrm{y}}}{V_{\mathrm{max}}}\right)^{\mathbf{BB}}\right)^{\frac{1}{\mathbf{BB}}}} \tag{381}$$

$$\frac{1}{\mu_0} = \frac{1}{\mu_{\mathrm{CB}}} + \frac{1}{\mu_{\mathrm{PH}}} + \frac{1}{\mu_{\mathrm{SR}}} \tag{382}$$

$$\mu_{\mathrm{SR}} = \frac{\mathbf{MUESR1}}{{E_{\mathrm{eff}}}^{M_{\mathrm{uesurface}}}} \tag{383}$$

$$\mu_{\mathrm{PH}} = \frac{M_{\mathrm{uephonon}}}{{E_{\mathrm{eff}}}^{\mathbf{MUEPH0}}} \tag{384}$$

$$\mu_{\mathrm{CB}} = \mathbf{MUECB0} + \mathbf{MUECB1} \cdot \frac{-Q_{\mathrm{n0}}}{q \cdot 10^{11}} \tag{385}$$

$$E_{\mathrm{eff}} = \frac{\left(\frac{\mathbf{NINV}}{\epsilon_{\mathrm{Si}}}\right) \cdot (-Q_{\mathrm{n0}})}{1 + (\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}) \cdot N_{\mathrm{invde}}} \tag{386}$$

The resistor current is written as

$$I_{\mathrm{ds,res}} = q \cdot N_{\mathrm{depm}} \cdot \mu_{\mathrm{leak,res}} \cdot \frac{W_{\mathrm{res}} \cdot W_{\mathrm{eff}}}{L_{\mathrm{eff}}} V_{\mathrm{ds,res}} \tag{387}$$

$$W_{\mathrm{res}} = \mathbf{TNDEP} \cdot (1 - \mathbf{TNDEPV} \cdot V_{\mathrm{ds}}) - W_{\mathrm{s}} - W_{\mathrm{b}} \tag{388}$$

$$W_{\mathrm{b}} = \sqrt{\frac{2\epsilon_{\mathrm{Si}}\epsilon_0 N_{\mathrm{subc}}}{qN_{\mathrm{depm}}\left(N_{\mathrm{depm}} + N_{\mathrm{subc}}\right)} \cdot (\phi_{\mathrm{bi}} - V_{\mathrm{bs}})} \tag{389}$$

$$W_{\mathrm{s}} = \sqrt{\frac{2\epsilon_{\mathrm{Si}}\epsilon_0}{q \cdot N_{\mathrm{depm}}}\left(-\phi_{\mathrm{res}}\right)} \tag{390}$$

where ϕ_{res} is the surface potential calculated separately from the accumulation current, and N_{depm} is the impurity concentration of the n layer. N_{subc} is defined in Eq. in (79), and ϕ_{bi} denotes the built-in potential of P-N junction and is defined as follows.

$$\phi_{\mathrm{bi}} = \frac{1}{\beta} \ln\left(\frac{N_{\mathrm{subc}} \cdot N_{\mathrm{depm}}}{{n_{\mathrm{i}}}^2}\right) \tag{391}$$

The effective potential at the drain side in the resistor part $V_{\mathrm{ds,res}}$ is defined as follows.

$$V_{\mathrm{ds,res}} = \frac{V_{\mathrm{ds}}}{\left[1 + \left(\frac{V_{\mathrm{ds}}}{V_{\mathrm{ds,sat}}}\right)^{\mathbf{DEPDDLT}}\right]^{\frac{1}{\mathbf{DEPDDLT}}}} \tag{392}$$

where

$$V_{\mathrm{ds,sat}} = V'_{\mathrm{G}} + \frac{qN_{\mathrm{depm}}\epsilon_{\mathrm{Si}}}{{C_{\mathrm{ox}}}^2}\left\{1 - \sqrt{1 + 2\frac{{C_{\mathrm{ox}}}^2}{qN_{\mathrm{depm}}\epsilon_{\mathrm{Si}}}\left\{V'_{\mathrm{G}} - \mathbf{DEPVSATR} \cdot \left(V_{\mathrm{bs}} + \frac{1}{\beta}\right)\right\}}\right\} \tag{393}$$

$$\mu_{\mathrm{leak,res}} = \frac{\mu_{0\mathrm{leak,res}}}{\left(1 + \left(\frac{\mu_{0\mathrm{leak,res}} E_{\mathrm{y}}}{DEP_{\mathrm{vmax}}}\right)^{\mathbf{DEPBB}}\right)^{\frac{1}{\mathbf{DEPBB}}}} \tag{394}$$

$$E_{\mathrm{y}} = \frac{V_{\mathrm{ds,res}}}{L_{\mathrm{ch}}} \tag{395}$$

$$\frac{1}{\mu_{0\mathrm{leak,res}}} = \frac{1}{\mu_{\mathrm{CB}}} + \frac{1}{\mu_{\mathrm{RES}}} \tag{396}$$

$$\mu_{\mathrm{CB}} = DEP_{\mathrm{mue0}} \tag{397}$$

$$\mu_{\mathrm{RES}} = \frac{DEP_{\mathrm{mue2}}}{E_{\mathrm{eff}}^{\mathbf{DEPMUEA1}}} \tag{398}$$

$$E_{\mathrm{eff}} = \frac{V_{\mathrm{gs}} - V_{\mathrm{bs}}}{T_{\mathrm{dep}}} \tag{399}$$

$$DEP_{\mathrm{vmax}} = \frac{\mathbf{DEPVMAX}}{1.8 + 0.4(T/\mathbf{TNOM}) + 0.1(T/\mathbf{TNOM})^2 - \mathbf{DEPVTMP} \cdot (1 - T/\mathbf{TNOM})} \tag{400}$$

$$DEP_{\mathrm{mue0}} = \frac{\mathbf{DEPMUE0}}{\left(\frac{T}{T_{\mathrm{nom}}}\right)^{\mathbf{DEPMUE0TMP}}} \tag{401}$$

$$DEP_{\mathrm{mue2}} = \frac{\mathbf{DEPMUE2}}{\left(\frac{T}{T_{\mathrm{nom}}}\right)^{\mathbf{DEPMUE2TMP}}} \tag{402}$$

DEPVFBC is the flat-band voltage of the resistor part for calculating ϕ_{res}.
DEPSUBSL is a fitting parameter for adjusting sub-threshold sloop for the resistor corrent.
The fitting parameter **DEPVGPSL** is introduced to achieve smooth transition from the depletion to the accumlation condition. If a minimum occurs for g_{m} at the transition point, adjust **DEPVGPSL** from zero.

25.3 CODEP=3 : new model

The drain current I_{ds} consists of the accumulation-mode current $I_{\mathrm{ds,acc}}$ which flows near the surface, and the resistor current $I_{\mathrm{ds,res}}$ which flows beneath the surface as

$$I_{\mathrm{ds}} = I_{\mathrm{ds,acc}} + I_{\mathrm{ds,res}} \tag{403}$$

The resistor current $I_{\mathrm{ds,res}}$ is subdivided into I_{res} and $I_{\mathrm{res,leak}}$.

$$I_{\mathrm{ds,res}} = I_{\mathrm{res}} + I_{\mathrm{res,leak}} \tag{404}$$

where I_{res} represents the current flowing the neutral part of the resistor region, and I_{leak} represents the leakage current flowing the resistor region in thanks to carrier injection at the source side even when the neutral part of the resistor region vanishes due to depletion at a biased condition.

25.3.1 Accumulation-mode current $I_{\mathrm{ds,acc}}$

In the depletion mode MOSFET model, the quasi-Fermi potential($V_{\mathrm{ds,eff}}$) for the majority carrier is written in the same way as that of the minority carrier.

$$V_{\mathrm{ds,eff}} = \frac{V_{\mathrm{ds}}}{\left[1 + \left(\frac{V_{\mathrm{ds}}}{V_{\mathrm{ds,sat}}}\right)^{\Delta}\right]^{\frac{1}{\Delta}}} \tag{405}$$

where

CODDLT=0 :

$$\Delta = \frac{\mathbf{DDLTMAX} \cdot T1}{\mathbf{DDLTMAX} + T1} + 1 \tag{406}$$

$$T1 = \mathbf{DDLTSLP} \cdot \left(L_{\mathrm{gate}}/10^{-6}\right) + \mathbf{DDLTICT} \tag{407}$$

CODDLT=1 (defualt) :

$$\Delta = \frac{\mathbf{DDLTMAX} \cdot T1}{\mathbf{DDLTMAX} + T1} + \mathbf{DDLTICT} \tag{408}$$

$$T1 = \mathbf{DDLTSLP} \cdot \left(L_{\mathrm{gate}}/10^{-6}\right) \tag{409}$$

The effective saturation voltage $V_{\rm ds,sat}$ is determined iteratively through a solution of the following set of equations:

$$C_{\rm ox} \cdot (V'_{\rm G} - \phi_{\rm vsat} + \mathbf{DEPVSATA}) + Q_{\rm sat} = 0 \tag{410}$$

$$Q_{\rm sat} = -\sqrt{\frac{2q\mathbf{NDEPM}\varepsilon_{\rm si}}{\beta}}\sqrt{\exp(-\beta\phi_{\rm vsat}) + \beta\phi_{\rm vsat} - 1} \tag{411}$$

$$V_{\rm ds,sat} = -\phi_{\rm vsat} \tag{412}$$

The total drain current $I_{\rm ds}$ is written as follows

$$I_{\rm ds} = \frac{W_{\rm eff}}{L_{\rm eff}} \cdot \mathbf{NF} \cdot \frac{1}{\beta}(\mu \cdot I_{\rm dd}) + I_{\rm ds,res} \tag{413}$$

where $L_{\rm eff}$ is the effective channel length that accounts for the channel-length modulation (CLM).
In the above equation, the first term represents the accumulation current flowing at the surface and $I_{\rm dd}$ is written as

$$I_{\rm dd} = -\beta\frac{(Q_{\rm n0} + Q_{\rm nl})}{2} \cdot (\phi_{\rm SL} - \phi_{\rm S0}) \tag{414}$$

$Q_{\rm n0}$ and $Q_{\rm nl}$ denote the accumlation charge in the burried layer at the source side and the drain side, respectively. The threshold voltage shift $\Delta V_{\rm th}$ due to the short-channel effect is modified by eliminating $V_{\rm bs}$ from the depletion width equation (see Eq. (32)) as

$$W_{\rm d} = \sqrt{\frac{2\epsilon_{\rm Si}(2\Phi_{\rm B})}{q \cdot \mathbf{NDEPM}}} \tag{415}$$

In the same way as for the inversion carrier the carrier mobility model for the accumulation current is written as

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_{\rm y}}{V_{\rm max}}\right)^{\mathbf{BB}}\right)^{\frac{1}{\mathbf{BB}}}} \tag{416}$$

$$\frac{1}{\mu_0} = \frac{1}{\mu_{\rm CB}} + \frac{1}{\mu_{\rm PH}} + \frac{1}{\mu_{\rm SR}} \tag{417}$$

$$\mu_{\rm SR} = \frac{\mathbf{MUESR1}}{E_{\rm eff}{}^{M_{\rm uesurface}}} \tag{418}$$

$$\mu_{\rm PH} = \frac{M_{\rm uephonon}}{E_{\rm eff}{}^{\mathbf{MUEPH0}}} \tag{419}$$

$$\mu_{\rm CB} = \mathbf{MUECB0} + \mathbf{MUECB1} \cdot \frac{-Q_{\rm n0}}{q \cdot 10^{11}} \cdot \{1 + (\phi_{\rm SL} - \phi_{\rm S0}) \cdot N_{\rm invd}\} \tag{420}$$

$$E_{\rm eff} = \frac{\left(\frac{\mathbf{NINV}}{\epsilon_{\rm Si}}\right) \cdot (-Q_{\rm n0})}{1 + (\phi_{\rm SL} - \phi_{\rm S0}) \cdot N_{\rm invde}} \tag{421}$$

where ϕ_{S0} and ϕ_{SL} are the surface potential solutions for I_{acc}, and ϕ_{b0} is the potential for the resistor region (Fig. 27). V_{max} is the saturation velocity given in Eq. (70).

Some prefactors consider the device size scaling as

$$M_{uephonon} = \mathbf{MUEPH1} \cdot \left(1 + \frac{\mathbf{MUEPHL}}{(L_{gate}/10^{-6})^{\mathbf{MUEPLP}}}\right) \cdot \left(1 + \frac{\mathbf{MUEPHW}}{(W_{gate}/10^{-6})^{\mathbf{MUEPWP}}}\right) \cdot \left(1 + \frac{\mathbf{MUEPHS}}{((L_{gate}/10^{-6})(W_{gate}/10^{-6}))^{\mathbf{MUEPSP}}}\right) \tag{422}$$

$$M_{uesurface} = \mathbf{MUESR0} \cdot \left(1 + \frac{\mathbf{MUESRL}}{(L_{gate}/10^{-6})^{\mathbf{MUESLP}}}\right) \cdot \left(1 + \frac{\mathbf{MUESRW}}{(W_{gate}/10^{-6})^{\mathbf{MUESWP}}}\right) \tag{423}$$

$$N_{invde} = \mathbf{NINVD} \cdot \left(1 + \frac{\mathbf{NINVDL}}{(L_{gate}/10^{-6})^{\mathbf{NINVDLP}}}\right) \cdot \left(1 + \frac{\mathbf{NINVDW}}{(W_{gate}/10^{-6})^{\mathbf{NINVDWP}}}\right) \tag{424}$$

where $\left(L_{gate}/10^{-6}\right)$ and $\left(W_{gate}/10^{-6}\right)$ or equivalently, $\left(L_{gate} \cdot 10^{6}\right)$ and $\left(W_{gate} \cdot 10^{6}\right)$ intend normalization to a unitless quantity, the magnitude of which stays around the unity (=1).

25.3.2 Resistor current $I_{ds,res}$

To recap, the resistor current is written as

$$I_{ds,res} = I_{res} + I_{res,leak} \tag{425}$$

In the following subsections, each component is described.

i) I_{res}

The resistor current in the neutral region is written as

$$I_{res} = q \cdot \mathbf{NF} \cdot N_{res} \cdot \mu_{res} \cdot W_{res} \cdot W_{eff} \cdot E_{dri} \tag{426}$$

where q is the elementary charge, N_{res} is the effective carrier density for the neutral region, μ_{res} is the effective mobility, W_{res} is the width for the neutral region, W_{eff} is the effective gate width, and E_{dri} is the effective electric field strength between the source and the drain within the resistor region. Further descriptions for these quantities follow below.

The effective electric field strength E_{dri} is expressed together with the quasi-Fermi potential difference

between source and drain, $V_{\mathrm{ds,res}}$, as

$$E_{\mathrm{dri}} = \frac{V_{\mathrm{ds,res}}}{L'_{\mathrm{eff}} + \mathbf{DEPRDRDL1}} \tag{427}$$

$$V_{\mathrm{ds,res}} = \frac{V_{\mathrm{ds}}}{\left[1 + \left(\frac{V_{\mathrm{ds}}}{V_{\mathrm{ds,sat,res}}}\right)^{\mathbf{DEPDDLT}}\right]^{\frac{1}{\mathbf{DEPDDLT}}}} \tag{428}$$

where L'_{eff} is the effective channel length without the channel-length modulation. $V_{\mathrm{ds,sat,res}}$ is the effective saturation voltage, obtained by solving the following set of equations iteratively:

$$-C_{\mathrm{ox}} \cdot (V_{\mathrm{G',res}} - \phi_{\mathrm{res}}) + Q_{\mathrm{res}} = 0 \tag{429}$$

$$Q_{\mathrm{res}} = \sqrt{\frac{2q \cdot \mathbf{NDEPM} \cdot \varepsilon_{\mathrm{si}}}{\beta}} \sqrt{\exp(\beta\phi_{\mathrm{res}}) - \beta\phi_{\mathrm{res}} - 1} \tag{430}$$

$$V_{\mathrm{ds,sat,res}} = \phi_{\mathrm{res}}(\geq 0) \tag{431}$$

where $V_{\mathrm{G',res}}$ is an effective gate voltage as

$$V_{\mathrm{G',res}} = V'_{\mathrm{G}} - \mathbf{DEPDVFBC} \tag{432}$$

The effective carrier concentration for I_{res} is

$$N_{\mathrm{res}} = \mathbf{NDEPM} \cdot \left(1 + \mathbf{DEPCAR} \cdot E_{\mathrm{dri}} \cdot \left(1 - \frac{1}{1 + \mu_{0,\mathrm{res}} \cdot \frac{E_{\mathrm{dri}}}{DEP_{\mathrm{vmax,res}}}}\right)\right) \tag{433}$$

where $\mu_{0,\mathrm{res}}$ represents the low-field mobility for I_{res}.

The width of the neutral region is expressed as

$$W_{\mathrm{res}} = \mathbf{TNDEP} - W_{\mathrm{s}} - W_{\mathrm{b}} \tag{434}$$

$$W_{\mathrm{s}} = \sqrt{\frac{2\epsilon_{\mathrm{Si}}\epsilon_0}{q \cdot \mathbf{NDEPM}} (-\phi_{\mathrm{res}})} \tag{435}$$

$$W_{\mathrm{b}} = \sqrt{\frac{2\epsilon_{\mathrm{Si}}\epsilon_0 N_{\mathrm{subc}}}{q \cdot \mathbf{NDEPM} \cdot (\mathbf{NDEPM} + N_{\mathrm{subc}})} \cdot (\phi_{\mathrm{bi}} - V_{\mathrm{bs}})} \tag{436}$$

where W_{s} and W_{b} represent the depletion layer thickness on the surface side, and the depletion layer thickness across the pn junction between the buried layer (resistor) and the substrate, respectively. ϕ_{bi} denotes the built-in potential of p/n junction and is defined as follows.

$$\phi_{\mathrm{bi}} = \frac{1}{\beta} \ln\left(\frac{N_{\mathrm{subc}} \cdot \mathbf{NDEPM}}{{n_{\mathrm{i}}}^2}\right) \tag{437}$$

where N_{subc} is defined elsewhere in Eq. (79). ϕ_{res} represents the surface potential calculated by solving the Poisson equation with the modified effective gate voltage $V_{\mathrm{gp,res}}$

$$V_{\mathrm{G',res}} = V'_{\mathrm{G}} - \mathbf{DEPDVFBC} \tag{438}$$

where the model parameter **DEPDVFBC** is introduced for fitting capability.

The resistor mobility μ_{res} for I_{res} is modeled as

$$\mu_{\mathrm{res}} = \frac{\mu_{0,\mathrm{res}}}{\left(1 + \left(\frac{\mu_{0,\mathrm{res}} \cdot E_{\mathrm{dri}}}{DEP_{\mathrm{vmax}}}\right)^{\mathbf{DEPBB}}\right)^{\frac{1}{\mathbf{DEPBB}}}} \tag{439}$$

where

$$E_{\text{dri}} = \frac{V_{\text{ds,res}}}{L'_{\text{eff}} - \textbf{DEPRDRDL2}} \tag{440}$$

where L'_{eff} is the effective channel length without channel length reduction due to CLM.
The low-field resistor mobility $\mu_{0,\text{res}}$ for I_{res} is modeled as

$$\frac{1}{\mu_{0,\text{res}}} = \frac{1}{\mu_{\text{CB,res}}} + \frac{1}{\mu_{\text{PH,res}}} \tag{441}$$

where

$$\mu_{\text{PH,res}} = \frac{DEP_{\text{muephonon,res}}}{E_{\text{eff,res}}{}^{\textbf{DEPMUEPH0}}} \tag{442}$$

$$\mu_{\text{CB,res}} = DEP_{\text{mue0,res}} + DEP_{\text{mue1,res}} \cdot \frac{-Q_{\text{resistor}}}{q \cdot 10^{10}} \cdot \{1 + V_{\text{ds,res}} \cdot N_{\text{invdC,res}}\} \tag{443}$$

$$Q_{\text{resistor}} = -q \cdot \textbf{NDEPM} \cdot (\textbf{TNDEP} - W_{\text{s}} - W_{\text{b}}) \tag{444}$$

The effective field for mobility evalutation is written as

$$E_{\text{eff,res}} = \frac{Q_{\text{resistor}}}{\varepsilon_{\text{si}}} \cdot \frac{1}{1 + V_{\text{ds,res}} \cdot N_{\text{invdH,res}}} \tag{445}$$

$DEP_{\text{mue0,res}}$, $DEP_{\text{mue1,res}}$, DEP_{vmax}, and $N_{\text{invd,res}}$ are

$$DEP_{\text{mue0,res}} = \textbf{DEPMUE0} \cdot \left(1 + \frac{\textbf{DEPMUE0L}}{(L_{\text{gate}}/10^{-6})^{\textbf{DEPMUE0LP}}}\right) \tag{446}$$

$$DEP_{\text{mue1,res}} = \textbf{DEPMUE1} \cdot \left(1 + \frac{\textbf{DEPMUE1L}}{(L_{\text{gate}}/10^{-6})^{\textbf{DEPMUE1LP}}}\right) \tag{447}$$

$$DEP_{\text{vmax,res}} = \textbf{DEPVMAX} \cdot \left(1 + \frac{\textbf{DEPVMAXL}}{(L_{\text{gate}}/10^{-6})^{\textbf{DEPVMAXLP}}}\right) \tag{448}$$

$$N_{\text{invdC,res}} = \textbf{DEPNINVDC} \cdot \left(1 + \frac{\textbf{DEPNINVDL}}{(L_{\text{gate}}/10^{-6})^{\textbf{DEPNINVDLP}}}\right) \cdot \left(1 + \frac{\textbf{DEPNINVDW}}{(W_{\text{gate}}/10^{-6})^{\textbf{DEPNINVDWP}}}\right) \tag{449}$$

$$N_{\text{invdH,res}} = \textbf{DEPNINVDH} \cdot \left(1 + \frac{\textbf{DEPNINVDL}}{(L_{\text{gate}}/10^{-6})^{\textbf{DEPNINVDLP}}}\right) \cdot \left(1 + \frac{\textbf{DEPNINVDW}}{(W_{\text{gate}}/10^{-6})^{\textbf{DEPNINVDWP}}}\right) \tag{450}$$

Temperature dependence can be considered in $DEP_{\text{muephonon,res}}$, $DEP_{\text{mue0,res}}$, and $DEP_{\text{vmax,res}}$, apart from the gate length dependence as follows:

$$DEP_{\text{muephonon,res}} = \frac{\textbf{DEPMUEPH1}}{\left(\frac{T}{T_{\text{nom}}}\right)^{\textbf{DEPMUETMP}}} \tag{451}$$

$$DEP_{\text{mue0,res}} = \frac{\textbf{DEPMUE0}}{\left(\frac{T}{T_{\text{nom}}}\right)^{\textbf{DEPMUE0TMP}}} \tag{452}$$

$$DEP_{\text{vmax}} = \frac{\textbf{DEPVMAX}}{1.8 + 0.4(T/\textbf{TNOM}) + 0.1(T/\textbf{TNOM})^2 - \textbf{DEPVTMP} \cdot (T/\textbf{TNOM}) - 1} \tag{453}$$

ii) $I_{\mathrm{res,leak}}$

The leakage current for the resistor region is expressed as

$$I_{\mathrm{res,leak}} = \mathbf{NF} \cdot W_{\mathrm{res,leak}} \cdot \mathbf{DEPJLEAK} \cdot \left(\frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}}\right)^{DEP_{\mathrm{WLP}}} \cdot \left(\frac{V_{\mathrm{ds,res0}}^{3}}{V_{\mathrm{ds,res0}}^{3} + 0.0005}\right) \tag{454}$$

where $W_{\mathrm{res,leak}}$ and W_{eff} represent the width of the neutral region, and the effective gate width, respectively. **DEPJLEAK** is a model parameter for the leakage current. DEP_{WLP} is a parameter that includes temperature dependence

$$DEP_{\mathrm{WLP}} = \mathbf{DEPWLP} + \mathbf{DEPWLPT} \cdot \left(1 - \frac{\mathbf{TEMP}}{\mathbf{TNOM}}\right) \tag{455}$$

$V_{\mathrm{ds,res0}}$ is the upper-limited $V_{\mathrm{ds,res}}$ which reaches asymptotically **DEPLEAK** as $V_{\mathrm{ds,res}}$ increases.

The width of the neutral region for $I_{\mathrm{res,leak}}$ is expressed as

$$W_{\mathrm{res,leak}} = \mathbf{TNDEP} - W_{\mathrm{s,leak}} - W_{\mathrm{b,leak}} \tag{456}$$

$$W_{\mathrm{b,leak}} = \sqrt{\frac{2\epsilon_{\mathrm{Si}}\epsilon_0 N_{\mathrm{subc}}}{q\mathbf{NDEPM}\left(\mathbf{NDEPM} + N_{\mathrm{subc}}\right)} \cdot \left(\phi_{\mathrm{bi}} - V_{\mathrm{bs}}\right)} \tag{457}$$

$$W_{\mathrm{s,leak}} = \sqrt{\frac{2\epsilon_{\mathrm{Si}}\epsilon_0}{q \cdot N_{\mathrm{depm}}}\left(-\phi_{\mathrm{res,leak}}\right)} \tag{458}$$

where $W_{\mathrm{s,leak}}$ and $W_{\mathrm{b,leak}}$ represent the depletion layer thickness on the surface side, and the depletion layer thickness across the pn junction between the buried layer (resistor) and the substrate, respectively. $\phi_{\mathrm{res,leak}}$ represents the surface potential calculated by solving iteratively the Poisson equation with the effective gate voltage

$$V_{\mathrm{G',leak}} = \left(\mathbf{VFBC} + \mathbf{DEPDVFBC}\right) - 3 \tag{459}$$

where “-3” determines the gate voltage at which pure generation-recombination leakage current is expected.

25.3.3 Channel Length Modulation (CLM)

The channel-length modulation model (see Chapter 11) is introduced with three model parameters (**CLM1**,**CLM2**,**CLM3**), describing the weakened gate control under the saturation condition. For the depletion model, **CLM5** and **CLM6** can be used to adjust I_{ds} gradual increase under the saturation condition.

For accumulation-mode current $I_{\mathrm{ds,acc}}$, the effective channel length in this section takes the CLM effects into account as

$$L_{\mathrm{eff}} - \Delta L \tag{460}$$

where L_{eff} represents the effective channel length (Section 3, Eq. (5)) and ΔL represents the channel length reduction (Section 11, Eqs. (72)—(74)) due to this effect. For resistor current $I_{\mathrm{ds,res}}$, the channel length reduction due to CLM is excluded.

25.3.4 Smoothing parameters

DEPQF: smoothing $V_{\mathrm{ds,sat}}$ to zero.

DEPSUBSL: adjust subthreshold slope of I_{res}.

DEPSUBSL0: adjust V_{bs} dependence of subthreshold slope of I_{res}.

DEPVGPSL: modify $V_{\mathrm{gp,res}}$ to suppress a gm peak of I_{res} when it is created.

DEPFDPD: for better fitting to C_{gg} vs. V_{gs} around $V_{\mathrm{gs}} = V_{\mathrm{fb}}$.

DEPPS: smoothe accumulation charge to zero

DEPQFRES: smoothe $V_{\mathrm{ds,sat,res}}$ to zero.

The HiSIM model parameters introduced in section 25 are summarized in Table 26.

Table 25: HiSIM model parameters introduced in section 25 of this manual.

	COMMON
CODEP	model flag to select the depletion model
NDEPM	impurity concentration of the surface layer
NDEPML	$L_{\rm gate}$ dependence of impurity concentration of the surface $\rm N^-$ layer
NDEPMLP	$L_{\rm gate}$ dependence of impurity concentration of the surface $\rm N^-$ layer
TNDEP	thickness of the surface layer
DEPMUE0	Coulomb scattering in the resistor region
DEPVMAX	saturation velocity in the resistor region
DEPBB	high-field-mobility degradation in the resistor region
DEPMUETMP	temperature dependence of the phonon scattering in the resistor region
DEPVTMP	temperature dependence of DEPVMAX
DEPMUE0TMP	temperature dependence of $DEP_{\rm mue0}$
	CODEP=1
DEPETA	$V_{\rm ds}$ dependence of the threshold voltage shift
DEPVDSEF1	effective drain potential coefficient-1 in the resistor region
DEPVDSEF1L	$L_{\rm gate}$ dependence of the effective drain potential coefficient-1
DEPVDSEF1LP	$L_{\rm gate}$ dependence of the effective drain potential coefficient-1
DEPVDSEF2	effective drain potential coefficient-2 in the resistor region
DEPVDSEF2L	$L_{\rm gate}$ dependence of the effective drain potential coefficient-2
DEPVDSEF2LP	$L_{\rm gate}$ dependence of the effective drain potential coefficient-2
DEPMUEBACK0	Coulomb scattering in the back region
DEPMUEBACK0L	$L_{\rm gate}$ dependence of the Coulomb scattering in the back region
DEPMUEBACK0LP	$L_{\rm gate}$ dependence of the Coulomb scattering in the back region
DEPMUEBACK1	Coulomb scattering in the back region
DEPMUEBACK1L	$L_{\rm gate}$ dependence of the Phonon scattering in the back region
DEPMUEBACK1LP	$L_{\rm gate}$ dependence of the Phonon scattering in the back region
DEPLEAK	leakage current coefficient
DEPLEAKL	$L_{\rm gate}$ dependence of leakage current coefficient
DEPLEAKLP	$L_{\rm gate}$ dependence of leakage current coefficient
DEPMUE1	Coulomb scattering in the resistor region
DEPMUEPH0	Phonon scattering in the resistor region
DEPMUEPH1	Phonon scattering in the resistor region
	CODEP=2
TNDEPV	$V_{\rm ds}$ dependence of the surface $\rm N^-$ layer thickness
DEPMUEA1	Modification of $\mu_{\rm res}$
DEPMUE2	Coulomb scattering of the resistor part
DEPDDLT	smoothing coefficient for $V_{\rm ds,res}$
DEPVSATR	$V_{\rm bs}$ dependence of $V_{\rm ds,sat}$ of the resistor part
DEPMUE2TMP	temperature dependence of $DEP_{\rm mue2}$
DEPLEAKL	$L_{\rm gate}$ dependence of leakage current coefficient
DEPLEAKLP	$L_{\rm gate}$ dependence of leakage current coefficient
DEPVFBC	flat-band voltage of the resistor part
DEPSUBSL	factor of the sub-threshold slope
DEPVGPSL	smoothing of $g_{\rm b}$ at $V_{\rm fb}$
DEPLEAK	leakage current coefficient

Table 26: HiSIM model parameters introduced in section 25 of this manual.

	CODEP=3
DEPCAR	high field injection in resistor region
DEPRDRDL1	pinch-off length in resistor region
DEPRDRDL2	pinch-off length in resistor region
DEPQF	smoothing of $V_{\rm ds,sat}$ to zero for dep/accum transition
DEPQFRES	smoothing of $V_{\rm ds,sat,res}$ to zero for dep/accum transition in resistor region
DEPFDPD	smoothing for FD/PD transition
DEPPS	smoothing for $\phi_{\rm S} - \phi_{\rm f}$
DEPNINVDC	Modification of Vdse dependence on Eeff (for Mu_res's Coulomb mobility)
DEPNINVDH	Modification of Vdse dependence on Eeff (for Mu_res's phonon mobility)
DEPRBR	parameter for resistance effect along substrate (for minority carrier)
DEPMUE1	Coulomb scattering in the resistor region (*common with* **CODEP**=1)
DEPMUE1L	$L_{\rm gate}$ dependence of the Phonon scattering in the resistor region
DEPMUE1LP	$L_{\rm gate}$ dependence of the Phonon scattering in the resistor region
DEPMUEPH0	Phonon scattering in the resistor region (*common with* **CODEP**=1)
DEPMUEPH1	Phonon scattering in the resistor region (*common with* **CODEP**=1)
DEPDVFBC	ajustment parameter for the gate effective voltage of the resistor part
DEPSUBSL	factor of the sub-threshold slope (*common with* **CODEP**=2)
DEPSUBSL0	factor of the sub-threshold slope
DEPVGPSL	smoothing of $g_{\rm b}$ at $V_{\rm fb}$ (*common with* **CODEP**=2)
DEPJLEAK	leakage current parameter for $J_{\rm ds,leak}$
DEPWLP	geometrical scaling exponent for leakage current
DEPLEAK	resistor leakage current

Table 27: Model Comparison

	CODEP=1	**CODEP**=2	**CODEP**=3
Structural parameters	**NDEPM, NDEPML, NDEPMLP** **TNDEP**		
Accumulation current	drift+diffusion	drift	
Quasi-Fermi	same as minority	modified	
Mobility	same as minority		
Short-channel effects	**DEPETA**	-	-
Resistor current	two terms	one term	two terms
Effective gate voltage	-	**DEPVFBC**	**DEPDVFBC**
Explicit bias dependence	-	**TNDEPV**	
Quasi-Fermi	**DEPVDSEF1**	-	-
	DEPVDSEF2	-	-
	-	**DEPDDLT**	
	-	**DEPVSATR**	-
	DEPLEAK		
Leak current	-	-	**DEPJLEAK**
Mobility			
Low-field mobility	**DEPMUEPH0**	-	**DEPMUEPH0**
	DEPMUEPH1	-	**DEPMUEPH1**
	DEPMUE1	-	**DEPMUE1**
	DEPMUE0 **DEPMUE0TMP** **DEPMUETMP** **DEPVTMP**		
	DEPMUEBACK0	-	-
	DEPMUEBACK1	-	-
	-	**DEPMUEA1**	-
	-	**DEPMUE2**	-
	-	**DEPMUE2TMP**	-
	-	-	**DEPNINVDC**
	-	-	**DEPNINVDH**
	-	-	**DEPRBR**
High-field mobility	**DEPBB** **DEPVMAX**		
	-	-	**DEPRDRDL2**
High-field injection	-	-	**DEPCAR**
CLM	-	-	**CLM1**
	-	-	**CLM2**
	-	-	**CLM3**
	-	-	**CLM5**
	-	-	**CLM6**
	-	-	**DEPRDRDL1**
Smoothing parameters	-	**DEPSUBSL**	
	-	-	**DEPSUBSL0**
	-	**DEPVGPSL**	
	const(0.3)	const(1.0)	**DEPQF**
	const(2.0)	const(4.0)	**DEPQFRES**
	const(0.12)	const(0.2)	**DEPFDPD**
	const(0.05)	const(0.05)	**DEPPS**

26 Aging Model

In power devices, aging occurs in two different places: (a) The channel region and (b) The drift region.

26.1 (a) The channel region

Two aging models are considered:

(I) the hot electron induced aging: HC Aging

(II) the N(P)BTI aging: N(P)BTI Aging

The HC aging is mostly responsible for nMOSFET and the N(P)BTI aging is for pMOSFET. The models are valid for simulating under both DC and transient conditions. Therefore, here the HC model is described for nMOSFET and the NBTI model is for pMOSFET. Both models can be activated at the same time.
To invoke the models, the following parameters should be set:

- **CODEG**=1 (for stress simulation)
  1. HC Aging model: **COISUB**=1 and **TRAPGC1MAX** > 0 should be set.
  2. N(P)BTI model: **TRAPA** > 0
- **CODEG**=0 (for post-stress simulation or normal simulation)
  1. HC Aging model: **COISUB**=1 and **TRAPGC1MAX** > 0 should be set.
  2. N(P)BTI model: **TRAPDVTH** > 0

Calculation flow is presented at the end of this subsection.

26.1.1 (I) HC Aging Model

Origin of the aging is modeled as the trap-density increase, which is included precisely in the Poisson equation solved iteratively [58]

$$\nabla^2\phi = -\frac{q}{\epsilon_{Si}}\left(p - n + N_{\rm D} - N_{\rm A} - N_{\rm tA}\right) \tag{461}$$

where p, n, $N_{\rm D}$ and $N_{\rm A}$ are the hole density, the electron density, the donor and the acceptor density, respectively. The trap density is denoted by $N_{\rm tA}$.
Two trap density distributions are considered, the shallow and the deep level, where the deep trap level is considered to be responsible for the aging. Thus $N_{\rm tA}$ is the sum of the two densities

$$N_{\rm tA} = N_{\rm tA1} + N_{\rm tA2} \tag{462}$$

where the analytical trap density is obtained after integrating the density with energy as [59, 60]

$$N_{\rm tA,n} = N_{\rm 0,n}\exp\left(\frac{E_{\rm f} - E_{\rm c}}{E_{\rm s,n}}\right) \tag{463}$$

where E_f is the Fermi energy and E_c is the conduction band edge energy. The gradient of the trap density distribution as a function of energy is described by $E_\mathrm{s,n}$. The subscript n (1 or 2) denotes the different trap levels. In modeling, the trap density at the band edge ($=g_\mathrm{c,n}$) and the trap gradient ($=E_\mathrm{s,n}$) are varied according to the stress time.

The shallow trap level, which is independent of time, is written with model parameters **TRAPGC2** and **TRAPES2** as

$$N_{0,2} = \mathbf{TRAPGC2} \cdot \mathbf{TRAPES2} \frac{\frac{kT}{\mathbf{TRAPES2}}}{\sin \frac{kT}{\mathbf{TRAPES2}}} \tag{464}$$

The deep trap level is written as

$$N_{0,1}(t) = g_\mathrm{c1,deg} \cdot E_\mathrm{s1,deg} \frac{\frac{kT}{E_\mathrm{s1,deg}}}{\sin \frac{kT}{E_\mathrm{s1,deg}}} < N_\mathrm{0,limit} \tag{465}$$

where $g_\mathrm{c1,deg}$, $E_\mathrm{s1,deg}$ and $N_\mathrm{0,limit}$ are written as

$$g_\mathrm{c1,deg} = \mathbf{TRAPGC1} + \frac{\mathbf{TRAPGC1MAX}}{gc,time1} \exp\left[-\frac{1}{2}\left(\frac{gc,time - gc,time2}{gc,time1}\right)^2\right] \tag{466}$$

$$gc,time = \ln\left(I_\mathrm{sub}{}' \cdot \mathbf{DEGTIME}/W\right) \tag{467}$$

$$gc,time1 = \ln\left(I_\mathrm{sub}{}' \cdot \mathbf{TRAPGCTIME1}/W\right) \tag{468}$$

$$gc,time2 = \ln\left(I_\mathrm{sub}{}' \cdot \mathbf{TRAPGCTIME2}/W\right) \tag{469}$$

$$E_\mathrm{s1,deg} = \mathbf{TRAPES1} + \frac{\mathbf{TRAPES1MAX}}{gc,time1} \exp\left[-\frac{1}{2}\left(\frac{es1,time - es1,time2}{es1,time1}\right)^2\right] \tag{470}$$

$$es1,time1 = \ln\left(I_\mathrm{sub}{}' \cdot \mathbf{TRAPESTIME1}/W\right) \tag{471}$$

$$es1,time2 = \ln\left(I_\mathrm{sub}{}' \cdot \mathbf{TRAPESTIME2}/W\right) \tag{472}$$

$$N_\mathrm{0,limit} = \mathbf{TRAPGCLIM} \cdot \mathbf{TRAPESLIM} \frac{\frac{kT}{\mathbf{TRAPESLIM}}}{\sin \frac{kT}{\mathbf{TRAPESLIM}}} \tag{473}$$

where $\mathbf{TRAPGC1,2,LIM}$ and $\mathbf{TRAPES1,2,LIM}$ are model parameters for the deep and the shallow trap densities. The time at which observable aging starts is determined by the model parameters **TRAPGCTIME1** and **TRAPESTIME1**, and the time at which aging enhancement ends is determined by **TRAPGCTIME2** and **TRAPESTIME2**. **DEGTIME** determines the aging time to be predicted.

$I_\mathrm{sub}{}'$ is determined as

a) DC simulation

$$I_\mathrm{sub}{}' = I_\mathrm{sub} \tag{474}$$

b) Circuit simulation

$$I_\mathrm{sub}{}' = \frac{\sum^{\mathbf{DEGTIME0}} I_\mathrm{sub}}{\mathbf{DEGTIME0}} \tag{475}$$

For the V_{ds} dependence, the model parameter **TRAPLX** is introduced as

$$N_{\mathrm{tA}} = N_{\mathrm{tA}} \cdot \exp\left(-\frac{V_{\mathrm{dseff}} - \phi_{\mathrm{SL}} + \phi_{\mathrm{S0}}}{\mathbf{TRAPLX}}\right) \tag{476}$$

The mobility degradation due to the trapped carriers is considered. In the effctive electric field of its original formulation (Eq. (58)) as

$$E_{\mathrm{eff0}} = E_{\mathrm{eff0}} + \frac{\mathbf{TRAPN}}{\epsilon_{\mathrm{Si}}} \cdot Q_{\mathrm{trap}} \cdot f(\phi_{\mathrm{S}}) \tag{477}$$

where Q_{trap} is the integrated trap density along the vertical direction. **TRAPN** is a fitting parameter in the same way as **NDEP** and **NINV**.
In addition to the trap density N_{tA} the model eliminating the midgap density can be activated by the Flag **CODEGES0**, realizing unoccupied midgap density with two model parameters **TRAPGC0** and **TRAPES0**.
DEGTIME determines the aging time to be predicted the device aging. In principle this is not model parameter but to be determined from outside. To distinguish the aging simulation under the DC condition for parameter extraction and the circuit simulation, the Flag **CODEGSTEP** must be determined.

26.1.2 (II) N(P)BTI Aging Model: Carrier trapping at interface

The hole trapping at Si/oxide interface of the NBTI is considered and modeled as the threshold voltage shift $\delta V_{\mathrm{th,trap}}$ as [61]

$$\delta V_{\mathrm{th,trap}} = \mathbf{TRAPA} \cdot \exp\left(\mathbf{TRAPB} \cdot E_{\mathrm{ox}}\right) \cdot \left[1 - \exp\left(-\frac{t_{\mathrm{s}}}{\mathbf{TRAPBTI}}\right)\right] \tag{478}$$

$$E_{\mathrm{ox}} = \frac{V_{\mathrm{Gon}} - \delta V_{\mathrm{th,trap}} - \phi_{\mathrm{S}}}{T_{\mathrm{ox}}} \tag{479}$$

$$t_{\mathrm{s}} = T_{\mathrm{cycle}} \cdot \mathbf{DEGTIME} \tag{480}$$

where ϕ_{S} is fixed to $2\Phi_{\mathrm{B}}$ (Eq. (33)) giving the threshold voltage condition, and T_{cycle} is calculated by integrating the stress time during circuit operation for **DEGTIME0** long. V_{Gon} is averaged V'_{G} under the switching-on condition.
The mobility degradation due to the trapped carriers is considered in the effective electric field in the same way for the HC effect (Eq. (477)) as

$$E_{\mathrm{eff0}} = E_{\mathrm{eff0}} + \frac{\mathbf{TRAPP} \cdot \Delta V_{\mathrm{th,trap}}}{T_{\mathrm{ox}}} \cdot f(\phi_{\mathrm{S}}) \tag{481}$$

where **TRAPP** is a fitting parameter.

The present implementation focuses on long-term aging, and no trap emission in included.

26.2 (b) The drift region

If $V_{\rm gs}$ and $V_{\rm ds}$ are high, the electric field increase in the drift region, especially at the STI corner, becomes very high. As the result, the impact ionization occurs. The causes a modification of the potential distribution. Modeling is done by modifying the internal node potential, which causes the carrier density change.

$$
\begin{aligned}
N_{\rm drift} = &\,\mathbf{NOVER}\left\{1+\mathbf{RDRCAR}\left(\frac{V_{\rm ddp}}{L_{\rm drft}-\mathbf{RDRDL2}}\right)\left(1-\frac{1}{1+\frac{\mu_{\rm drift0}}{V_{\rm max_drift}}\cdot\frac{V_{\rm ddp}}{L_{\rm drift}}}\right)\right\}\\
&+\left(\mathbf{RDRQOVER}\frac{-Q'_{\rm over}}{q}\right)\\
&+\mathbf{NOVER}\cdot D_{\rm vddp}
\end{aligned}
\tag{482}
$$

For the $V_{\rm ds}$ dependence, the model parameter **TRAPDLX** is introduced as

$$
D_{\rm vddp} = D_{\rm vddp,deg}\cdot\exp\left(-\frac{V_{\rm dseff}-\phi_{\rm SL}+\phi_{\rm S0}}{\mathbf{TRAPDLX}}\right) \tag{483}
$$

$$
D_{\rm vddp,deg} = \mathbf{TRAPDVDDP} + \frac{\mathbf{TRAPD1MAX}}{time1}\exp\left[-\frac{1}{2}\left(\frac{time-time2}{time1}\right)^2\right] \tag{484}
$$

$$
time = \ln\left(I_{\rm ds}{}'\cdot\mathbf{DEGTIME}/W\right) \tag{485}
$$

$$
time1 = \ln\left(I_{\rm ds}{}'\cdot\mathbf{TRAPDTIME1}/W\right) \tag{486}
$$

$$
time2 = \ln\left(I_{\rm ds}{}'\cdot\mathbf{TRAPDTIME2}/W\right) \tag{487}
$$

where **TRAPDVDDP** and **TRAPD1MAX** are a model parameter. The time at which observable aging starts is determined by the model parameter **TRAPDTIME1** and the time at which aging enhancement ends is determined by **TRAPDTIME2**.
$I_{\rm ds}{}'$ is determined as

a) DC simulation

$$
I_{\rm ds}{}' = I_{\rm ds} \tag{488}
$$

b) Circuit simulation

$$
I_{\rm ds}{}' = \frac{\sum^{\mathbf{DEGTIME0}} I_{\rm ds}}{\mathbf{DEGTIME0}} \tag{489}
$$

The HiSIM model parameters introduced in section 26 are summarized in Table 28.

Table 28: HiSIM model parameters introduced in section 26 of this manual.

	Aging Conditions: These are in principle no model parameters. Please refer simulator definition
DEGTIME	stress duration
DEGTIME0	circuit simulation duration
	HC Aging Model
TRAPTAUCAP	time constant of trap caputure
TRAPLX	Vds dependence of deep trap
TRAPGC1	deep trap density
TRAPGC1MAX	time dependent deep trap
TRAPGCTIME1	aging start time
TRAPGCTIME2	aging saturation time
TRAPGCLIM	limit of trap density
TRAPESLIM	limit of trap density gradient
TRAPES1	deep trap density gradient
TRAPES1MAX	time dependent deep trap density gradient
TRAPESTIME1	aging start time
TRAPESTIME2	aging saturate time
TRAPN	mobility degradation due to traps
TRAPGC2	shallow trap density
TRAPES2	shallow trap density coefficient
TRAPGC0	midgap trap density
TRAPES0	midgap trap density gradient
TRAPD1MAX	time dependent drift-region trap density gradient
TRAPDTIME1	aging start time
TRAPDTIME2	aging saturate time
TRAPDLX	Vds dependence of trap in the drift region
TRAPDVDDP	time dependent the carrier type accumulated in the drift region
	N(P)BTI Aging Model
TRAPA	coeffcient of existing interface trap density
TRAPB	coeffcient of existing interface trap density
TRAPP	coefficient of BTI trap for Eeff
TRAPBTI	coeffcient of existing interface trap density
	Flags
CODEG	set to 1 for aging simulation
CODEGSTEP	set to 0 for aging for DC and set to 1 for circuit aging

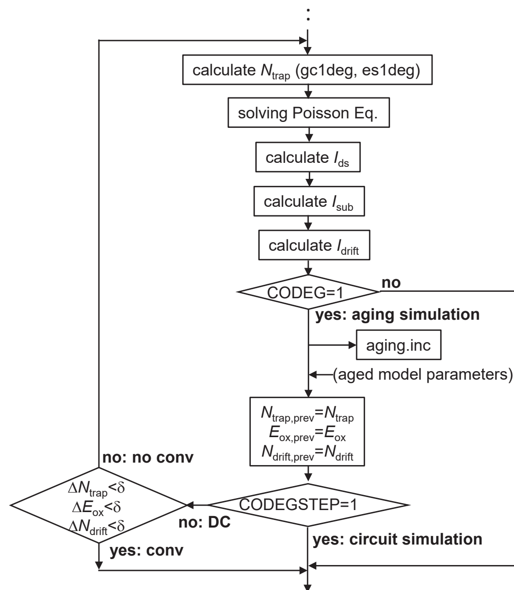

Fig. 28: Calculation Flow for aging.

27 Binning Model

The binning option is introduced to secure enough accuracy of model calculation results, even though the effects observed are not modeled yet. The binning method is the same as that used in BSIM3/4

$$\mathit{Bin_HiSIM_model_parameter} = \mathbf{HiSIM_model_parameter} + \frac{\mathbf{P1}}{L_{\mathrm{bin}}} + \frac{\mathbf{P2}}{W_{\mathrm{bin}}} + \frac{\mathbf{P3}}{L_{\mathrm{bin}} W_{\mathrm{bin}}} \tag{490}$$

where **P1**, **P2**, and **P3** are model parameters for **L HiSIM_model_parameter**, **W HiSIM_model_parameter**, and **L · W HiSIM_model_parameter**, respectively, and

$$L_{\mathrm{bin}} = \left(L_{\mathrm{gate}} \cdot 10^6\right)^{\mathbf{LBINN}} \tag{491}$$

$$W_{\mathrm{bin}} = \left(W_{\mathrm{gate}} \cdot 10^6\right)^{\mathbf{WBINN}} \tag{492}$$

The HiSIM model parameters introduced in section 27 are summarized in Table 29.

Table 29: HiSIM model parameters introduced in section 27 of this manual.

Parameter	Description
LBINN	power of L_{drawn} function
WBINN	power of W_{drawn} function
LMAX	maximum length of L_{drawn} valid
LMIN	minimum length of L_{drawn} valid
WMAX	maximum length of W_{drawn} valid
WMIN	minimum length of W_{drawn} valid

The model parameters which are effectively binned and which should not be used for binning are summarized in Table 30.

Table 30: HiSIM model parameters to be used for the binning option.

parameter	recommended	usable	not be used
basic	**NSUBC**		**TOX**, **KAPPA**, **XLD**
	VFBC		**LL**, **LLD**, **LLN**, **XWD**
			WL, **WLD**, **WLN**, **VBI**
mobility	**MUECB0**	**NINV**	**MUEPH0**, **MUESR0**
	MUECB1	**NDEP**	**MUEPHL**, **MUEPLP**
	MUEPH1		**MUEPHS**, **MUEPSP**
	MUESR1		**MUESRL**, **MUESLP**
			MUEPHW, **MUEPWP**
			MUESRW, **MUESWP**
	VMAX	**VOVER**	**VOVERP**
			BB
short-channel	**NSUBP**	**SC1**, **SC2**, **SC3**	**PARL2**, **LP**
& pocket		**SCP1**, **SCP2**, **SCP3**	**LPEXT**
		NPEXT	**SCP21**, **SCP22**, **BS1**, **BS2**
poly-depletion		**PGD1**	**PGD2**, **PGD4**
CLM		**CLM1**, **CLM2**, **CLM3**	**CLM5**, **CLM6**
QME			**QME1**, **QME2**, **QME3**
resistance			**RSH**, **RSHG**
			RBPB, **RBPD**, **RBPS**
		RTH0	
$W_{\rm gate}$ depnd.		**WFC**, **WVTH0**	**NSUBPW**, **NSUBPWP**
small size		**WL2**	**WL2P**
temperature		**EG0**	**TNOM**
		BGTMP1, **BGTMP2**	**EGIG**
		VTMP, **MUETMP**	**IGTEMP2**, **IGTEMP3**
		VDIFFJ	
STI	**WSTI**, **VTHSTI**		**WL1**, **WL1P**
	NSTI		
	SCSTI1, **SCSTI2**		
overlap	**LOVER**, **VFBOVER**	**CGSO**, **CGDO**, **CGBO**	
	NOVER	**NOVERS**, **CVDSOVER**	
$I_{\rm sub}$	**SUB1**	**SUB2**, **SVDS**	**SUB1L**, **SUB1LP**, **SUB2L**
		SVBS, **SVGS**	**SLG**, **SVGSL**, **SVGSLP**
		IBPC1, **IBPC2**	**SVGSW**, **SVGSWP**, **SLGL**
			SLGLP, **SVBSL**, **SVBSLP**
		IPBC1, **IPBC2**	
$I_{\rm gate}$	**GLEAK1**, **GLEAK2**	**GLEAK6**	**GLEAK4**, **GLEAK5**
	GLEAK3		**GLEAK7**
$I_{\rm gs}/I_{\rm gd}$	**GLKSD1**, **GLKSD2**		**GLKSD3**
$I_{\rm gb}$	**GLKB1**, **GLKB2**		
$I_{\rm GIDL}$		**GIDL1**, **GIDL2**	
junction		**JS0**, **JS0SW**, **NJ**, **CISBK**	
noise	**NFTRP**, **NFALP**	**FALPH**	**CIT**
LOD	**NSUBCSTI1**		
	NSUMCSTI2		
	NSUBCSTI3		
	NSUBPSTI1		
	NSUBPSTI2		
	NSUBPSTI3		
	MUESTI1		
	MUESTI2		
	MUESTI3		

28 Exclusion of Modeled Effects and Model Flags

1. To exclude specific modeled effects, following parameter settings should be chosen:

Effect	Setting
Short-Channel Effect	**SC1** = **SC2** = **SC3** = 0
Reverse-Short-Channel Effect	**LP** = 0
Quantum-Mechanical Effect	**QME1** = **QME3** = 0
Poly-Depletion Effect	**PGD1** = **PGD2** = 0
Channel-Length Modulation	**CLM1** = **CLM2** = **CLM3** = 0
Narrow-Channel Effect	**WFC** = **MUEPHW** = **WL1** = 0
Small-Size Effect	**WL2** = 0

Following flags are prepared to select required model options.

2. Selection for asymmetrical (LDMOS) or HV-MOS structure is done:

   COSYM = 0: LDMOS (default)

   COSYM = 1: symmetrical/asymmetrical HV-MOS

3. Selection for $R_{\rm drift}$ model:

   CORDRIFT = 0: old model provided for earlier versions of HiSIM_HV 1.

   CORDRIFT = 1: new model (default).

4. Drift region resistances

   CORS = 0: no resistance on the source side will be included.

   CORS = 1: the source-side resistance will be included.

   CORD = 0: no resistance on the drain side will be included.

   CORD = 1: the drain-side resistance will be included.

5. Contact resistances $R_{\rm s}$ and $R_{\rm d}$ are included:

   CORSRD = 0: no

   CORSRD = 1 & **RS**/**RD** $\neq 0$: yes, as internal resistance nodes

   CORSRD = 2 & **RD** $\neq 0$: yes, analytical description

   CORSRD = 3 & **RD** $\neq 0$: yes, both internal nodes and analytical description (default)

   CORSRD = -1 & **RS**/**RD** $\neq 0$: yes, as external resistance nodes

   Note. These are valid for **CORDRIFT** = 0 only.

6. Overlap charges/capacitances are added to intrinsic ones:

   COADOV = 0: no

   COADOV = 1: yes (default)

7. Bias dependent overlap capacitance model is selected at drain side:

   COOVLP = 0: constant overlap capacitance

   COOVLP = 1: yes (default) including constant values as option

8. Bias dependent overlap capacitance model is selected at source side:

   COOVLPS = 0: constant overlap capacitance (default)

   COOVLPS = 1: yes including constant values as option

9. Method for calculating potential in overlap region is selected:

COQOVSM = 0: analytical equation excluding inversion charge

COQOVSM = 1: iterative solution (default)

COQOVSM = 2: analytical equation including inversion charge

10. Self-Heating Effect is considered:

COSELFHEAT = 0: no (default)

COSELFHEAT = 1: yes, power clipping (up to version 2.3.0)

COSELFHEAT = 2: yes, temperature clipping (new)

11. Substrate current I_{sub} is calculated:

COISUB = 0: no (default)

COISUB = 1: yes

12. Gate current I_{gate} is calculated:

COIIGS = 0: no (default)

COIIGS = 1: yes

13. GIDL current I_{GIDL} is calculated:

COGIDL = 0: no (default)

COGIDL = 1: yes

14. STI leakage current $I_{\mathrm{ds,STI}}$ is calculated:

COISTI = 0: no (default)

COISTI = 1: yes

CAUTION: This model is not supported yet in the depletion mode model.

15. Non-quasi-static (NQS) mode is invoked:

CONQS = 0: no (default)

CONQS = 1: yes

A separate flag for NQS effects on overlap charge is available.

CONQSOV = 0: off (default)

CONQSOV = 1: on

16. Gate-contact resistance is included:

CORG = 0: no (default)

CORG = 1: yes

17. Substrate resistance network is invoked:

CORBNET = 0: no (default)

CORBNET = 1: yes

18. $1/f$ noise is calculated:

COFLICK = 0: no (default)

COFLICK = 1: yes

19. Thermal noise is calculated:

    COTHRML = 0: no (default)

    COTHRML = 1: yes

    CAUTION: This model is not supported yet in the depletion mode model.

20. Induced gate and cross correlation noise are calculated:

    COIGN = 0 ∥ **COTHRML** = 0: no (default)

    COIGN = 1 & **COTHRML** = 1: yes

    CAUTION: This model is not supported yet in the depletion mode model.

21. Previous ϕ_S is used for the iteration:

    COPPRV = 0: no

    COPPRV = 1: yes (default)

22. Parameter variations for the DFM support is considered:

    CODFM = 0: no (default)

    CODFM = 1: yes

23. Previous Ids is used for calculating source/drain resistance effect (R_s and/or $R_d \neq 0$): This flag is inactivated.

    COIPRV = 0: no (default)

    COIPRV = 1: yes

24. Selection for temperature dependence of models:

	$R_{d0,temp}$	$R_{dvd,temp}$	V_{max}	N_{invd}	
COTEMP = 0:	T	$T0$	$T0$	$T0$	:default & backward compatible
COTEMP = 1:	$T0$	$T0$	$T0$	$T0$	
COTEMP = 2:	T	T	T	T	
COTEMP = 3:	T	T	$T0$	$T0$	

where T includes the temperature increase by the self-heating effect and $T0$ is without.

25. Selection for the 5th node:

    COSUBNODE = 0: the 5th node is the thermal nodel (default).

    COSUBNODE = 1: the 5th node is the V_{sub} node.

26. Selection for output message whether model parameter is within recommendend range:

    COERRREP = 0: no message is given.

    COERRREP = 1: range check result is given (default).

27. Selection for the depletion mode model:

    CODEP = 0: conventional HVMOS/LDMOS model (default).

    CODEP = 1: 2.20 old depletion mode HVMOS/LDMOS model.

    CODEP = 2: 2.30 old depletion mode HVMOS/LDMOS model.

    CODEP = 3: 2.40 new depletion mode HVMOS/LDMOS model.

28. Selection for the $V_{\mathrm{ds,sat}}$ model :

    CODDLT = 0: previous $V_{\mathrm{ds,sat}}$ model.

    CODDLT = 1: new $V_{\mathrm{ds,sat}}$ model (default).

29. Hard breakdown (avalanche breakdown) is calculated:

    COHBD = 0: no (default)

    COHBD = 1 or -1: yes

30. Snapback is calculated:

    COSNP = 0: no (default)

    COSNP = 1: yes; **CORBNET**=1 and **COISUB**=1 should be also specified.

31. Diode connection:

    CODIO=0: All three diode components (bottom area, STI sidewall and gate sidewall) connect the outer branches (sb,s) or (db,d). (default)

    CODIO=1: Gate-sidewall peripheral component connects the inner branches (bp,sp) or (bp,dp) and remaining components connect the outer branches (sb,s) or (db,d).

32. Selection for the aging model:

    CODEG = 0: no (default)

    CODEG = 1: yes

33. Selection for simulation step in the aging model:

    CODEGSTEP = 0: circuit (default)

    CODEGSTEP = 1: DC stress simulation

34. Selection for realizing unoccupied midgap density:

    CODEGES0 = 0: no (default)

    CODEGES0 = 1: yes

35. Selection for bias-dependent overlap length (section 16.3)

    COOVJUNC = 0: using $\phi_{\mathrm{s,over}}$ (default; original implementation)

    COOVJUNC = 1: using V_{db} (more reasonable implementation)

36. Selection for capacitance due to trench gate (section 16.5)

    COTRENCH = 0: no (default)

    COTRENCH = 1: yes

29 List of Instance Parameters

Partly the same instance-parameter names and their definitions as in the BSIM3/4 models are adopted for the convenience of HiSIM users. The HiSIM Research Group wishes to acknowledge the UC Berkeley BSIM Research Group for the introduction of these instance parameters.

L	gate length ($L_{\rm gate}$) default: **L** $= 2\mu m$
W	gate width ($W_{\rm gate}$) default: **W** $= 5\mu m$
	** Diode **
AD	area of drain junction
AS	area of source junction
PD	perimeter of drain junction
PS	perimeter of source junction
	** Source/Drain Resistance **
NRS	number of source squares
NRD	number of drain squares
	** Gate Resistance **
XGW	distance from the gate contact to the channel edge
XGL	offset of the gate length
NF	number of gate fingers
M	multiplication factor
NGCON	number of gate contacts
	** Substrate Network **
RBPB	substrate resistance network
RBPD	substrate resistance network
RBPS	substrate resistance network
	** Length of Diffusion **
SA	length of diffusion between gate and STI
SB	length of diffusion between gate and STI
SD	length of diffusion between gate and gate
	** Temperature **
DTEMP	device temperature change
	** Design for Manufacturability **
NSUBCDFM	substrate impurity concentration
	** Substrate Current **
SUBLD1	substrate current induced in $L_{\rm drift}$ (inactivated)
SUBLD2	substrate current induced in $L_{\rm drift}$ (inactivated)
	** Resistance **
LDRIFT1	lenght of lightly doped drift region (default: 0)
LDRIFT2	length of heavily doped drift region (defailt: 1 μm)
LDRIFT1S	lenght of lightly doped drift region in source side (default: 0)
LDRIFT2S	length of heavily doped drift region in source side (defailt: 1 μm)
	** Overlap **
LOVER	lenght of overlap region in source side for LDMOS
LOVERLD	length of overlap region in drain side
LOVERS	lenght of overlap region in source side for HVMOS
COSELFHEAT	falg to switch on the self-heating effect
COSUBNODE	flag for selection of the 5th node

NPEXT	maximum concentration of pocket tail
FALPH	power of f describing deviation of $1/f$
RS	source-contact resistance of LDD region
RD	drain-contact resistance of LDD region
RD22	V_{bs} dependence of **RD** for **CORSRD**=2,3
RD23	modification of **RD** for **CORSRD**=2,3
RD24	V_{gs} dependence of **RD** for **CORSRD**=2,3
RDVG11	V_{gs} dependence of **RD** for **CORSRD**=1,3
RDICT1	**LDRFIT1** dependence of resistance for **CORSRD**=1,3
RDOV13	alternative L_{over} depepdence model for **CORSRD**
RDSLP1	**LDRFIT1** dependence of resistance for **CORSRD**=1,3
RDVB	V_{bs} dependence of **RD** for **CORSRD**=1,3
RDVD	V_{ds} dependence of **RD** for **CORSRD**=1,3
RTH0	thermal resistance
VOVER	velocity overshoot effect
CGBO	gate-to-bulk overlap capacitance
CVDSOVER	modification of the C_{gg} peak for $V_{\mathrm{ds}} \neq 0$
POWRAT	thermal dissipation

30 Default Parameters and Limits of the Parameter Values

The maximum and minimum limits of the model parameter are recommended values. These values may be violated in some specific cases. "default" in remarks means that the default value is preferable.

Parameter	Unit	Min	Max	Default	Remarks
VERSION		2.20	2.40	2.40	
TOX	[m]			7n	
XL	[m]			0	
XW	[m]			0	
XLD	[m]	0	50n	0	
XWD	[m]	-100n	300n	0	
XWDLD	[m]			0	given if $\neq$ **XWD**
XWDC	[m]	-500n	500n	0	given if $\neq$ **XWD**
TPOLY	[m]			200n	
LL	[$m^{\mathbf{LLN+1}}$]			0	
LLD	[m]			0	
LLN	[—]			0	
WL	[$m^{\mathbf{WLN+1}}$]			0	
WLD	[m]			0	
WLN	[—]			0	
NSUBC	[cm^{-3}]	1×10^{16}	1×10^{19}	3×10^{17}	**CODEP**=0
		1×10^{16}	1×10^{19}	5×10^{16}	**CODEP**=1,2,3
NSUBP	[cm^{-3}]	1×10^{16}	1×10^{19}	1×10^{18}	**CODEP**=0
		1×10^{16}	1×10^{19}	1×10^{17}	**CODEP**=1,2,3
DDRIFT	[m]			1.0×10^{-6}	
NSUBSUB	[cm^{-3}]			1.0×10^{15}	required for $V_{\mathrm{sub,s}}$ dependence
LP	[m]	0	300n	15n	**CODEP**=0
		0	300n	0n	**CODEP**=1,2,3
∗**NPEXT**	[cm^{-3}]	1×10^{16}	1×10^{18}	5×10^{17}	
∗**LPEXT**	[m]	1×10^{-50}	1×10^{-5}	1×10^{-50}	
VFBC	[V]	-1.2	0.0	-1.0	**CODEP**=0
		-1.2	0.8	-0.2	**CODEP**=1,2,3
VBI	[V]	1.0	1.2	1.1	
KAPPA	[—]			3.9	
EG0	[eV]	1.0	1.3	1.1785	
BGTMP1	[$eV\,K^{-1}$]	50μ	1000μ	90.25μ	default
BGTMP2	[$eV\,K^{-2}$]	-1μ	1μ	0.1μ	
TNOM	[°C]	22	32	27	
VMAX	[$cm\,s^{-1}$]	1MEG	20MEG	10MEG	
VMAXT1	[$cm\,(sK)^{-1}$]			0	
VMAXT2	[$cm\,(sK^2)^{-1}$]			0	
VOVER	[$m^{\mathbf{VOVERP}}$]	0	4.0	0.3	
VOVERP	[—]	0	2.0	0.3	
∗**VTMP**	[—]	-2.0	1.0	0	
QME1	[Vm]	0	1n	0	
QME2	[V]	1.0	3.0	2.0	
QME3	[m]	0	500p	0	
PGD1	[V]	0	30m	0	
PGD2	[V]	0	1.5	1.0	
∗**PGD4**	[—]	0	3.0	0	
PARL2	[m]	0	50n	10n	
SC1	[—]	0	10	0	
SC2	[V^{-1}]	0	1	0	

Parameter	Unit	Min	Max	Default	Remarks
∗**SC3**	[V^{-1}m]	0	20μ	0	
∗ ∗ **SC4**	[1/V]	0		0	
SCP1	[—]	0	10	0	
SCP2	[V^{-1}]	0	1	0	
∗**SCP3**	[V^{-1}m]	0	200n	0	
∗**SCP21**	[V]	0	5.0	0	
∗**SCP22**	[V^4]	0	0	0	reset to zero
∗**BS1**	[V^2]	0	0.05	0	
∗**BS2**	[V]	0.5	1.0	0.9	
∗**PTL**	[V]	0		0	
∗**PTLP**	[—]			1.0	
∗**PTP**	[—]	3.0	4.0	3.5	
∗**PT2**	[V^{-1}]	0		0	
∗**PT4**	[V^{-2}]	0		0	
∗**PT4P**	[—]	0		1	
∗**GDL**	[—]	0	0.22	0	
∗**GDLP**	[—]			0	
∗**GDLD**	[m]			0	
MUECB0	[$cm^2V^{-1}s^{-1}$]	100	100k	1k	
MUECB1	[$cm^2V^{-1}s^{-1}$]	5	10k	100	
MUEPH0	[—]	0.25	0.35	0.3	default
MUEPH1	[$cm^2V^{-1}s^{-1}$ $(V\,cm^{-1})^{\mathbf{MUEPH0}}$]	2k	30k	20k (nMOS) 9k(pMOS)	
MUEEFB	[V^{-1}]			0.0	
MUETMP	[—]	0.5	2.5	1.5	
∗**MUEPHL**	[—]			0	
∗**MUEPLP**	[—]			1.0	
MUESR0	[—]	1.8	2.2	2.0	default
MUESR1	[$cm^2V^{-1}s^{-1}$ $(V\,cm^{-1})^{\mathbf{MUESR0}}$]	$1{\times}10^{14}$ $1{\times}10^{14}$	$1{\times}10^{16}$ $1{\times}10^{16}$	$6{\times}10^{14}$ $5{\times}10^{15}$	**CODEP**=0 **CODEP**=1,2,3
∗**MUESRL**	[—]			0	
∗**MUESLP**	[—]			1.0	
NDEP	[—]	0	1.0	1.0	
∗**NDEPL**	[—]			0	
∗**NDEPLP**	[—]			1.0	
NINV	[—]	0	1.0	0.5	
NINVD	[1/V]	0		0.0	
NINVDW	[—]	0		0.0	
NINVDWP	[—]	0		1.0	
NINVDT1	[1/K]	0		0.0	
NINVDT2	[$1/K^2$]	0		0.0	
BB	[—]			2.0(nMOS) 1.0(pMOS)	
WFC	[$F\,m^{-1}$]	$-5.0{\times}10^{-15}$	$1{\times}10^{-6}$	0	
∗**WVTH0**	[V]			0	
∗**NSUBCW**	[—]			0	
∗**NSUBCWP**	[—]			1	
∗**NSUBP0**	[cm^{-3}]			0	
∗**NSUBWP**	[—]			1.0	
∗**MUEPHW**	[—]			0	possibly negative
∗**MUEPWP**	[—]			1.0	
∗**MUESRW**	[—]			0	possibly positive
∗**MUESWP**	[—]			1.0	
∗**VTHSTI**	[V]			0	

Parameter	Unit	Min	Max	Default	Remarks
VDSTI	[—]			0	
SCSTI1	[—]			0	
SCSTI2	[V^{-1}]			0	
NSTI	[cm^{-3}]	1×10^{16}	1×10^{19}	5×10^{17}	
WSTI	[m]			0	
WSTIL	[—]			0	
WSTILP	[—]			1.0	
WSTIW	[—]			0	
WSTIWP	[—]			1.0	
WL1	[—]			0	
WL1P	[—]			1.0	
NSUBPSTI1	[m]			0	
NSUBPSTI2	[—]			0	
NSUBPSTI3	[—]			1.0	
MUESTI1	[m]			0	
MUESTI2	[—]			0	
MUESTI3	[—]			1.0	
WL2	[V]			0	
WL2P	[—]			1.0	
∗**MUEPHS**	[—]			0	
∗**MUEPSP**	[—]			1.0	
∗**VOVERS**	[—]			0	
∗**VOVERSP**	[—]			0	
CLM1	[—]	0.01	1.0	0.05	**CODEP**=0,3
CLM2	[—]	1.0	4.0	2.0	**CODEP**=0,3
CLM3	[—]	0.5	5.0	1.0	**CODEP**=0,3
CLM5	[—]	0	2.0	1.0	**CODEP**=0,3
CLM6	[—]	0	20.0	0	**CODEP**=0,3
SUB1	[V^{-1}]			10	
SUB1L	[$m^{\mathbf{SUB1LP}}$]			2.5×10^{-3}	
SUB1LP	[—]			1.0	
SUB2	[V]			25.0	
SUB2L	[m]	0	1.0	2×10^{-6}	
SUBTMP	[1/T]	0	5×10^{-3}	0	
SVDS	[—]			0.8	
SLG	[m]			3×10^{-8}	
SLGL	[$m^{\mathbf{SLGLP}}$]			0	
SLGLP	[—]			1.0	
SVBS	[—]			0.5	
SVBSL	[$m^{\mathbf{SVBSLP}}$]			0	
SVBSLP	[—]			1.0	
SVGS	[—]			0.8	
SVGSL	[$m^{\mathbf{SVGSLP}}$]			0	
SVGSLP	[—]			1.0	
SVGSW	[$m^{\mathbf{SVGSWP}}$]			0	
SVGSWP	[—]			1.0	
IBPC1	[VA^{-1}]	0	1.0×10^{12}	0	
IBPC1L	[—]			0	
IBPC1LP	[—]			1.0	
IBPC2	[V^{-1}]	0	1.0×10^{12}	0	
SUBLD1	[V^{-1}]			0	
SUBLD1L	[$\mu m^{\mathbf{SUBLD1LP}}$]			0	
SUBLD1LP	[—]			1.0	
SUBLD2	[mV^{-1}]			0	
XPDV	[]	0		0	

Parameter	Unit	Min	Max	Default	Remarks
XPVDTH	[]	0		0	
XPVDTHG	[]	-1	1	0	
MPHDFM	[—]	-3	3	-0.3	
SAREF	[m]			1.0×10^{-6}	
SBREF	[m]			1.0×10^{-6}	
GLEAK1	[$V^{-3/2}s^{-1}$]			50	
GLEAK2	[$V^{-1/2}cm^{-1}$]			10MEG	
GLEAK3	[—]			60×10^{-3}	
GLEAK4	[m^{-1}]			4.0	
∗**GLEAK5**	[$V\,m^{-1}$]			7.5×10^{3}	
∗**GLEAK6**	[V]			250×10^{-3}	
∗**GLEAK7**	[m^2]			1×10^{-6}	
∗**EGIG**	[V]			0.0	
∗**IGTEMP2**	[V K]			0	
∗**IGTEMP3**	[$V\,K^2$]			0	
GLKSD1	[$A\,m\,V^{-2}$]			1×10^{-15}	
GLKSD2	[$V^{-1}m^{-1}$]			1×10^{3}	
GLKSD3	[m^{-1}]			-1×10^{3}	
GLKB1	[$A\,V^{-2}\,m^{-2}$]			5×10^{-16}	
GLKB2	[$m\,V^{-1}$]			1.0	
GLKB3	[V]			0	
GLPART1	[-]	0	1.0	0.5	
FN1	[$V^{-1.5}\cdot$ m^2]			50	
FN2	[$V^{-0.5}\cdot$ m^{-1}]			170×10^{-6}	
FN3	[V]			0	
FVBS	[—]			12×10^{-3}	
GIDL1	[$V^{-3/2}s^{-1}m$]			2.0	
GIDL2	[$V^{-0.5}m^{-1}$]			3×10^{7}	
GIDL3	[—]			0.9	
∗**GIDL4**	[V]			0	
∗**GIDL5**	[—]			0.2	
VBSMIN	[V]				no more required
VGSMIN	[V]			-100(nMOS)	fixed
				100(pMOS)	fixed
VZADD0	[V]			0.01	fixed
PZADD0	[V]			0.005	fixed
DDLTMAX	[—]	1	10	10	
DDLTSLP	[μm^{-1}]	0	20	10	
DDLTICT	[—]	-3	20	0	
JS0	[$A\,m^{-2}$]			0.5×10^{-6}	
JS0D	[$A\,m^{-2}$]			**JS0**	
JS0S	[$A\,m^{-2}$]			**JS0**	
JS0SW	[$A\,m^{-1}$]			0	
JS0SWD	[$A\,m^{-1}$]			**JS0SW**	
JS0SWS	[$A\,m^{-1}$]			**JS0SW**	
JS0SWG	[$A\,m^{-1}$]			0	**CODIO**=1
JS0SWGD	[$A\,m^{-1}$]			**JS0SWG**	**CODIO**=1
JS0SWGS	[$A\,m^{-1}$]			**JS0SWG**	**CODIO**=1
NJ	[—]			1.0	
NJD	[—]			**NJ**	
NJS	[—]			**NJ**	
NJSW	[—]			1.0	
NJSWD	[—]			**NJSW**	
NJSWS	[—]			**NJSW**	
NJSWG	[—]			1.0	

Parameter	Unit	Min	Max	Default	Remarks
NJSWGD	[—]			**NJSWG**	
NJSWGS	[—]			**NJSWG**	
XTI	[—]			2.0	
XTID	[—]			**XTI**	
XTIS	[—]			**XTI**	
XTI2	[—]			0	
XTI2D	[—]			**XTI**	
XTI2S	[—]			**XTI**	
DIVX	[V^{-1}]			0	
DIVXD	[V^{-1}]			**DIVX**	
DIVXS	[V^{-1}]			**DIVX**	
CTEMP	[—]			0	
CISB	[—]			0	
CISBD	[—]			**CISB**	
CISBS	[—]			**CISB**	
CISBK	[A]			0	
CISBKD	[A]			**CISBK**	
CISBKS	[A]			**CISBK**	
CVB	[—]	-0.1	0.2	0	
CVBD	[—]	-0.1	0.2	**CVB**	
CVBS	[—]	-0.1	0.2	**CVB**	
CJ	[$F\,m^{-2}$]			$5{\times}10^{-4}$	
CJD	[$F\,m^{-2}$]			**CJ**	
CJS	[$F\,m^{-2}$]			**CJ**	
CJSW	[$F\,m^{-1}$]			$5{\times}10^{-10}$	
CJSWD	[$F\,m^{-1}$]			**CJSW**	
CJSWS	[$F\,m^{-1}$]			**CJSW**	
CJSWG	[$F\,m^{-1}$]			$5{\times}10^{-10}$	
CJSWGD	[$F\,m^{-1}$]			**CJSWG**	
CJSWGS	[$F\,m^{-1}$]			**CJSWG**	
MJ	[—]			0.5	
MJD	[—]			**MJ**	
MJS	[—]			**MJ**	
MJSW	[—]			0.33	
MJSWD	[—]			**MJSW**	
MJSWS	[—]			**MJSW**	
MJSWG	[—]			0.33	
MJSWGD	[—]			**MJSWG**	
MJSWGS	[—]			**MJSWG**	
PB	[V]			1.0	
PBD	[V]			**PB**	
PBS	[V]			**PB**	
PBSW	[V]			1.0	
PBSWD	[V]			**PBSW**	
PBSWS	[V]			**PBSW**	
PBSWG	[V]			1.0	
PBSWGD	[V]			**PBSWG**	
PBSWGS	[V]			**PBSWG**	
VDIFFJ	[V]			$0.6{\times}10^{-3}$	
VDIFFJD	[V]			**VDIFFJ**	
VDIFFJS	[V]			**VDIFFJ**	
TCJBD	[K^{-1}]			0	
TCJBDSW	[K^{-1}]			0	
TCJBDSWG	[K^{-1}]			0	
TCJBS	[K^{-1}]			0	

Parameter	Unit	Min	Max	Default	Remarks
TCJBSSW	[K^{-1}]			0	
TCJBSSWG	[K^{-1}]			0	
HBDA				0.0	
HBDB				0.0	
HBDC				100.0	
HBDF				1.0	
HBDCTMP				0.0	
SUB1SNP	[1/V]			**SUB1**	**COSNP**=1
SUB2SNP	[V]			0.6 × **SUB2**	**COSNP**=1
SVDSSNP	[—]			**SVDS**	**COSNP**=1
NFALP	[cm s]			1×10^{-19}	
NFTRP	[V^{-1}]			1×10^{10}	
∗**CIT**	[$F\,cm^{-2}$]			0	
FALPH	[sm^3]			1.0	
DLY1	[s]			100×10^{-12}	
DLY2	[m^2]			0.7	
DLY3	[Ωm^2]			0.8×10^{-6}	
DLYOV	[1/A]			0.8×10^{-4}	
XQY	[m]	10n	50n	0	
XQY1	[$F\cdot\mu m^{\mathbf{XQY2}-1}$]	0		0	
XQY2	[—]	0		2	
OVSLP	[mV^{-1}]			2.1×10^{-7}	
OVMAG	[V]			0.6	
CGSO	[$F\,m^{-1}$]	0	100nm $\times C_{ox}$		to be set by user
CGDO	[$F\,m^{-1}$]	0	100nm $\times C_{ox}$		to be set by user
CGBO	[$F\,m^{-1}$]	0		0	
RS	[Ωm]	0	0.01	0	
RD	[Ωm]	0	0.1	0	
RSH	[$V\,A^{-1}$square]	0	500	0	
RSHG	[$V\,A^{-1}$square]	0	100	0	
GBMIN	[—]			1×10^{-12}	for circuit simulation
GDSLEAK	[—]			0	for circuit simulation
RBPB	[Ω]			50	
RBPD	[Ω]			50	
RBPS	[Ω]			50	
RTH0	[Kcm/W]	0	10	0.1	
RTHTEMP1	[m/W]	-1	1	0	
RTHTEMP2	[m/W/K]	-1	1	0	
CTH0	[Ws/(Kcm)]			1×10^{-7}	
RTH0L	[—]	-100	100	0	
RTH0LP	[—]	-10	10	1	
RTH0W	[—]	-100	100	0	
RTH0WP	[—]	-10	10	1	
RTH0NF	[—]	-5	5	0	
POWRAT	[—]	0	1.0	1.0	
PRATTEMP1	[1/K]	-1	1	0	
PRATTEMP2	[$1/K^2$]	-1	1	0	
SHEMAX	[K]	300	900	500	
SHEMAXDLT	[—]	0		0.1	
XLDLD	[m]	0		1×10^{-6}	reset to **XLDLD** ≥ 0
LOVERLD	[m]	0		1.0×10^{-6}	

Parameter	Unit	Min	Max	Default	Remarks
LOVERS	[m]	0		30n	
LOVER	[m]	0		30n	
NOVER	[cm^{-3}]			3×10^{16}	
NOVERS	[cm^{-3}]			1.0×10^{17}	
VFBOVER	[V]	-1.2	1	0.5	
QOVADD	[F/m^2]			0	
QOVJUNC	[—]	-1	50	0	
CVDSOVER	[—]	0	1.0	0	(**COTRENCH**=0)
LDRIFT1	[m]	0		1.0×10^{-6}	
LDRIFT2	[m]	0		1.0×10^{-6}	
WTRENCH	[m]	0		0.2×10^{-6}	(**COTRENCH**=1)
OLMDLT	[—]	0	100	5	(**COTRENCH**=1)
CORDRIFT=1					
RDRDL1	[m]			0	
RDRDL2	[m]			0	
RDRCX	[—]	0	1	0	reset within the range
RDRCAR	[mV^{-1}]	0	50n	100n	
RDRDJUNC	[m]			1.0×10^{-6}	
RDRBB	[—]			1.0	
RDRBBS	[—]			1.0	
RDRMUE	[$cm^2(V\cdot s)^{-1}$]	100	3000	1000	
RDRMUES	[$cm^2(V\cdot s)^{-1}$]	100	3000	1000	
RDRMUEL	[—]			0	
RDRMUELP	[—]			1	
RDRBBTMP	[1/K]			0	
RDRMUETMP	[—]	0.0	2.0	0	
RDRVMAX	[cm s^{-1}]	1MEG	100MEG	30MEG	
RDRVMAXS	[cm s^{-1}]	1MEG	100MEG	30MEG	
RDRVMAXL	[—]			0	
RDRVMAXLP	[—]			1	
RDRVMAXW	[—]			0	
RDRVMAXWP	[—]			1	
RDRVTMP	[—]	-2.0	1.0	0	
RDRQOVER	[1/cm]	0	1×10^7	1×10^5	
CORDRIFT=0					
RDVG11	[]	0	$V_{\mathrm{ds,max}}/30$	0	**CORSRD**=1,3
RDVG12	[V^{-1}]	0	$V_{\mathrm{ds,max}}$	100	**CORSRD**=1,3
RDVD	[Ωcm/V]	0	2.0	7.0×10^{-2}	**CORSRD**=1,3
RDVB	[V^{-1}]	0	2.0	0	**CORSRD**=1,3
RDS	[$\mu m^{\mathbf{RDSP}}$]	-100	100	0	**CORSRD**=1,3
RDSP	[—]	-10	10	1	**CORSRD**=1,3
RDVDL	[$\mu m^{-\mathbf{RDVDLP}}$]	-100	100	0	**CORSRD**=1,3
RDVDLP	[—]	-10	10	1	**CORSRD**=1,3
RDVDS	[$\mu m^{\mathbf{RDVDSP}}$]	-100	100	0	**CORSRD**=1,3
RDVDSP	[—]	-10	10	1	**CORSRD**=1,3
RD20	[—]	0	30	0	**CORSRD**=2,3
RD21	[—]	0	1.0	1.0	**CORSRD**=2,3
RD22	[$\Omega\ m/V^{\mathbf{RD22D+1}}$]	-5.0	0	0	**CORSRD**=2,3
RD22D	[—]	0	2.0	0	**CORSRD**=2,3
RD23	[$\Omega\ m/V^{\mathbf{RD21}}$]	0	2.0	0.005	**CORSRD**=2,3
RD23L	[$\mu m^{-\mathbf{RD23LP}}$]	-100	100	0	**CORSRD**=2,3
RD23LP	[—]	-10	10	1	**CORSRD**=2,3
RD23S	[$\mu m^{\mathbf{RD23SP+1}}$]	-100	100	0	**CORSRD**=2,3
RD23SP	[—]	-10	10	1	**CORSRD**=2,3

Parameter	Unit	Min	Max	Default	Remarks
RD24	[Ωm/V$^{\mathbf{RD21}+1}$]	0	0.1	0	**CORSRD**=2,3
RD25	[V]	0	$V_{\mathrm{gs,max}}$	0	**CORSRD**=2,3
RDOV11	[—]	0	10	0	**CORSRD**=1,3
RDOV12	[—]	0	2	1.0	**CORSRD**=1,3
RDOV13	[—]	0	1.0	1.0	**CORSRD**=1,3
RDSLP1	[—]	-10	10	0	**CORSRD**=1,3
RDICT1	[—]	-10	10	1.0	**CORSRD**=1,3
RDSLP2	[—]	-10	10	1	**CORSRD**=1,3
RDICT2	[—]	-10	10	0	**CORSRD**=1,3
RDTEMP1	[Ωcm/K]	-0.1	2	0	
RDTEMP2	[Ωcm/K^2]	-1.0×10^{-3}	1.0×10^{-3}	0	
RDVDTEMP1	[Ωcm V^{-1} K^{-1}]	-0.1	1.0	0	
RDVDTEMP2	[Ωcm V^{-1} K^{-2}]	-1.0×10^{-3}	1.0×10^{-3}	0	
RDVDSUB	[—]			0.3	
RDVSUB	[—]			1.0	
VBISUB	[—]			0.7	
Depletion mode					
	CODEP=1,2,3				
NDEPM	[cm^{-3}]	5×10^{15}	1×10^{18}	1×10^{17}	(**CODEP**=1,2)
				4×10^{16}	(**CODEP**=3)
NDEPML	[—]			0	
NDEPMLP	[—]			1	
TNDEP	[m]	10n	100n	200n	(**CODEP**=1,2)
				300n	(**CODEP**=3)
DEPMUE0	[cm^{2}V^{-1}s^{-1}]	1	1e5	1000	(**CODEP**=1,2)
		1	1e10	1×10^8	(**CODEP**=3)
DEPMUE0L	[—]			0	
DEPMUE0LP	[—]			1	
DEPMUE1	[cm^{2}V^{-1}s^{-1}]			0	(**CODEP**=1,2)
				100	(**CODEP**=3)
DEPMUE1L	[—]			0	
DEPMUE1LP	[—]			1	
DEPMUEPH0	[—]			0.3	(**CODEP**=1,2)
				0	(**CODEP**=3)
DEPMUEPH1	[cm^{2}V^{-1}s^{-1}]	1	1e5	5×10^3	(**CODEP**=1,2)
		100	2e9	400	(**CODEP**=3)
DEPVMAX	[cm/s]			3×10^7	(**CODEP**=1,2)
				1×10^7	(**CODEP**=3)
DEPVMAXL	[—]			0	
DEPVMAXLP	[—]			1	
DEPBB	[—]	0.01		1	(**CODEP**=1,2)
				2	(**CODEP**=3)
DEPMUETMP	[—]			1.5	
DEPVTMP	[—]			0.0	
DEPLEAK	[V]	0	5	0.5	(**CODEP**=1,2)
		0	5	0.1	(**CODEP**=3)
DEPLEAKL	[—]			0	
DEPLEAKLP	[—]			1	
	CODEP=3				
DEPDVFBC	[V]			0.1	**CODEP**=3
DEPRBR	[—]	0	1	1	**CODEP**=3
DEPJLEAK	[A/m^2]	0		0	**CODEP**=3
DEPWLP	[—]			0	**CODEP**=3
DEPNINVDC	[1/V]			100	**CODEP**=3
DEPNINVDH	[1/V]			10	**CODEP**=3

Parameter	Unit	Min	Max	Default	Remarks
DEPNINVDL	[—]			0	**CODEP**=3
DEPNINVDLP	[—]			0	**CODEP**=3
DEPNINVDW	[—]			0	**CODEP**=3
DEPNINVDWP	[—]			0	**CODEP**=3
DEPNINVDT1	[—]			0	**CODEP**=3
DEPNINVDT2	[—]			0	**CODEP**=3
DEPCAR	[m/V]			0	**CODEP**=3
DEPRDRDL1	[m]			0.0	**CODEP**=3
DEPRDRDL2	[m]			0.0	**CODEP**=3
DEPSUBSL0	[—]	10n		**DEPSUBSL**	**CODEP**=3
DEPQF	[V]	10n	8	0.01	**CODEP**=3
DEPQFRES	[V]	10n	8	0.05	**CODEP**=3
DEPFDPD	[V]	10n	4	0.2	**CODEP**=3
DEPPS	[V]			0.01	**CODEP**=3
DEPVSATA	[V]			0.0	**CODEP**=3
	****CODEP**=2,3**				
TNDEPV	[V^{-1}]			0.0	
DEPMUE2	[$cm^2V^{-1}s^{-1}$]	0		10^3	
DEPDDLT	[—]			3.0	(**CODEP**=2)
				1.0	(**CODEP**=3)
DEPSUBSL	[—]	10n		2.0	
DEPMUE0TMP	[—]			0.0	
DEPVGPSL	[V]	0		0.0	(**CODEP**=2)
				0.2	(**CODEP**=3)
	** **CODEP**=2**				
DEPVFBC	[V]			-0.2	**CODEP**=2
DEPMUEA1	[—]			0.0	**CODEP**=2
DEPVSATR	[—]			0	**CODEP**=2
DEPMUE2TMP	[—]			0.0	**CODEP**=2
	****CODEP**=1,2**				
DEPVDSEF1	[V]			2.0	**CODEP**=1,2
DEPVDSEF1L	[—]			0	**CODEP**=1,2
DEPVDSEF1LP	[—]			1	**CODEP**=1,2
DEPVDSEF2	[—]	0.1	4.0	0.5	**CODEP**=1,2
DEPVDSEF2L	[—]			0	**CODEP**=1,2
DEPVDSEF2LP	[—]			1	**CODEP**=1,2
	****CODEP**=1**				
DEPETA	[V^{-1}]			0	**CODEP**=1
DEPMUEBACK0	[$cm^2V^{-1}s^{-1}$]	1	1e5	100	**CODEP**=1
DEPMUEBACK0L	[—]			0	**CODEP**=1
DEPMUEBACK0LP	[—]			1	**CODEP**=1
DEPMUEBACK1	[$cm^2V^{-1}s^{-1}$]			0	**CODEP**=1
DEPMUEBACK1L	[—]			0	**CODEP**=1
DEPMUEBACK1LP	[—]			1	**CODEP**=1
Aging model parameter					
DEGTIME	[s]			0.0	**CODEG**=1
TRAPTAUCAP	[s]			10^{-6}	**CODEG**=1
TRAPLX	[V]			1	**CODEG**=1
TRAPGC1	[$cm^{-3}eV^{-1}$]			10^{15}	**CODEG**=1
TRAPGC1MAX	[$cm^{-3}eV^{-1}$]			5×10^{19}	**CODEG**=1
TRAPGCTIME1	[s]			30	**CODEG**=1
TRAPGCTIME2	[s]			10^8	**CODEG**=1
TRAPGCLIM	[s]			10^{18}	**CODEG**=1
TRAPESLIM	[s]			5	**CODEG**=1
TRAPES1	[eV]			0.2	**CODEG**=1

Parameter	Unit	Min	Max	Default	Remarks
TRAPES1MAX	[eV]			1	**CODEG**=1
TRAPESTIME1	[s]			100	**CODEG**=1
TRAPESTIME2	[s]			10^8	**CODEG**=1
TRAPGC2	[$cm^{-3}eV^{-1}$]			5×10^{13}	**CODEG**=1
TRAPES2	[eV]			0.03	**CODEG**=1
TRAPTEMP1	[1/K]			0	**CODEG**=1
TRAPTEMP2	[$1/K^2$]			0	**CODEG**=1
TRAPN	[—]			1.0	**CODEG**=1
TRAPP	[—]			1.0	**CODEG**=1
					Drift region
TRAPD1MAX	[$cm^{-3}eV^{-1}$]			30	**CODEG**=1
TRAPDTIME1	[s]			1000	**CODEG**=1
TRAPDTIME2	[s]			2×10^{10}	**CODEG**=1
TRAPDLX	[—]			1	**CODEG**=1
TRAPDVDDP	[—]			0	

31 Overview of the Parameter-Extraction Procedure

31.1 General MOSFET Part

In HiSIM, device characteristics are strongly dependent on basic device parameter values, such as the impurity concentration and the oxide thickness. Therefore, the parameter-value extraction has to be repeated with measured characteristics of different devices in a specific sequence until extracted parameter values reproduce all device characteristics consistently and reliably. To achieve reliable results, it is recommended to start with initial parameter values according to the recommendations listed in the table below. Since some of the model parameters such as $T_{\rm ox}$ are difficult to extract, they are expected to be determined directly by dedicated measurements. Threshold voltage measurements allow to derive a rough extraction for the model parameters referred to as "basic device parameters". The parameters identified with the symbol "*" in the Model Parameter Table are initially fixed to zero.

Determined by dedicated measurements (not changed during extraction procedure) are used	Default values listed in the section 30 initially for the groups of parameters listed below
TOX	basic device parameters (not listed on left side) gate leakage GIDL source/bulk and drain/bulk diodes noise subthreshold swing non-quasi-static model overlap capacitances

The sequence of device selection for the parameter extraction is recommended in 4 steps

1. Long-Channel Devices
2. Short-Channel Devices
3. Long-Narrow Devices
4. Short-Narrow Devices

Prior to the extracttion, a rough extraction with measured $V_{\rm th} - L_{\rm gate}$ characteristics is recommended to get rough idea about parameter values. These parameters are usually important giving strong influence on accuracy of the total parameter extraction. The parameter extraction of the general MOSFET part is summarized in the following Table.

31.2 HiSIM_HV Specific Part

Model parameters are categorized into two parts: (1) general MOSFET related parameters and (2) the HiSIM_HV specific parameters. The HiSIM_HV specific model parameters are extracted after the extraction of the intrinsic MOSFET part. Recommended extraction procedure is to perform first (1) and then (2). Thus the parameter extraction is done in the following sequence:

1. rougth extraction of the MOSFET parameters with measured $V_{\rm th} - L_{\rm gate}$
2. fine extraction with measured subthreshold in $I_{\rm ds} - V_{\rm gs}$
3. extraction of mobility parameters with $I_{\rm ds} - V_{\rm gs}$ and $I_{\rm ds} - V_{\rm ds}$

Table 32: Summary of the 7 steps of HiSIM's Parameter Extraction Procedure.

Step	Description	Parameters
Step 1: Initial preparation and rough extraction		
1-1.	Initialize all parameters to their default values	
1-2.	Use the measured gate-oxide thickness for TOX	TOX
1-3.	Rough extraction with V_{th}-dependence on L_{gate} $[V_{\mathrm{th}} - V_{\mathrm{gs}}]$	**NSUBC**, **VFB**, **SC1**, **SC2**, **SC3**, **NSUBP**, **LP**, **SCP1**, **SCP2**, **SCP3**, **NPEXT**, **LPEXT**
1-4.	Quantum and poly-depletion effects $[C_{\mathrm{gg}} - V_{\mathrm{gs}}]$	**QME1**, **QME2**, **QME3**, **PGD1**, **PGD2**
Step 2: Extraction with long and wide transistors		
2-1.	Fitting of sub-threshold characteristics $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**NSUBC**, **VFB**, **MUECB0**, **MUECB1**
2-2.	Determination of mobility parameters for low V_{ds} $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**MUEPH0**, **MUEPH1**, **MUESR0**, **MUESR1**
2-3.	Determination of mobility parameters for high V_{ds} $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**NINV**, **NDEP**
Step 3: Extraction with medium/short length and large width transistors		
3-1.	Pocket-parameter extraction with medium length transistors $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**NSUBP**, **LP**, **SCP1**, **SCP2**, **SCP3**, **NPEXT**, **LPEXT**
3-2.	Short-channel-parameter extraction with short-length transistors $[V_{\mathrm{th}} - L_{\mathrm{gate}}]$	**SC1**, **SC2**, **SC3**, **PARL2**, **XLD**
3-3.	Mobility-parameter refinement for low V_{d} $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**MUEPHL**, **MUEPLP**, **MUESRL**, **MUESLP**
3-4.	Velocity parameter extraction for high V_{d} $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**VMAX**, **VOVER**, **VOVERP**
3-5.	Parameters for channel-length modulation $[I_{\mathrm{ds}} - V_{\mathrm{ds}}]$	**CLM1**, **CLM2**, **CLM3**
3-6.	Source/drain resistances $[I_{\mathrm{ds}} - V_{\mathrm{ds}}]$	**RS**, **RD**, **RSH**, **NRS**, **NRD**
Step 4: Extraction of the width dependencies for long transistors		
4-1.	Fitting of sub-threshold width dependencies $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**NSUBC**, **NSUBCW**, **NSUBCWP**, **WFC**, **XWD**, **WVTH0**
4-2.	Fitting of mobility width dependencies $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**MUEPHW**, **MUEPWP**, **MUESRW**, **MUESWP**
Step 5: Extraction of the width dependencies for short transistors		
5-1.	Fitting of sub-threshold dependencies $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**NSUBP0**, **NSUBWP**
Step 6: Extraction of small-geometry effects		
6-1.	Effective channel-length corrections	**WL2**, **WL2P**
6-2.	Mobility and velocity $[I_{\mathrm{ds}} - V_{\mathrm{ds}}]$	**MUEPHS**, **MUEPSP**, **VOVERS**, **VOVERSP**
Step 7: Extraction of temperature dependence with long-channel transistors		
7-1.	Sub-threshold dependencies $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**BGTMP1**, **BGTMP2**, **EG0**
7-2.	Mobility and maximum carrier-velocity dependencies $[I_{\mathrm{ds}} - V_{\mathrm{gs}}]$	**MUETMP**, **VTMP**

4. extraction of resistance parameters with $I_{\mathrm{ds}} - V_{\mathrm{gs}}$ and $I_{\mathrm{ds}} - V_{\mathrm{ds}}$
5. fine extraction of resistance with channel-conductance and trans-conductance
6. capacitacne extraction

Agreement of the extraction results after the 3rd step is not sufficient especially in high V_{gs} region and low V_{ds} region. The 4th resistance-extraction step is focused on the resion where the quasi-saturation effect is obvious. It is recommended to repeat the extraction steps from 3rd to 5th to achieve better fitting. The steps from 1st to 3rd are the same as the conventional extraction procedure.
The extraction of the resistance parameters are done after the model selection as summarized in Fig. 29.

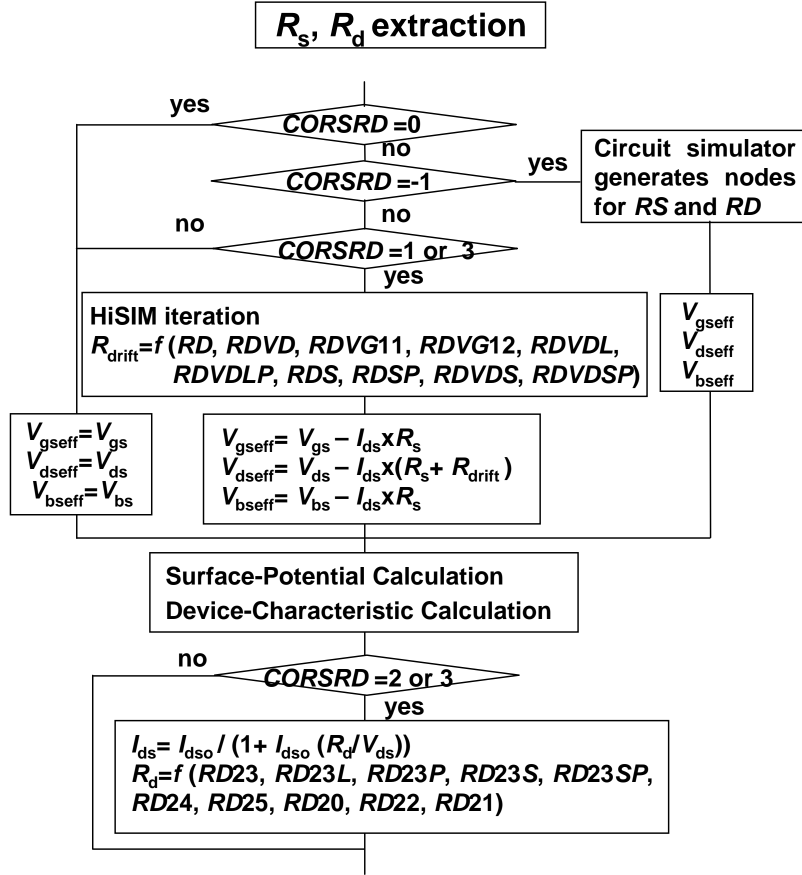

Fig. 29: Parameter extraction flow for resistance parameters. For the new resistance model (**CORDRIFT**=1) the flag **CORSRD** is no more valid but only one extraction procedure is followed, namely the "HiSIM iteration" part with the new model equations.

If the self-heating effect is activatied, all device characteristics are changed drastically. Retunning of model parameters are required. These model parameters are mostly related to the mobility and resistance models. The temperature dependent parameters are extracted without the self-heating effect with temperature dependent measurements. These values are usually not necessary to be modified after activating the self-heating effect.

References

[1] M. Miura-Mattausch, H. J. Mattausch, and T. Ezaki, "The Physics and Modeling of MOSFETs," *World Scientific*, 2008.

[2] H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors," *Solid-State Electron.*, vol. 9, pp. 927–937, Oct. 1966.

[3] H. J. Mattausch, M. Miyake, T. Iizuka, H. Kikuchihara, M. Miura-Mattausch, "The Second-Generation of HiSIM_HV Compact Models for High-Voltage MOSFETs," IEEE Trans. Electron Devices, vol. 60, no. 2, pp. 653-661, Feb. 2013.

[4] M. Yokomichi, N. Sadachika, M. Miyake, T. Kajiwara, H. J. Mattausch, and M. Miura-Mattausch, "Laterally diffused metal oxide semiconductor model for device and circuit optimization," *Jpn. J. Appl. Phys.*, vol. 47, pp. 2560–2563, April 2008.

[5] Y. Oritsuki, M. Yokomichi, T. Sadachika, M. Miyake, T. Kajiwara, H. Kikuchihara, T. Yoshida, U. Feldmann, H. J. Mattausch, and M. Miura-Mattausch, "HiSIM-LDMOS/HV: A complete surface-potential-based MOSFET model for high voltage applications," *Proc. NSTI-Nanotech*, pp. 893–896, Boston, June, 2008.

[6] U. Feldmann, M. Miyake, T. Kajiwara, and M. Miura-Mattausch"On local handling of inner equations in compact models," Scientific Computing in Electrical Engineering, Helsinki, pp. 143–150,Sept. 2008.

[7] M. Miura-Mattausch, U. Feldmann, A. Rahm, M. Bollu, and D. Savignac, "Unified complete MOSFET model for analysis of digital and analog circuits," *IEEE Trans. CAD/ICAS*, vol. 15, pp. 1–7, Jan. 1996.

[8] S.-Y. Oh, D. E. Ward, and R. W. Dutton, "Transient Analysis of MOS Transistors," *IEEE J. Solid-State Circ.*, vol. SC–15, pp. 636–643, Aug. 1980.

[9] Y. P. Tsividis, "Operation and Modeling of the MOS Transistor," *McGraw-Hill*, 1999.

[10] J. R. Brews, "A charge-sheet model of the MOSFET," *Solid-State Electron.*, vol. 21, pp. 345–355, Feb. 1978.

[11] M. Miura-Mattausch and H. Jacobs, "Analytical model for circuit simulation with quarter micron metal oxide semiconductor field effect transistors: Subthreshold characteristics," *Jpn. J. Appl. Phys.*, vol. 29, pp. L2279–L2282, Dec. 1990.

[12] C. T. Sah, "Characteristics of the metal-oxide-semiconductor transistors," *IEEE Electron Devices*, vol. ED-11, pp. 324–345, 1964.

[13] P. M. Rousseau, S. W. Crowder, P. B. Griffin, and J. D. Plummer, "Arsenic deactivation enhanced diffusion and the reverse short-channel effect," *IEEE Electron Device Lett.*, vol. 18, pp. 42–44, 1997.

[14] M. Suetake, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, N. Shigyo, S. Odanaka, and N. Nakayama, "Precise physical modeling of the reverse-short-channel effect for circuit simulation," in *Proc. SISPAD*, pp. 207–210, Sep. 1999.

[15] M. Miura-Mattausch, M. Suetake, H. J. Mattausch, S. Kumashiro, N. Shigyo, S. Odanaka, and N. Nakayama, "Physical modeling of the reverse-short-channel effect for circuit simulation," *IEEE Electron Devices*, vol. 48, pp. 2449-2452, Oct., 2001.

[16] S. Kumashiro, H. Sakamoto, and K. Takeuchi, "Modeling of channel boron distribution deep sub-0.1μm n-MOSFETs," *IEICE Trans. Electro.*, vol. E82-C, June 1999.

[17] D. Buss, "Device issues in the integration of analog/RF functions in deep submicron digital CMOS," *Tech. Digest IEDM*, pp. 423–426, 1999.

[18] D. Kitamaru, H. Ueno, K. Morikawa, M. Tanaka, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "$V_{\rm th}$ model of pocket-implanted MOSFETs for circuit simulation," *Proc. SISPAD*, pp. 392–395, 2001.

[19] H. Ueno, D. Kitamaru, K. Morikawa, M. Tanaka, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Impurity-Profile-Based Threshold-Voltage Model of Pocket-Implanted MOSFETs for Circuit Simulation," *IEEE Electron Devices*, vol. 49, pp. 1783–1789, Oct 2002.

[20] M. Suetake, K. Suematsu, H. Nagakura, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, S. Odanaka, and N. Nakayama, "HiSIM: A drift-diffusion-based advanced MOSFET model for circuit simulation with easy parameter extraction," *Proc. SISPAD*, pp. 261–264, 2000.

[21] F. Stern and W. E. Howard, "Properties of semiconductor surface inversion layers in the electric quantum limit," *Phys. Rev.*, vol. 163, No. 3, pp. 816–835, 1967.

[22] Z. Yu, R. W. Dutton, and R. A. Kiehl, "Circuit device modeling at the quantum level," *Proc. IWCE-6*, pp. 222–229, 1998.

[23] T. Ando, A. B. Fowler, and F. Stern, "Electronic properties of two-dimensional systems," *Rev. Modern Phys.*, vol. 54, pp. 437–621, 1982.

[24] Y. Matsumoto and Y. Uemura, "Scattering mechanism and low temperature mobility of MOS inversion layers," *Jpn. J. Appl. Phys. Suppl.*, vol. 2, Pt 2, pp. 367–370, 1974.

[25] S. Takagi, M. Iwase, and A. Toriumi, "On the universality of inversion-layer mobility in n- and p-channel MOSFETs," *Tech. Digest IEDM*, pp. 398–401, 1988.

[26] S. Matsumoto, K. Hisamitsu, M. Tanaka, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, S. Odanaka, and N. Nakayama, "Validity of the Mobility Universality for Scaled Metal-Oxide-Semiconductor Field-Effect Transistors down to 100nm Gate Length," *J. Appl. Phys.*, vol. 92, pp. 5228–5232, 2002.

[27] D. M. Caughey and R. E. Thomas, "Carrier mobilities in Silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, pp. 2192–2193, 1967.

[28] K. Joardar, K. K. Gullapalli, C. C. McAndrew, M. E. Burnham, and A. Wild, "An improved MOSFET model for circuit simulation," *IEEE Trans. Electron Devices*, vol. 45, pp. 134–148, Jan. 1998.

[29] Y. A. El-Mansy and A. R. Boothroyd, "A simple two-dimensional model of IGFET operation in the saturation region," *IEEE Trans. Electron Devices*, vol. ED-24, pp. 241–253, 1977.

[30] D. Navarro, T. Mizoguchi, M. Suetake, K. Hisamitsu, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "A compact model of the pinch-off region of 100nm MOSFETs based on the surface potential," *IEICE Trans. Electron.*, vol. E88-C, No. 5, pp. 1079-1086, 2005.

[31] G. Scott, J. Lutze, M. Rubin, F. Nouri, and M. Manley, "NMOS drive current reduction caused by transistor layout and trench isolation induced stress," *Tech. Digest IEDM*, pp. 827–830, 1999.

[32] M. Miura-Mattausch, "Analytical MOSFET model for quarter micron technologies," *IEEE Trans. CAD/ICAS*, vol. 13, pp. 610–615, 1994.

[33] F. H. Gaensslen and R. C. Jaeger, "Temperature dependent threshold behavior of depletion mode MOSFETs." *Solid-State Electron.*, vol. 22, pp. 423–430, 1979.

[34] *BSIM4.0.0 MOSFET Model, User's Manual*, Department of Electrical Engineering and Computer Science, University of California, Berkeley CA, 2000.

[35] D. Navarro, K. Hisamitsu, T. Yamaoka, M. Tanaka, H. Kawano, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Circuit-Simulation Model of Gate-Drain- Capacitance Changes in Small-Size MOSFETs Due to High Channel-Field Gradients," Proc. SISPAD, pp. 51-52, 2002.

[36] B. J. Sheu and P.-K. Ko, "Measurement and modeling of short-channel MOS transistor gate capacitances," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 464–472, 1987.

[37] R. Shrivastava and K. Fitzpatrik, "A simple model for the overlap capacitance of a VLSI MOS device," *Proc. IEEE*, vol. ED-29, pp. 1870–1875, 1982.

[38] N. Arora, "MOSFET models for VLSI circuit simulation: theory and practice," *Springer-Verlag*, 1993.

[39] E. O. Kane, "Zener Tunneling in Semiconductors," *J. Phys. Chem. Solids*, vol. 12, pp. 181–188, 1959.

[40] Q. Ngo, D. Navarro, T. Mizoguchi, S. Hosokawa, H. Ueno, M. Miura-Mattausch, and C. Y. Yang, "Gate Current Partitioning in MOSFET Models for Circuit Simulation," *Proc. Modeling and Simulation of Microsystems*, vol. 1.2, pp. 322–325, 2003.

[41] R. Inagaki, K. Konno, N. Sadachika, D. Navarro, K. Machida, Q. Ngo, C. Y. Yang, T. Ezaki, H. J. Mattausch, M. Miura-Mattausch, and Y. Inoue, "A Gate–Current Model for Advanced MOSFET Technologies Implemented into HiSIM2," *Proc. Int. 3rd Workshop on Compact Modeling*, Yokohama, Jan. 2006.

[42] T. Yoshida, M. Miura-Mattausch, H. Ueno, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Conservation of symmetry at $V_{\rm ds} = 0$ for reliable analog simulations," submitted for publication.

[43] *BSIM3, version3.0 manual*, Department of Electrical Engineering and Computer Science, University of California, Berkeley CA, 1996.

[44] S. Matsumoto, H. Ueno, S. Hosokawa, T. Kitamura, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "$1/f$ noise characteristics in 100nm-MOSFETs and its modeling for circuit simulation," *IEICE Trans. Electron.*, vol. E88-C, pp. 247–254, 2005.

[45] A. van der Ziel, "Noise in solid state devices and circuits," New York, John Wiley

[46] S. Hosokawa, Y. Shiraga, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, H. Masuda, and S. Miyamoto, "Origin of enhanced thermal noise for 100nm-MOSFETs," Ext. Abs. SSDM, pp. 20–22, 2003.

[47] S. Hosokawa, D. Navarro, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, and S. Miyamoto, "Gate-length and drain-voltage dependence of thermal drain noise in advanced metal-oxide-semiconductor field-effect transistors," Appl. Phys. Lett. 87, 092104, 2005.

[48] M. Miura-Mattausch, H. Ueno, H. J. Mattausch, K. Morikawa, S. Itoh, A. Kobayashi, and H. Masuda, "100nm-MOSFET model for circuit simulation: Challenges and solutions," *IEICE Trans. Electron.*, vol. E86-C, pp. 1009–1021, 2003.

[49] T. Warabino, M. Miyake, N. Sadachika, D. Navarro, Y. Takeda, G. Suzuki, T. Ezaki, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, and S. Miyamoto, "Analysis and compact modeling of MOSFET high-frequency noise,"Proc. SISPAD, pp. 158-161, 2006.

[50] N. Nakayama, D. Navarro, M. Tanaka, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, S. Kumashiro, M. Taguchi, and S. Miyamoto, "Non-quasi-static model for MOSFET based on carrier-transit delay," *Electronics Letters*, vol. 40, pp. 276–278, 2004.

[51] D. Navarro, N. Nakayama, K. Machida, Y. Takeda, H. Ueno, H. J. Mattausch, M. Miura-Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, T. Kage, and S. Miyamoto,"Modeling of carrier transport dynamics at GHz-frequencies for RF circuit simulation," Proc. SISPAD, pp. 259-262, 2004.

[52] D. Navarro, Y. Takeda, M. Miyake, N. Nakayama, K. Machida, T. Ezaki, H. J. Mattausch, M. Miura-Mattausch, "A carrier-tansit-delay-based non-quasi-static MOSFET model for circuit simulation and

its application to harmonic distortion analysis," IEEE T. Electron Devices, vol. 53, pp. 2025–2034, 2006.

[53] K. Machida, D. Navarro, M. Miyake, R. Inagaki, N. Sadachika, G. Suzuki, Y. Takeda, T. Ezaki, H. J. Mattausch, M. Miura-Mattausch, "Efficient NQS MOSFET Model for both Time-Domain and Frequency-Domain Analysis," Proc. SiRF, pp. 73-76, 2006.

[54] D. Navarro, Y. Takeda, M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, T. Kage, and S. Miyamoto,"On the validity of conventional MOSFET nonlinearity characterization at RF switching," IEEE Microwave and Wireless Components Lett., pp. 125-127, 2006.

[55] T. Kajiwara, M. Miyake, N. Sadachika, H. Kikuchihara, U. Feldmann, H. J. Mattausch, and M. Miura-Mattausch, "Spatial distribution analysis of self-heating effect in high-voltage MOSFETs," to be appeared in Proc. APEC, Feb. 2009.

[56] A. Tanaka, Y. Oritsuki, H. Kikuchihara, M. Miyake, H. J. Mattausch, M. Miura-Mattausch, Y. Liu and K. Green, "Quasi-2-dimensional compact resistor model for the drift region in high-voltage LDMOS devices," IEEE Trans. Electron Devices, vol. 58, no. 7, pp. 2072-2080, Jul. 2011.

[57] T. Iizuka, T. Sakuda, Y. Oritsuki, A. Tanaka, M. Miyake, H. Kikuchihara, U. Feldmann, H. J. Mattausch, M. Miura-Mattausch, "Compact Modeling of Expansion Effects in LDMOS," IEICE Trans. Electron., Vol. E95-C, No. 11, pp. 1817-1823, Nov. 2012.

[58] H. Tanoue, A. Tanaka, Y. Oodate, T. Nakahagi, C. Ma, M. Miyake, H. J. Mattausch, and M. Miura-Mattausch, "Universal Properties and Compact Modeling of Dynamic Hot-Electron Degradation in n-MOSFETs," IEEE Int. Reliability Phys. Symp., pp. CM 4.1, April 2013.

[59] T. Leroux, "Static and Dynamic Analysis of Amorphous-Silicon Field-Effect Transistors," Solid-State Electron., vol. 29, no. 1, pp. 47-58, Jan. 1986.

[60] S. Miyano, Y. Shimizu, T. Murakami, M. Miura-Mattausch and HiSIM Research Center, "A surface potential based Poly-Si TFT model for circuit simulation," Proc. SISPAD, pp. 373-376, September, 2008.

[61] C. Ma, H. J. Mattausch, K. Matsuzawa, S. Yamaguchi, T. Hoshida, M. Imade, R. Koh, T. Arakawa, and M. Miura-Mattausch, "Universal NBTI Compact Model for Circuit Aging Simulation under Any Stress Conditions," IEEE Trans. Semiconductor Manufacturing, vol. 14, no. 3, pp. 818-825, 2014.