HiSIM_HV 2.1.0 User's Manual

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1 LDMOS/HVMOS Structures

HiSIM (Hiroshima-university STARC IGFET Model) is the first complete surface-potential-based MOSFET model for circuit simulation based on the drift-diffusion theory [1], which was originally developed by Pao and Sah [2]. The model has been extended for power MOSFETs by considering the resistance effect explicitly, which is named HiSIM_HV.

There are two types of structures commonly used for high voltage applications. One is the asymmetrical laterally diffused structure called LDMOS and the other is originally the symmetrical structure, which we distinguish by referring to it as HVMOS. However, the asymmetrical HVMOS structure is also possible. HiSIM_HV is valid for modeling all these structure types [3, 4].

The most important features of LDMOS/HVMOS devices, different from the conventional MOSFET, are originating from the drift region introduced to achieve the sustainability of high voltages. By varying the lengh as well as the dopant concentration of the drift region, various devices with various operating biase conditions are realized as shown in Fig. 1 for the LDMOS structure.

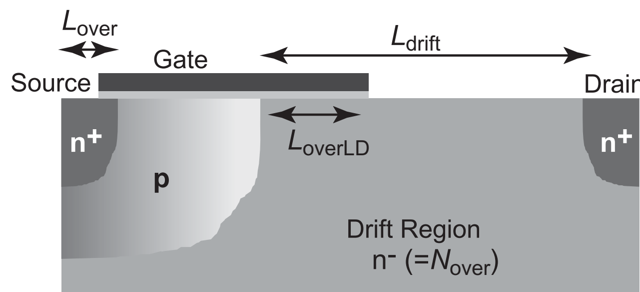

Fig. 1: Schematic of the typical LDMOS structure and device parameters.

A schmatic of the general structures for LDMOS and HVMOS are shown in Fig. 2 for the n-channel case. To make the structural definition easy, Flag **COSYM** is introduced as shown in Fig. 3. **COSYM**=0 refers to the asymmetrical LDMOS, and all structural parameters have to be determined independently. **COSYM**=1 refers to symmetrical/asymmetrical HVMOS. If parameter values of the source side are given, they are activated. If they are not given, parameter values of the drain side are copied to the source side automatically.

Table 1 summarizes the structural parameters to be determined. If the overlap length **LOVER** is determined instead of **LOVERS**, **LOVER** is taken for **LOVERS**. Model parameters for resistances at the source side and the drain side are distinguished by **RS** and **RD** for the asymmetrical HVMOS.

HiSIM_HV 1.2.0 includes the substrate node $V_{\rm sub}$ as schematically shown in Fig. 4, where model parameters **DDRIFT** and **NSUBSUB** are newly introduced for $D_{\rm drift}$ and $N_{\rm subsub}$, respectively. The node inclusion is done by selecting Flag **COSUBNODE**=0 as the 5th node.

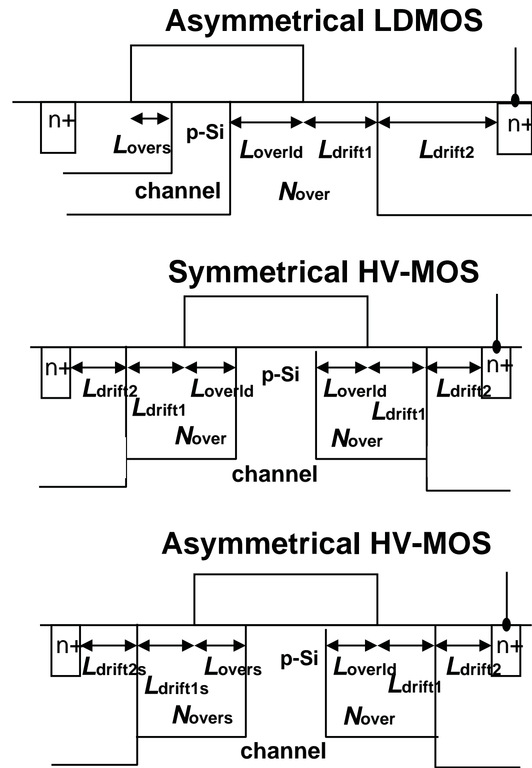

Fig. 2: Device parameters in HiSIM_HV.

The HiSIM_HV model parameters introduced in section 1 are summarized in Table 2.

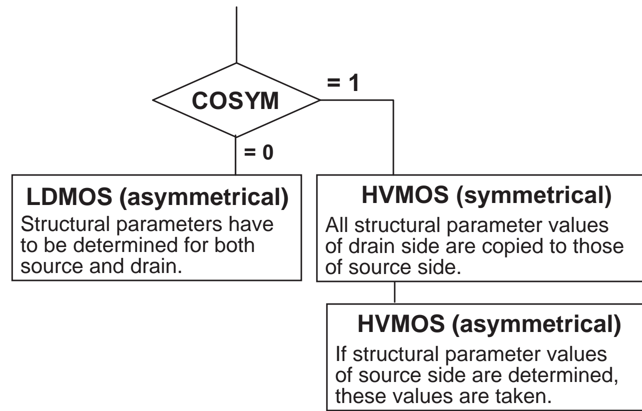

Fig. 3: Device parameters of HiSIM_HV.

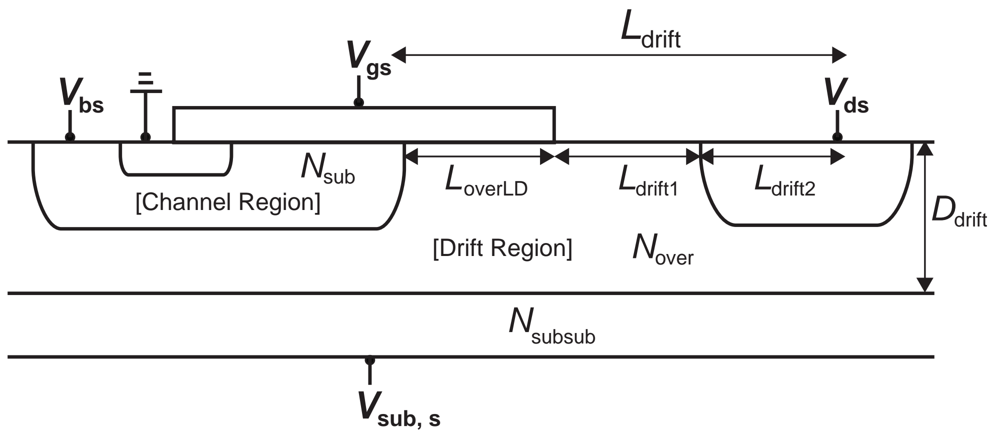

Fig. 4: Schematic of a LDMOS with the substrate node $V_{\mathrm{sub,s}}$.

Table 1: HiSIM_HV 1.2.0 model parameters introduced.

	structure	source	drain
COSYM=0	**LDMOS**	**LOVERS** **RS**	**LOVERLD** **LDRIFT1** **LDRIFT2** **NOVER** **RD**
COSYM=1	**symmetrical HVMOS**		**LOVERLD** **LDRIFT1** **LDRIFT2** **NOVER** **RD**
COSYM=1	**asymmetrical HVMOS**	**LOVERS** **LDRIFT1S** **LDRIFT2S** **NOVERS** **RS**	**LOVERLD** **LDRIFT1** **LDRIFT2** **NOVER** **RD**

Table 2: HiSIM_HV 1.2.0 model parameters introduced in section 1 of this manual.

Parameter	Description
LOVER	overlap length at source side for **LOVERS**
LOVERLD	overlap length at drain, and at source, if **COSYM**=1
LDRIFT1	length of lightly doped drift region at drain, and at source, if **COSYM**=1
LDRIFT2	length of heavily doped drift region at drain, and at source, if **COSYM**=1
NOVER	impurity concentration of **LOVERLD** at drain, and at source, if **COSYM**=1
LOVERS	overlap length at source
LDRIFT1S	length of lightly doped drift region at source, if **COSYM**=1 and the value is determined
LDRIFT2S	length of heavily doped drift region at source, if **COSYM**=1 and the value is determined
NOVERS	impurity concentration of **LOVERS** at source, if **COSYM**=1 and the value is determined
VBSMIN	minimum V_{bs} voltage applied: No need and inactivated.
DDRIFT	depth of the drift region
NSUBSUB	impurity concentration of the substrate required for V_{sub} dependence

2 Basic Concept

HiSIM_HV solves the potential distribution along the surface by solving the Poisson equation iteratively including the resistance effect in the drift region, where the bias dependence of the resistance is considered. The HiSIM compact model determines the complete potential distribution along the device including the surface potential at the source side ϕ_{S0}, the potential at the pinch-off point ϕ_{SL}, the potential at the channel/drain junction, $\phi_S(\Delta L)$, and the final potential value at the drain contact $\phi_{S0} + V_{ds}$ as shown in Fig. 5. The potential V_{dseff} is the potential value which mostly determines the device characteristics. This potential node is considered explicitly in addition to the node potential of V_{ds}. Advanced version concealing the internal node to speed up the simulation has been developed in parallel [5].

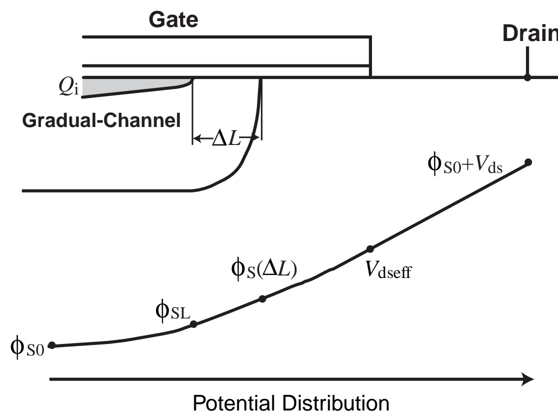

Fig. 5: Schematic of the surface potential distribution in the channel at the drain side of the LDMOS device structure.

3 Definition of Device Size

The effective channel length $L_{\rm eff}$ and width $W_{\rm eff}$ are calculated from the gate length $L_{\rm gate}$ and width $W_{\rm gate}$, where $L_{\rm gate}$ and width $W_{\rm gate}$ deviate from the gate drawn length and width

$$L_{\rm gate} = L_{\rm drawn} + \mathbf{XL} \quad (1)$$
$$W_{\rm gate} = \frac{W_{\rm drawn}}{\mathbf{NF}} + \mathbf{XW} \quad (2)$$

$$L_{\rm poly} = L_{\rm gate} - 2 \cdot \frac{\mathbf{LL}}{(L_{\rm gate} + \mathbf{LLD})^{\mathbf{LLN}}} \quad (3)$$
$$W_{\rm poly} = W_{\rm gate} - 2 \cdot \frac{\mathbf{WL}}{(W_{\rm gate} + \mathbf{WLD})^{\mathbf{WLN}}} \quad (4)$$

$$L_{\rm eff} = L_{\rm poly} - \mathbf{XLD} - \mathbf{XLDLD} \quad (5)$$
$$W_{\rm eff} = W_{\rm poly} - 2 \cdot \mathbf{XWD} \quad (6)$$
$$W_{\rm eff,LD} = W_{\rm poly} - 2 \cdot \mathbf{XWDLD} \quad (7)$$
$$W_{\rm effc} = W_{\rm poly} - 2 \cdot \mathbf{XWDC} \quad (8)$$
$$\quad (9)$$

where **XLD**/**XLDLD** and **XWD** account for the overlaps of source/drain contact and the gate oxide as shown in Fig. 6. Widening of $W_{\rm eff}$ due to the extension of electric-force line of the drift region is considered by **XWDLD**. The model parameter **XWDC** is introduced to describe the different width dependence of capacitacnes from currents. If the value is not given, the same value as **XWD** is taken. **LL**, **LLD**, **LLN**, **WL**, **WLD**, and **WLN** are further model parameters for including $L_{\rm gate}$ or $W_{\rm gate}$ dependencies on $L_{\rm eff}$ and $W_{\rm eff}$.

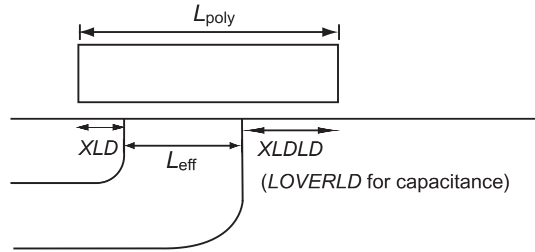

Fig. 6: Cross section of the device.

The HiSIM model parameters introduced in section 3 are summarized in Table 3.

Table 3: HiSIM model parameters introduced in section 3 of this manual. $*$ and # indicate minor parameters and # an instance parameter, respectively.

Parameter	Description
#NF	number of gate fingers
XL	difference between real and drawn gate length
XW	difference between real and drawn gate width
XLD	gate-overlap in length at source side
XLDLD	gate-overlap in length at drain side
XWD	gate-overlap in width
XWDLD	widening of drift width
XWDC	gate-overlap in width for capacitance calculation
LL	coefficient of gate length modification
LLD	coefficient of gate length modification
LLN	coefficient of gate length modification
WL	coefficient of gate width modification
WLD	coefficient of gate width modification
WLN	coefficient of gate width modification

4 Charges

By applying the Gauss law, the charge density induced in the channel is derived from the Poisson equation [6]:

$$
\begin{aligned}
-(Q_\mathrm{B}+Q_\mathrm{I}) &= C_\mathrm{ox}\big(V'_\mathrm{G}-\phi_\mathrm{S}(y)\big)\\
&= \sqrt{\frac{2\epsilon_\mathrm{Si}qN_\mathrm{sub}}{\beta}}\Big[\exp\big\{-\beta(\phi_\mathrm{S}(y)-V_\mathrm{bs})\big\}+\beta(\phi_\mathrm{S}(y)-V_\mathrm{bs})-1\\
&\quad+\frac{n_\mathrm{p0}}{p_\mathrm{p0}}\Big\{\exp\big(\beta(\phi_\mathrm{S}(y)-\phi_\mathrm{f}(y))\big)-\exp\big(\beta(V_\mathrm{bs}-\phi_\mathrm{f}(y))\big)\Big\}\Big]^{\frac{1}{2}}
\end{aligned}
$$

$$C_\mathrm{ox}=\frac{\epsilon_0\mathbf{KAPPA}}{\mathbf{TOX}} \tag{10}$$

$$V'_\mathrm{G}=V_\mathrm{gs}-\mathbf{VFBC}+\Delta V_\mathrm{th} \tag{11}$$

$$\beta=\frac{q}{kT} \tag{12}$$

where **VFBC** is the flat-band voltage, **TOX** is the physical gate-oxide thickness, and ΔV_th is the threshold voltage shift in comparison to the threshold voltage of a long-channel transistor [10]. ϵ_0 and **KAPPA** are permittivities in vacuum and in the gate dielectric, respectively. The electron charge is denoted by q, and ϵ_Si and N_sub are the silicon permittivity and the substrate impurity concentration, respectively. The Boltzmann constant and the lattice temperature in Kelvin are k and T, respectively. The quasi-Fermi potential $\phi_\mathrm{f}(y)$ preserves the following relationship:

$$\phi_\mathrm{f}(L_\mathrm{eff})-\phi_\mathrm{f}(0)=V_\mathrm{ds,mod} \tag{13}$$

where $V_\mathrm{ds,mod}$ is introduced to fit measured transition characteristics of the channel conductance g_ds between the linear region and the saturation region to compensate for insufficiencies of the charge-sheet approximation as

$$V_\mathrm{ds,mod}=\frac{V_\mathrm{ds}}{\left[1+\left(\frac{V_\mathrm{ds}}{V_\mathrm{ds,sat}}\right)^{\Delta}\right]^{\frac{1}{\Delta}}} \tag{14}$$

where

$$\Delta=\frac{\mathbf{DDLTMAX}\cdot T1}{\mathbf{DDLTMAX}+T1}+1 \tag{15}$$

$$T1=\mathbf{DDLTSLP}\cdot L_\mathrm{gate}\cdot 10^6+\mathbf{DDLTICT} \tag{16}$$

and $V_\mathrm{ds,sat}$ is calculated by solving the Poisson equation analytically by neglecting the inversion carrier density [1].

The electron concentration at equilibrium condition n_p0 is

$$n_\mathrm{p0}=\frac{n_\mathrm{i}^2}{p_\mathrm{p0}} \tag{17}$$

where the intrinsic carrier concentration $n_{\rm i}$ is

$$n_{\rm i} = n_{\rm i0} T^{\frac{3}{2}} \exp\left(-\frac{E_{\rm g}}{2q}\beta\right) \tag{18}$$

$p_{\rm p0}$ is approximated to be $N_{\rm sub}$, and $E_{\rm g}$ describes the temperature dependence of the bandgap (see section 14).

Analytical equations for $Q_{\rm B}$ and $Q_{\rm I}$ are derived as a function of $\phi_{\rm S0}$ and $\phi_{\rm SL}$. The final equations for $Q_{\rm B}$, $Q_{\rm I}$, and $Q_{\rm D}$ are given in Eqs. (19)- (21).

$$\begin{aligned}
Q_{\rm B} = &-\frac{\mu(W_{\rm eff}\cdot\mathbf{NF})^2}{I_{\rm ds}}\Bigg[const0\, C_{\rm ox}(V_{\rm G}-\mathbf{VFBC})\frac{1}{\beta}\frac{2}{3}\Big[\big\{\beta(\phi_{\rm S}-V_{\rm bs})-1\big\}^{\frac{3}{2}}\Big]_{\phi_{\rm S0}}^{\phi_{\rm SL}} \\
&- const0\, C_{\rm ox}\frac{1}{\beta}\frac{2}{3}\Big[\phi_{\rm S}\big\{\beta(\phi_{\rm S}-V_{\rm bs})-1\big\}^{\frac{3}{2}}\Big]_{\phi_{\rm S0}}^{\phi_{\rm SL}} + const0\, C_{\rm ox}\frac{1}{\beta}\frac{2}{3}\frac{1}{\beta}\frac{2}{5}\Big[\big\{\beta(\phi_{\rm S}-V_{\rm bs})-1\big\}^{\frac{5}{2}}\Big]_{\phi_{\rm S0}}^{\phi_{\rm SL}} \\
&- const0^2\frac{1}{\beta}\frac{1}{2}\big[\beta^2(\phi_{\rm SL}-V_{\rm bs})^2-2\beta(\phi_{\rm SL}-V_{\rm bs})+1-\beta^2(\phi_{\rm S0}-V_{\rm bs})^2+2\beta(\phi_{\rm S0}-V_{\rm bs})-1\big]\Bigg] \\
&- \frac{1}{\beta}\frac{\mu(W_{\rm eff}\cdot\mathbf{NF})^2}{I_{\rm ds}}\Big[const0\, C_{\rm ox}\frac{1}{\beta}\frac{2}{3}\big\{\beta(\phi_{\rm S}-V_{\rm bs})-1\big\}^{\frac{3}{2}} + \frac{1}{2}const0^2\beta\phi_{\rm S}\Big]_{\phi_{\rm S0}}^{\phi_{\rm SL}}
\end{aligned} \tag{19}$$

Here $const0$ is defined as

$$const0 = \sqrt{\frac{2\epsilon_{\rm Si} q N_{\rm sub}}{\beta}}$$

while μ and $I_{\rm ds}$ are the carrier mobility and the drain current, respectively [7, 8].

$$Q_{\rm I} = -WLC_{\rm ox}(VgVt)\frac{2}{3}\left(\frac{1+\alpha+\alpha^2}{1+\alpha}\right) \tag{20}$$

$$Q_{\rm D} = Q_{\rm I}\left(\frac{3}{5}-\frac{1}{5}\frac{1+2\alpha}{(1+\alpha)(1+\alpha+\alpha^2)}\right) \tag{21}$$

where the surface-potential-based description derives

$$\alpha = 1-\frac{(1+\delta)(\phi_{\rm SL}-\phi_{\rm S0})}{VgVt} \tag{22}$$

$$VgVt = V_{\rm gs}-\left(\mathbf{VFBC}+\phi_{\rm S0}+\frac{const0}{C_{\rm ox}}BPS0^{\frac{1}{2}}\right) \tag{23}$$

$$\delta = C0Cox\frac{4}{3}\frac{1}{\beta}\frac{(BPSL^{\frac{3}{2}}-BPS0^{\frac{3}{2}})}{(\phi_{\rm SL}-\phi_{\rm S0})^2} - C0Cox\frac{2}{\beta}\frac{(BPSL^{\frac{1}{2}}-BPS0^{\frac{1}{2}})}{(\phi_{\rm SL}-\phi_{\rm S0})^2} - 2C0Cox\frac{BPS0^{\frac{1}{2}}}{(\phi_{\rm SL}-\phi_{\rm S0})} \tag{24}$$

and

$$
\begin{aligned}
C0Cox =& \frac{const0}{C_{\rm ox}} \\
BPSL^{\frac{1}{2}} =& \sqrt{\beta(\phi_{\rm SL} - V_{\rm bs}) - 1} \\
BPS0^{\frac{1}{2}} =& \sqrt{\beta(\phi_{\rm S0} - V_{\rm bs}) - 1} \\
BPSL^{\frac{3}{2}} =& (BPSL^{\frac{1}{2}})^3 \\
BPS0^{\frac{3}{2}} =& (BPS0^{\frac{1}{2}})^3
\end{aligned} \tag{25}
$$

The HiSIM model parameters introduced in section 4 are summarized in Table 4.

Table 4: HiSIM model parameters introduced in section 4 of this manual. $*$ indicates minor parameters.

VFBC	flat-band voltage
VBI	built-in potentail
TOX	physical gate-oxide thickness
KAPPA	dielectric constant of gate dielectric
***DDLTMAX**	smoothing coefficient for $V_{\rm ds}$
***DDLTSLP**	$L_{\rm gate}$ dependence of smoothing coefficient
***DDLTICT**	$L_{\rm gate}$ dependence of smoothing coefficient

5 Drain Current

Under the gradual-channel approximation together with approximations of an idealized gate structure and uniform channel doping, the equation for the drain current $I_{\rm ds}$ is written [6, 9]

$$I_{\rm ds} = \frac{W_{\rm eff} \cdot \mathbf{NF}}{L_{\rm eff}} \cdot \mu \cdot \frac{I_{\rm dd}}{\beta} \tag{26}$$

$$\begin{aligned} I_{\rm dd} &= C_{\rm ox}(\beta V'_{\rm G} + 1)(\phi_{\rm SL} - \phi_{\rm S0}) - \frac{\beta}{2} C_{\rm ox}(\phi_{\rm SL}^2 - \phi_{\rm S0}^2) \\ &\quad - \frac{2}{3} const0 \Big[\big\{ \beta(\phi_{\rm SL} - V_{\rm bs}) - 1 \big\}^{\frac{3}{2}} - \big\{ \beta(\phi_{\rm S0} - V_{\rm bs}) - 1 \big\}^{\frac{3}{2}} \Big] \\ &\quad + const0 \Big[\big\{ \beta(\phi_{\rm SL} - V_{\rm bs}) - 1 \big\}^{\frac{1}{2}} - \big\{ \beta(\phi_{\rm S0} - V_{\rm bs}) - 1 \big\}^{\frac{1}{2}} \Big] \end{aligned} \tag{27}$$

The above description includes the further approximation that the mobility μ is independent of position along the channel y.

6 Threshold Voltage Shift

Different from the drift approximation, the drift-diffusion approximation does not require a threshold voltage parameter $V_{\rm th}$ for describing device performances. The MOSFET device parameters such as the oxide thickness $T_{\rm ox}$ and the substrate doping concentration $N_{\rm subc}$ determine the complete MOSFET behavior including the subthreshold characteristics automatically and consistently. However, HiSIM derives many detailed informations on the MOSFET fabrication technology with the $V_{\rm th}$ changes from a long-channel transistor ($\Delta V_{\rm th}$) as a function of gate length ($L_{\rm gate}$). The modeled $\Delta V_{\rm th}$ is incorporated in the $\phi_{\rm S}$ iteration as can be seen in Eq. (11), and can be viewed as consisting of two main effects or components:

(I) the short-channel effect: $\Delta V_{\rm th,SC}$

(II) the reverse-short-channel effect: $\Delta V_{\rm th,R}$ and $\Delta V_{\rm th,P}$

The separation into these two components ($\Delta V_{\rm th} = \Delta V_{\rm th,SC} + \Delta V_{\rm th,R}$ (or $\Delta V_{\rm th,P}$)) is schematically shown in Fig. 7.

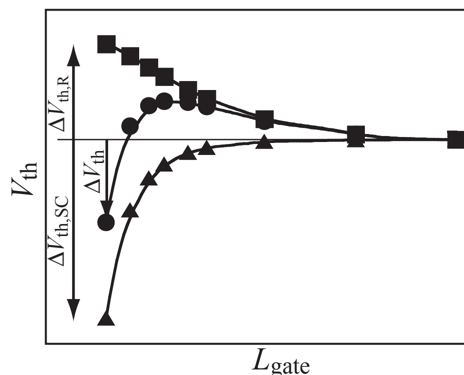

Fig. 7: Schematic plot of the separation of $V_{\rm th}$ into the contributions of the short-channel and the reverse-short-channel effect.

6.1 (I) Short-Channel Effects

All observed phenomena are caused by the lateral-electric-field contribution in the MOSFET channel, which is important even at threshold condition with small $V_{\rm ds}$. Thus $\Delta V_{\rm th,SC}$ can be written as a function of the lateral electric field E_y by applying the Gauss law. A parabolic potential distribution along the channel is approximated, which results in a position independent gradient of the lateral electric field $\frac{dE_y}{dy}$ [10]

$$\Delta V_{\rm th,SC} = \frac{\epsilon_{\rm Si}}{C_{\rm ox}} W_{\rm d} \frac{dE_y}{dy} \tag{28}$$

where $W_{\rm d}$ is the depletion-layer thickness written as

$$W_{\rm d} = \sqrt{\frac{2\epsilon_{\rm Si}(2\Phi_{\rm B} - V_{\rm bs})}{qN_{\rm sub}}} \tag{29}$$

$$2\Phi_{\rm B} = \frac{2}{\beta}\ln\left(\frac{N_{\rm sub}}{n_{\rm i}}\right) \tag{30}$$

where $n_{\rm i}$ is the intrinsic carrier density. $\frac{dE_y}{dy}$ is derived with model parameters in the form

$$\frac{dE_y}{dy} = \frac{2(\mathbf{VBI} - 2\Phi_{\rm B})}{(L_{\rm gate} - \mathbf{PARL2})^2}\left(\mathbf{SC1} + \mathbf{SC2}\cdot V_{\rm ds}\cdot\{1 + \mathbf{SC4}\cdot(2\Phi_{\rm B} - V_{\rm bs})\} + \mathbf{SC3}\cdot\frac{2\Phi_{\rm B} - V_{\rm bs}}{L_{\rm gate}}\right) \tag{31}$$

VBI and **PARL2** represent the built-in potential and the depletion width of the junction vertical to the channel, respectively. $V'_{\rm G}$ and $const0$ were defined in Eqs. (11) and (20), respectively. The model parameter **SC1** determines the threshold voltage shift for small $V_{\rm ds}$ and $V_{\rm bs}$, and is expected to be unity. If measured $V_{\rm th}$ is plotted as a function of $V_{\rm ds}$, it shows nearly a linear dependence. The gradient is proportional to **SC2**. **SC3** implements a correction of the charge-sheet approximation as well as the impurity-profile gradient along the vertical direction, and is expected to be small. **PTHROU**, describing the increase of the subthreshold swing for short-channel transistors, was deleted and was modeled as the punchthrough effect.

6.2 (II) Reverse-Short-Channel Effects

The reverse-short-channel effect is categorized into resulting from two physical MOSFET properties:

(i) Impurity concentration inhomogeneity in the direction vertical to the channel (vertical channel inhomogeneity)
(obvious in the retrograded implantation): $\Delta V_{\rm th,R}$

(ii) Impurity concentration inhomogeneity in the direction parallel to the channel (lateral channel inhomogeneity)
(obvious in the pocket implantation): $\Delta V_{\rm th,P}$

(i) Impurity concentration inhomogeneity in the direction vertical to the channel (Retrograded Implantation)

The above model parameters **SC3** and **SCP3** (see in 6.2. (ii)) can be successfully used, if the inhomogeneity is not extremely large.

For cases where the inhomogeneity is large or where positive $V_{\rm bs}$ is applied, deviation from the linearity of $V_{\rm th}$ as a function of $\sqrt{2\Phi_{\rm B} - V_{\rm bs}}$ is modeled with two fitting parameters **BS1** and **BS2** as

$$Q_{\rm Bmod} = \sqrt{2q\cdot N_{\rm sub}\cdot\epsilon_{Si}\cdot\left(2\Phi_{\rm B} - V_{\rm bs} - \frac{\mathbf{BS1}}{\mathbf{BS2} - V_{\rm bs}}\right)} \tag{32}$$

where **BS1** represents the strength of the deviation and **BS2** is the starting value of $V_{\rm bs}$ where the deviation becomes visible. This $Q_{\rm Bmod}$ is incorporated into the $\Delta V_{\rm th}$ desription as be seen in Eq. (34).

(ii) Impurity concentration inhomogeneity in the lateral direction parallel to the channel (Pocket Implantation)

The model equations for the $V_{\rm th}$ shift due to the pocket implant are:

$$\Delta V_{\rm th,P} = (V_{\rm th,R} - V_{\rm th0})\frac{\epsilon_{\rm Si}}{C_{\rm ox}}W_{\rm d}\frac{dE_{y,\rm P}}{dy} \tag{33}$$

$$V_{\rm th,R} = \mathbf{VFBC} + 2\Phi_{\rm B} + \frac{Q_{\rm Bmod}}{C_{\rm ox}} + \frac{1}{\beta}\log\left(\frac{N_{\rm subb}}{N_{\rm subc}}\right) \tag{34}$$

$$V_{\rm th0} = \mathbf{VFBC} + 2\Phi_{\rm BC} + \frac{\sqrt{2qN_{\rm subc}\epsilon_{\rm Si}(2\Phi_{\rm BC} - V_{\rm bs})}}{C_{\rm ox}} \tag{35}$$

$$\frac{dE_{y,\rm P}}{dy} = \frac{2(\mathbf{VBI} - 2\Phi_{\rm B})}{\mathbf{LP}^2}\left(\mathbf{SCP1} + \mathbf{SCP2}\cdot V_{\rm ds} + \mathbf{SCP3}\cdot\frac{2\Phi_{\rm B} - V_{\rm bs}}{\mathbf{LP}}\right) \tag{36}$$

$$N_{\rm subb} = 2\cdot\mathbf{NSUBP} - \frac{(\mathbf{NSUBP} - N_{\rm subc})\cdot L_{\rm gate}}{\mathbf{LP}} - N_{\rm subc} \tag{37}$$

where $N_{\rm subc}$ is the substrate impurity concentration as defined in Eq. (74). The parameters **SCP1 - SCP3** describe the short-channel effect caused by the potential minimum at the higher impurity concentration of the pocket. $2\Phi_{\rm BC}$ is the potential giving threshold condition with $N_{\rm subc}$ and $2\Phi_{\rm B}$ is the equivalent potential with $N_{\rm sub}$

$$\Phi_{\rm BC} = \frac{2}{\beta}\ln\left(\frac{N_{\rm subc}}{n_{\rm i}}\right) \tag{38}$$

$$\Phi_{\rm B} = \frac{2}{\beta}\ln\left(\frac{N_{\rm sub}}{n_{\rm i}}\right) \tag{39}$$

$$N_{\rm sub} = \frac{N_{\rm subc}(L_{\rm gate} - \mathbf{LP}) + \mathbf{NSUBP}\cdot\mathbf{LP}}{L_{\rm gate}} \tag{40}$$

As defined in Eq. (40), $N_{\rm sub}$ is replaced to the averaged impurity concentration in the channel and $N_{\rm subb}$ is introduced, beginning from channel lengths where pockets at source and drain start to overlap.
As $V_{\rm ds}$ approaches zero, the $V_{\rm th}$ dependence on $V_{\rm ds}$ deviates from linearity and $V_{\rm th}$ increases drastically as shown schematically in Fig. 8. This is modeled with two model parameters **SCP21** and **SCP22** as

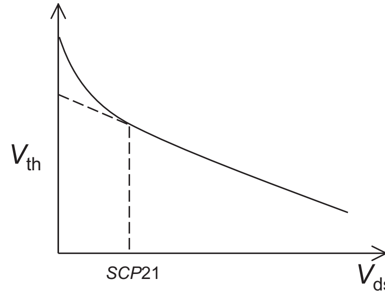

Fig. 8: Threshold voltage as a function of $V_{\rm ds}$. The deviation from linearity for small $V_{\rm ds}$ is modeled with parameters **SCP21** and **SCP22**.

$$\Delta V_{\rm th,P} = \Delta V_{\rm th,P} - \frac{\mathbf{SCP22}}{(\mathbf{SCP21} + V_{\rm ds})^2} \tag{41}$$

where **SCP21** determines the $V_{\rm ds}$ value at which $V_{\rm th}$ starts to deviate from linearity as a function of $V_{\rm ds}$. The parameter **SCP22** determines the gradient of this deviation.

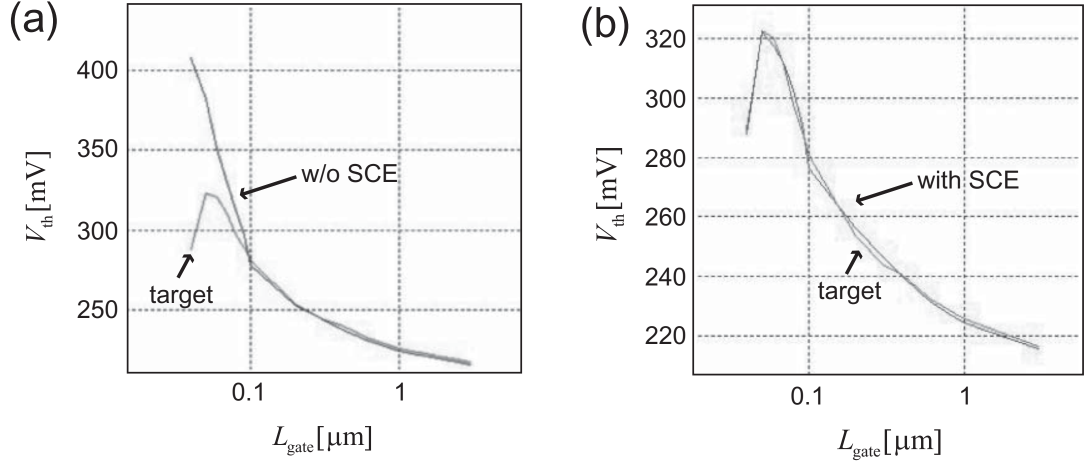

Fig. 9: Comparison of measurements and pocket-implant model for $V_{\rm th}$ as a function of $L_{\rm gate}$. Results (a) with and (b) without short-channel effects (SCE) are shown.

$V_{\rm th,R}$ and $V_{\rm th0}$, defined in Eqs. (34) and (35), are the threshold voltages for the cases with and without pocket-implant, respectively. The overlap start of source and drain pockets causes a steep increase of $V_{\rm th}$ as a function of decreasing $L_{\rm gate}$. This effect enables to extract **LP** from measurements. Fig. 9 compares the $V_{\rm th}$-$L_{\rm gate}$ characteristics of the developed pocket-implant model with and without inclusion of the short-channel effects (SCE). The steep increase at $L_{\rm gate}$=0.1μm in Fig. 9a means the starting of the pocket overlap, where **LP**=0.05μm.

In some cases the pocket profile cannot be described by the single linearly decreasing form, but provides extensive tails as schematically shown in Fig. 10. Therefore, two model parameters **NPEXT** and **LPEXT** are introduced to model the pocket tails as

$$N_{\rm sub} = N_{\rm sub} + \frac{\mathbf{NPEXT} - N_{\rm subc}}{\left(\frac{1}{\mathbf{xx}} + \frac{1}{\mathbf{LPEXT}}\right) L_{\rm gate}} \tag{42}$$

where

$$\mathbf{xx} = 0.5 \cdot L_{\rm gate} - \mathbf{LP} \ . \tag{43}$$

NPEXT is the maximum concentration of the pocket tail and **LPEXT** describes the tail extension characteristics. Usually strong pocket implantation induces a vertical impurity distribution at the same time. For fitting the measured results in such cases it is recommended to use the parameter **SCP3** together with parameters **BS1** and **BS2**.

The HiSIM model parameters introduced in section 6 are summarized in Table 5.

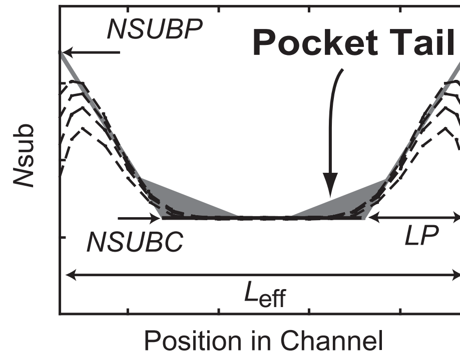

Fig. 10: Modeled pocket tail with **NPEXT** and **LPEXT**.

Table 5: HiSIM model parameters introduced in section 6 of this manual. ∗ indicates minor parameters.

Parameter	Description
VBI	built-in potential
PARL2	depletion width of channel/contact junction
SC1	magnitude of short-channel effect
SC2	$V_{\rm ds}$ dependence of short-channel effect
∗**SC3**	$V_{\rm bs}$ dependence of short-channel effect
∗**SC4**	$V_{\rm bs}$ dependence of short-channel effect
NSUBP	maximum pocket concentration
LP	pocket penetration length
∗**BS1**	body-coefficient modification due to impurity profile
∗**BS2**	body-coefficient modification due to impurity profile
SCP1	magnitude of short-channel effect due to pocket
SCP2	$V_{\rm ds}$ dependence of short-channel due to pocket
∗**SCP3**	$V_{\rm bs}$ dependence of short-channel effect due to pocket
∗**SCP21**	short-channel-effect modification for small $V_{\rm ds}$
∗**SCP22**	short-channel-effect modification for small $V_{\rm ds}$
∗**NPEXT**	maximum concentration of pocket tail
∗**LPEXT**	extension length of pocket tail

7 Short-Channel Effects

7.1 Punchthrough Effect

The origin of the punchthrough effect is the bipolar effect through source, substrate, and drain.The effect is described by a power function of the potential difference

$$POTENTIAL = (\mathbf{VBI} - \phi_{\mathrm{S0}})^{\mathbf{PTP}} \tag{44}$$

The final drain current I_{ds} is written

$$\begin{aligned} I_{\mathrm{ds}} &= I_{\mathrm{ds}} + PUNCH \\ PUNCH &= \frac{W_{\mathrm{eff}} \cdot \mathbf{NF}}{L_{\mathrm{eff}}} \frac{\mu}{\beta} \cdot (\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}) \\ & \left\{ C_{\mathrm{ox}} \cdot \beta \frac{\mathbf{PTL}}{(L_{\mathrm{gate}} \cdot 10^6)^{\mathbf{PTLP}}} \cdot POTENTIAL \cdot \left(1 + \mathbf{PT2} \cdot V_{\mathrm{ds}} + \frac{\mathbf{PT4} \cdot (\phi_{\mathrm{S0}} - V_{\mathrm{bs}})}{(L_{\mathrm{gate}} \cdot 10^6)^{\mathbf{PT4P}}} \right) \right\} \end{aligned} \tag{45}$$

where model parameters **PTL**, **PTLP**, **PT2**, **PT4**, and **PT4P** are introduced.

7.2 Channel Conductance

The high field under the saturation condition causes the pinch-off region and the current flows away from the surface. This effect is considered as the lateral-field-induced charge for the capacitacne (see section 16). The simplified formulation is applied to consider the effect as

$$\begin{aligned} I_{\mathrm{ds}} &= I_{\mathrm{ds}} + \frac{W_{\mathrm{eff}} \cdot \mathbf{NF}}{L_{\mathrm{eff}}} \frac{\mu}{\beta} \cdot (\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}) \cdot CONDUCTANCE \\ CONDUCTANCE &= C_{\mathrm{ox}} \cdot \beta \frac{\mathbf{GDL}}{(L_{\mathrm{gate}} \cdot 10^6 + \mathbf{GDLD} \cdot 10^6)^{\mathbf{GDLP}}} \cdot V_{\mathrm{ds}} \end{aligned} \tag{46}$$

The HiSIM model parameters introduced in section 7 are summarized in Table 6.

Table 6: HiSIM model parameters introduced in section 7 of this manual. ∗ indicates minor parameters.

Parameter	Description
∗**PTL**	strength of punchthrough effect
∗**PTLP**	channel-length dependence of punchthrough effect
∗**PTP**	strength of punchthrough effect
∗**PT2**	V_{ds} dependence of punchthrough effect
∗**PT4**	V_{bs} dependence of punchthrough effect
∗**PT4P**	V_{bs} dependence of punchthrough effect
∗**GDL**	strength of high-field effect
∗**GDLP**	channel-length dependence of high-field effect
∗**GDLD**	channel-length dependence of high-field effect

8 Depletion Effect of the Gate Poly-Si

Carrier depletion in the gate poly-Si near the gate-oxide interface starts after the formation of the inversion layer in the substrate as shown in Fig. 11.

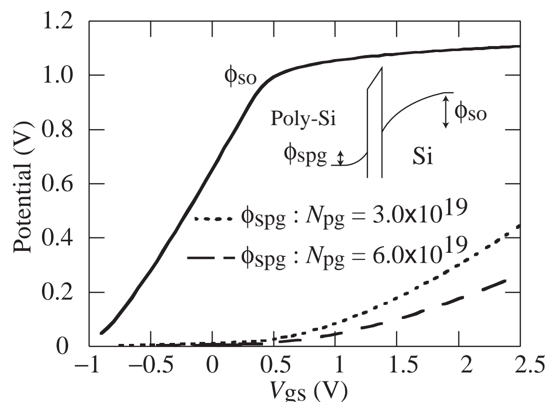

Fig. 11: Simulated surface potential at the source side ($\phi_{\rm S0}$) as a function of $V_{\rm gs}$. The poly-depletion potential is also shown for two doping concentrations $N_{\rm pg}$ in the poly-Si.

To eliminate the necessary iteration procedure for the circuit-simulation application, the potential drop within the poly-Si $\phi_{\rm Spg}$ is approximated as a function of $V_{\rm gs}$ and $V_{\rm ds}$ by the simple formula of Eq. (47), and is included in the $\Delta V_{\rm th}$ calculation as a potential drop of $V_{\rm gs}$.

$$\phi_{\rm Spg} = \mathbf{PGD1} \left(1 + \frac{1}{L_{\rm gate} \cdot 10^6}\right)^{\mathbf{PGD4}} \exp\left(\frac{V_{\rm gs} - \mathbf{PGD2}}{V}\right) \tag{47}$$

The HiSIM model parameters introduced in section 8 are summarized in Table 7.

Table 7: HiSIM model parameters introduced in section 8 of this manual. ∗ indicates a minor parameter.

PGD1	strength of poly depletion
PGD2	threshold voltage of poly depletion
∗**PGD4**	$L_{\rm gate}$ dependence of poly depletion

9 Quantum-Mechanical Effects

The main quantum-mechanical phenomenon, which has to be included into a MOSFET model for circuit simulation, is the repulsion of the channel's carrier-density peak into the substrate away from the surface. This can be described phenomenologically by an increased effective oxide thickness $T_{\rm ox}$ [20, 21]. The calculated $\Delta T_{\rm ox}$-$V_{\rm gs}$ characteristics is shown in Fig. 12. Equations implemented into HiSIM for the reproduction of quantum mechanical effects are:

$$T_{\rm ox} = \mathbf{TOX} + \Delta T_{\rm ox} \tag{48}$$

$$\Delta T_{\rm ox} = \frac{\mathbf{QME1}}{V_{\rm gs} - V_{\rm th}(T_{\rm ox} = \mathbf{TOX}) + \mathbf{QME2}} + \mathbf{QME3} \tag{49}$$

where **QME1**, **QME2**, and **QME3** are the quantum-effect model parameters. A limiting function is introduced in the source code to avoid unreasonable $\Delta T_{\rm ox}$ increase below the threshold voltage.

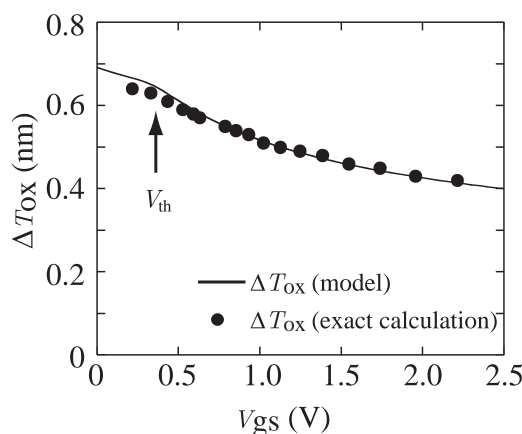

Fig. 12: Calculated $T_{\rm ox}$ increase by the quantum mechanical effect. The solid line shows model results with Eqs. (48) and (49). Symbols are exact calculation results by solving the Poisson equation and the Schrödinger equation simultaneously.

The HiSIM model parameters introduced in section 9 are summarized in Table 8.

Table 8: HiSIM model parameters introduced in section 9 of this manual.

QME1	$V_{\rm gs}$ dependence
QME2	$V_{\rm gs}$ dependence
QME3	minimum $T_{\rm ox}$ modification

10 Mobility Model

The low-field mobility is described with the following expressions and includes the three independent mechanisms of Coulomb, phonon and surface-roughness scattering [22]:

$$\frac{1}{\mu_0} = \frac{1}{\mu_{\rm CB}} + \frac{1}{\mu_{\rm PH}} + \frac{1}{\mu_{\rm SR}} \tag{50}$$

$$\mu_{\rm CB}(\text{Coulomb}) = \mathbf{MUECB0} + \mathbf{MUECB1}\frac{Q_{\rm i}}{q \cdot 10^{11}} \tag{51}$$

$$\mu_{\rm PH}(\text{phonon}) = \frac{M_{\rm uephonon}}{E_{\rm eff}^{\mathbf{MUEPH0}}} \tag{52}$$

$$\mu_{\rm SR}(\text{surface roughness}) = \frac{\mathbf{MUESR1}}{E_{\rm eff}^{M_{\rm uesurface}}} \tag{53}$$

where $\mu_{\rm PH}$(phonon) is temperature dependent as modeled in section 14.
Here $E_{\rm eff}$ is the effective field normal to the surface. The field are written as

$$E_{\rm eff} = \frac{1}{\epsilon_{\rm Si}}\left(N_{\rm dep} \cdot Q_{\rm b} + \mathbf{NINV} \cdot Q_{\rm i}\right) \cdot f(\phi_{\rm S}) \tag{54}$$

$$f(\phi_{\rm S}) = \frac{1}{1 + (\phi_{\rm SL} - \phi_{\rm S0}) \cdot N_{\rm invd}} \tag{55}$$

$$N_{\rm invd} = \mathbf{NINVD} \tag{56}$$

where $N_{\rm dep}$ considers the gate length dependence with two model parameters **NDEPL** and **NDEPLP** as

$$N_{\rm dep} = \mathbf{NDEP}\frac{L_{\rm gate}^{\mathbf{NDEPLP}}}{\mathbf{NDEPL} + (L_{\rm gate} \cdot 10^6)^{\mathbf{NDEPLP}}} \tag{57}$$

The funtion $f(\phi_{\rm S})$ is introduced to reproduce the reduced resistance effect for small $V_{\rm ds}$ with the model parameter **NINVD**.
The mobility universality preserves following conditions [23, 24]

$$\mathbf{MUEPH0} \simeq 0.3 \tag{58}$$

$$M_{\rm uesurface} = 2.0 \tag{59}$$

$$\mathbf{NDEP} = 1.0 \tag{60}$$

$$\mathbf{NINV} = 0.5 \tag{61}$$

However, these parameters can be used for fitting purposes [25], if it is necessary.
The $L_{\rm gate}$ dependence of the mobility is considered as

$$M_{\rm uephonon} = \mathbf{MUEPH1} \cdot \left(1 + \frac{\mathbf{MUEPHL}}{(L_{\rm gate} \cdot 10^6)^{\mathbf{MUEPLP}}}\right) \tag{62}$$

$$M_{\rm uesurface} = \mathbf{MUESR0} \cdot \left(1 + \frac{\mathbf{MUESRL}}{(L_{\rm gate} \cdot 10^6)^{\mathbf{MUESLP}}}\right) \tag{63}$$

The high-field mobility is modeled as [26]

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_\mathrm{y}}{V_\mathrm{max}}\right)^{\mathbf{BB}}\right)^{\frac{1}{\mathbf{BB}}}} \tag{64}$$

The velocity overshoot is included in the mobility model in the following manner

$$V_\mathrm{max} = \mathbf{VMAX} \cdot \left(1 + \frac{\mathbf{VOVER}}{(L_\mathrm{gate} \cdot 10^6)^{\mathbf{VOVERP}}}\right) \tag{65}$$

The HiSIM model parameters introduced in section 10 are summarized in Table 9.

Table 9: HiSIM model parameters introduced in section 10 of this manual. ∗ indicates minor parameters.

MUECB0	Coulomb scattering
MUECB1	Coulomb scattering
MUEPH0	phonon scattering
MUEPH1	phonon scattering
∗**MUEPHL**	length dependence of phonon mobility reduction
∗**MUEPLP**	length dependence of phonon mobility reduction
MUESR0	surface-roughness scattering
MUESR1	surface-roughness scattering
∗**MUESRL**	length dependence of surface roughness mobility reduction
∗**MUESLP**	length dependence of surface roughness mobility reduction
NDEP	depletion charge contribution on effective-electric field
***NDEPL**	modification of depletion charge contribution for short-channel case
***NDEPLP**	modification of depletion charge contribution for short-channel case
NINV	inversion charge contribution on effective-electric field
***NINVD**	reduced resistance effect for small V_ds
BB	high-field-mobility degradation
VMAX	maximum saturation velocity
VOVER	velocity overshoot effect
VOVERP	L_eff dependence of velocity overshoot

11 Channel-Length Modulation

The gradual-channel approximation is applied to derive analytical equations for describing device characteristics. However, this approximation is not valid for large $V_{\rm ds}$ causing the pinch-off phenomenon in the channel. To include the pinch-off phenomenon in HiSIM, we apply the conventional method of modeling the pinch-off region (ΔL) separately from the rest of the channel as depicted in Fig. 13 [28].

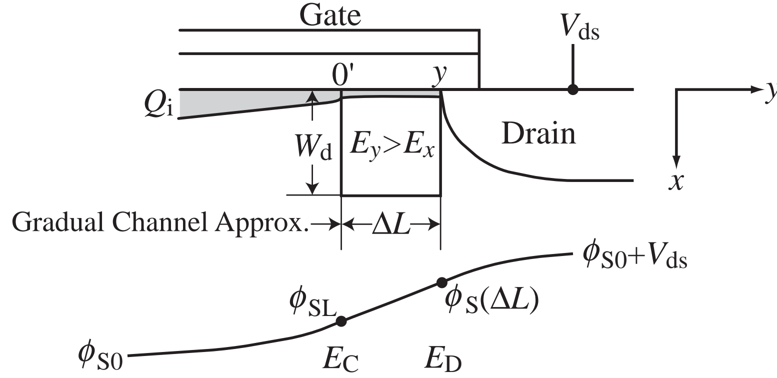

Fig. 13: Schematic showing the correlation among physical quantities in the pinch-off region.

The potential value at the end of the channel ($\phi_{\rm S}(\Delta L)$) lies between $\phi_{\rm SL}$ and $\phi_{\rm S0}+V_{\rm ds}$. The exact value is dependent on the junction profile between the channel and the drain contact. This dependence is modeled with the parameter **CLM1** as

$$\phi_{\rm S}(\Delta L) = (1 - \mathbf{CLM1})\cdot\phi_{\rm SL} + \mathbf{CLM1}\cdot(\phi_{\rm S0}+V_{\rm ds}) \tag{66}$$

where **CLM1** can be interpreted to represent the hardness of the junction and must be in the range $0 \le \mathbf{CLM1} \le 1$. Here $\mathbf{CLM1} = 1$ means that the contact profile is abrupt and the complete potential increase occurs in the ΔL region, whereas $\mathbf{CLM1} = 0$ corresponds to the opposite condition and there is no potential increase in the ΔL region.

The final ΔL is derived as

$$\begin{aligned}\Delta L =& \frac{1}{2}\Bigg[-\frac{1}{L_{eff}}\left(2\frac{I_{\rm dd}}{\beta Q_{\rm i}}z + 2\frac{N_{\rm sub}}{\epsilon_{Si}}(\phi_s(\Delta L)-\phi_{SL})z^2 + E_0 z^2\right)\\ &+\sqrt{\frac{1}{L_{eff}^2}\left(2\frac{I_{\rm dd}}{\beta Q_{\rm i}}z + 2\frac{N_{\rm sub}}{\epsilon_{Si}}(\phi_s(\Delta L)-\phi_{SL})z^2 + E_0 z^2\right)^2 + 4\left(2\frac{N_{\rm sub}}{\epsilon_{Si}}(\phi_s(\Delta L)-\phi_{SL})z^2 + E_0 z^2\right)}\Bigg]\end{aligned} \tag{67}$$

where E_0 is fixed to 10^5 and

$$z = \frac{\epsilon_{Si}}{\mathbf{CLM2}\cdot Q_b + \mathbf{CLM3}\cdot Q_i} \tag{68}$$

Two model parameters **CLM2** and **CLM3** are introduced to consider the uncertainty of $Q_{\rm i}$ in the pinch-off region and to counterbalance the two contributions from $Q_{\rm b}$ ($= qN_{\rm sub}W_{\rm d}$) and $Q_{\rm i}$. It has to be notified that ΔL is equal to zero, when **CLM1**=0.

Additional contributions on CLM such as the pocket effect is modeled as

$$\Delta L = \Delta L \left(1 + \mathbf{CLM6} \cdot (L_{\rm gate} \cdot 10^{6})^{\mathbf{CLM5}}\right) \tag{69}$$

It can be happen that $L_{\rm eff} - \Delta L$ becomes negative, if extracted **CLM5** and **CLM6** values are out of acceptable ranges. In this case HiSIM gives "warning" and fixes $L_{\rm eff} - \Delta L$ to $1nm$.

The HiSIM model parameters introduced in section 11 are summarized in Table 10.

Table 10: HiSIM model parameters introduced in section 11 of this manual.

CLM1	hardness coefficient of channel/contact junction
CLM2	coefficient for $Q_{\rm B}$ contribution
CLM3	coefficient for $Q_{\rm I}$ contribution
***CLM5**	effect of pocket implantation
***CLM6**	effect of pocket implantation

12 Narrow-Channel Effects

12.1 Threshold Voltage Modification

The fringing capacitances $C_{\rm ef}$ at the edge of the isolation is modeled [8] as

$$\Delta V_{\rm th,W} = \left(\frac{1}{C_{\rm ox}} - \frac{1}{C_{\rm ox} + 2C_{\rm ef}/(L_{\rm eff}W_{\rm eff})}\right) qN_{\rm sub}W_{\rm d} + \frac{\mathbf{WVTH0}}{W_{\rm gate}\cdot 10^6} \tag{70}$$

where **WVTH0** is the parameter for including the basic width dependence and

$$C_{\rm ef} = \frac{2\epsilon_{\rm ox}}{\pi}L_{\rm eff}\ln\left(\frac{2T_{\rm fox}}{T_{\rm ox}}\right) = \frac{\mathbf{WFC}}{2}L_{\rm eff} \tag{71}$$

Here, $T_{\rm fox}$ is the thickness of the oxide at the trench edge, and **WFC** is the model parameter for including the edge-fringing-capacitance effects. The final $\Delta V_{\rm th}$ of Eq. (11), under inclusion of the shallow-trench-isolation effects, becomes:

$$\Delta V_{\rm th} = \Delta V_{\rm th,SC} + \Delta V_{\rm th,R} + \Delta V_{\rm th,P} + \Delta V_{\rm th,W} - \phi_{\rm Spg} \tag{72}$$

The width dependence of the pocket impurity concentration is modeled as

$$N_{\rm subp} = \mathbf{NSUBP}\cdot\left(1 + \frac{\mathbf{NSUBP0}}{(W_{\rm gate}\cdot 10^6)^{\mathbf{NSUBWP}}}\right) \tag{73}$$

The width dependence of the substrate impurity concentration $N_{\rm subc}$ is also considered as

$$N_{\rm subc} = \mathbf{NSUBC}\cdot\left(1 + \frac{\mathbf{NSUBCW}}{(W_{\rm gate}\cdot 10^6)^{\mathbf{NSUBCWP}}}\right) \tag{74}$$

12.2 Mobility Change

A reduction of $I_{\rm ds,sat}$ with reduced $W_{\rm gate}$ as indicated by curve C1 in Fig. 14 [30] is modeled by a decreasing phonon mobility with two model parameters **MUEPHW** and **MUEPWP** as

$$M_{\rm uephonon} = M_{\rm uephonon}\cdot\left(1 + \frac{\mathbf{MUEPHW}}{(W_{\rm gate}\cdot 10^6)^{\mathbf{MUEPWP}}}\right) \tag{75}$$

A start to increase for narrower $W_{\rm gate}$ as denoted by curve C2 is modeled as a change of the surface-roughness contribution caused by a carrier flow in increasing distance from the surface as

$$M_{\rm uesurface} = M_{\rm uesurface}\cdot\left(1 + \frac{\mathbf{MUESRW}}{(W_{\rm gate}\cdot 10^6)^{\mathbf{MUESWP}}}\right) \tag{76}$$

Further width dependences are included as

$$N_{\rm invd} = N_{\rm invd}\cdot\left(1 + \frac{\mathbf{NINVDW}}{(W_{\rm gate}\cdot 10^6)^{\mathbf{NINVDWP}}}\right) \tag{77}$$

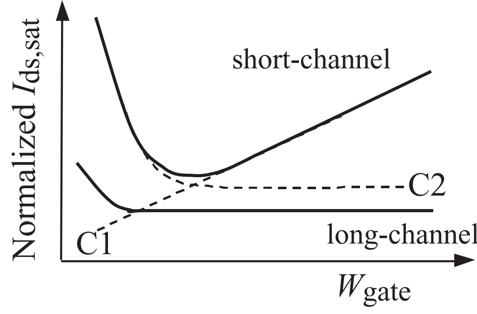

Fig. 14: Schematic of the normalized saturation current $I_{\rm ds,sat}$ as a function of the gate width $W_{\rm gate}$ for two different gate lengths $L_{\rm gate}$.

12.3 Transistor Leakage due to Shallow Trench Isolation (STI): Hump in $I_{\rm ds}$

The surface potential of the leakage regions at the trench edges can be derived analytically as [31]

$$\phi_{\rm S,STI} = V'_{\rm gs,STI} + \frac{\epsilon_{\rm Si} Q_{\rm N,STI}}{C'^{\,2}_{\rm ox}} \left[1 - \sqrt{1 + \frac{2C'^{\,2}_{\rm ox}}{\epsilon_{\rm Si} Q_{\rm N,STI}} \left(V'_{\rm gs,STI} - V_{\rm bs} - \frac{1}{\beta} \right)} \right] \tag{78}$$

where

$$Q_{\rm N,STI} = q \cdot \mathbf{NSTI} \tag{79}$$

$$V'_{\rm gs,STI} = V_{\rm gs} - \mathbf{VFBC} + V_{\rm thSTI} + \Delta V_{\rm th,SCSTI} \tag{80}$$

where

$$V_{\rm thSTI} = \mathbf{VTHSTI} - \mathbf{VDSTI} \cdot V_{\rm ds} \tag{81}$$

and

$$\Delta V_{\rm th,SCSTI} = \frac{\epsilon_{\rm Si}}{C_{\rm ox}} W_{\rm d,STI} \frac{dE_y}{dy} \tag{82}$$

The threshold voltage for the STI effect **VTHSTI** includes features of STI such as **NSTI** which are diferent from the substrate. The depletion-layer thickness $W_{\rm d,STI}$ is written as

$$W_{\rm d,STI} = \sqrt{\frac{2\epsilon_{\rm Si}(2\Phi_{\rm B,STI} - V_{\rm bs})}{q\mathbf{NSTI}}}. \tag{83}$$

$\frac{dE_y}{dy}$ is described with model parameters in the same form as in section 6.1 on short-channel effects

$$\frac{dE_y}{dy} = \frac{2(\mathbf{VBI} - 2\Phi_{\rm B,STI})}{(L_{\rm gate,sm} - \mathbf{PARL2})^2} (\mathbf{SCSTI1} + \mathbf{SCSTI2} \cdot V_{\rm ds}) \tag{84}$$

where

$$L_{\rm gate,sm} = L_{\rm gate} + \frac{\mathbf{WL1}}{wl^{\mathbf{WL1P}}} \tag{85}$$

$$wl = (W_{\mathrm{gate}} \cdot 10^6) \times (L_{\mathrm{gate}} \cdot 10^6) \tag{86}$$

The modeling of the transistor leakage for STI technologies is based on the idea that the current in the subthreshold region is governed only by the diffusion term. The carrier concentration $Q_{\mathrm{i,STI}}$ is calculated analytically for the subthreshold region, where the STI effect is obvious [1]. The final leakage current equation is written as

$$I_{\mathrm{ds,STI}} = 2\frac{W_{\mathrm{STI}}}{L_{\mathrm{eff}} - \Delta L}\mu\frac{Q_{\mathrm{i,STI}}}{\beta}\left[1 - \exp(-\beta V_{\mathrm{ds}})\right] \tag{87}$$

where W_{STI} determines the width of the high-field region. The gate length dependence of W_{STI} is included as

$$W_{\mathrm{STI}} = \mathbf{WSTI}\left(1 + \frac{\mathbf{WSTIL}}{(L_{\mathrm{gate,sm}} \cdot 10^6)^{\mathbf{WSTILP}}}\right)\left(1 + \frac{\mathbf{WSTIW}}{(W_{\mathrm{gate,sm}} \cdot 10^6)^{\mathbf{WSTIWP}}}\right) \tag{88}$$

12.4 Small Geometry

Small size devices do not show the same scaling characteristic as long-channel or wide-channel devices, but rather deviate significantly. The reason is mainly due to the resolution inaccuracy of the lithography. The small geometry effects are modeled first as the threshold voltage shift

$$\Delta V_{\mathrm{th}} = \Delta V_{\mathrm{th,SC}} + \Delta V_{\mathrm{th,R}} + \Delta V_{\mathrm{th,P}} + \Delta V_{\mathrm{th,W}} + \Delta V_{\mathrm{th,sm}} - \phi_{\mathrm{Spg}} \tag{89}$$

where

$$\Delta V_{\mathrm{th,sm}} = \frac{\mathbf{WL2}}{wl^{\mathbf{WL2P}}} \tag{90}$$

The mobility modification due to the small device geometry is also modeled in the phonon scattering as

$$M_{\mathrm{uephonon}} = M_{\mathrm{uephonon}} \cdot \left(1 + \frac{\mathbf{MUEPHS}}{wl^{\mathbf{MUEPSP}}}\right) \tag{91}$$

$$V_{\mathrm{max}} = V_{\mathrm{max}} \cdot \left(1 + \frac{\mathbf{VOVERS}}{wl^{\mathbf{VOVERSP}}}\right) \tag{92}$$

The HiSIM model parameters introduced in section 12 are summarized in Table 11.

Table 11: HiSIM model parameters introduced in section 12 of this manual. ∗ indicates minor parameters.

WFC	threshold voltage change due to capacitance change
∗**WVTH0**	threshold voltage shift
NSUBC	substrate-impurity concentration
∗**NSUBCW**	width dependence of substrate-impurity concentration
∗**NSUBCWP**	width dependence of substrate-impurity concentration
∗**NSUBP0**	modification of pocket concentration for narrow width
∗**NSUBWP**	modification of pocket concentration for narrow width
∗**MUEPHW**	phonon related mobility reduction
∗**MUEPWP**	phonon related mobility reduction
∗**MUESRW**	change of surface roughness related mobility
∗**MUESWP**	change of surface roughness related mobility
∗**NINVDW**	width dependence on high field mobility
∗**NINVDWP**	width dependence on high field mobility
∗**VTHSTI**	threshold voltage shift due to STI
∗**VDSTI**	threshold voltage shift dependence on $V_{\rm ds}$ due to STI
***SCSTI1**	the same effect as **SC1** but at STI edge
***SCSTI2**	the same effect as **SC2** but at STI edge
NSTI	substrate-impurity concentration at the STI edge
WSTI	width of the high-field region at STI edge
***WSTIL**	channel-length dependence of **WSTI**
***WSTILP**	channel-length dependence of **WSTI**
***WSTIW**	channel-width dependence of **WSTI**
***WSTIWP**	channel-width dependence of **WSTI**
WL1	threshold volatge shift of STI leakage due to small size effect
WL1P	threshold voltage shift of STI leakage due to small size effect
WL2	threshold volatge shift due to small size effect
WL2P	threshold voltage shift due to small size effect
∗**MUEPHS**	mobility modification due to small size
∗**MUEPSP**	mobility modification due to small size
∗**VOVERS**	modification of maximum velocity due to small size
∗**VOVERSP**	modification of maximum velocity due to small size

13 Effects of the Source/Drain Diffusion Length for Shallow Trench Isolation (STI) Technologies

The diffusion length, $L_{\rm od}$ between MOSFET gate and STI edge affects the MOSFET characteristics. The influence is observed mainly in $V_{\rm th}$ and in the saturation current. The $V_{\rm th}$ change is attributed to a change of the pocket impurity concentration and modeled as

$$N_{\rm substi} = \frac{1 + T1 \cdot T2}{1 + T1 \cdot T3} \tag{93}$$

where

$$\begin{aligned} T1 &= \frac{1}{1 + \mathbf{NSUBPSTI2}} \\ T2 &= \frac{\mathbf{NSUBPSTI1}}{L_{\rm od_half}}^{\mathbf{NSUBPSTI3}} \\ T3 &= \frac{\mathbf{NSUBPSTI1}}{L_{\rm od_half_ref}}^{\mathbf{NSUBPSTI3}} \end{aligned} \tag{94}$$

which is used to modify the pocket concentration $N_{\rm subp}$ as

$$N_{\rm subp} = N_{\rm subp} \cdot N_{\rm substi}. \tag{95}$$

The saturation-current change is attributed to a change of the mobility and modeled as

$$M_{\rm uesti} = \frac{1 + T1 \cdot T2}{1 + T1 \cdot T3} \tag{96}$$

where

$$\begin{aligned} T1 &= \frac{1}{1 + \mathbf{MUESTI2}} \\ T2 &= \frac{\mathbf{MUESTI1}}{L_{\rm od_half}}^{\mathbf{MUESTI3}} \\ T3 &= \frac{\mathbf{MUESTI1}}{L_{\rm od_half_eff}}^{\mathbf{MUESTI3}} \end{aligned} \tag{97}$$

which is used to modify the phonon mobility parameter $M_{\rm uephonon}$ as

$$M_{\rm uephonon} = M_{\rm uephonon} \cdot M_{\rm uesti} \tag{98}$$

where $L_{\rm od_half}$ and $L_{\rm od_half_eff}$ are determined in the same way as BSIM4.6.0 with model parameters **SAREF** and **SBREF** and instance parameters **SA**, **SB**, and **SD**.

The HiSIM model parameters introduced in section 13 are summarized in Table 12.

Table 12: HiSIM model parameters introduced in section 13 of this manual. # indicates instance parameters.

Parameter	Description
NSUBPSTI1	pocket concentration change due to diffusion-region length between gate and STI
NSUBPSTI2	pocket concentration change due to diffusion-region length between gate and STI
NSUBPSTI3	pocket concentration change due to diffusion-region length between gate and STI
MUESTI1	mobility change due to diffusion-region length between gate and STI
MUESTI2	mobility change due to diffusion-region length between gate and STI
MUESTI3	mobility change due to diffusion-region length between gate and STI
SAREF	length of diffusion between gate and STI
SBREF	length of diffusion between gate and STI
#**SA**	length of diffusion between gate and STI
#**SB**	length of diffusion between gate and STI
#**SD**	length of diffusion between gate and gate

14 Temperature Dependences

In HiSIM_HV **TEMP** is treated as a simulation option, and temperature $T0$ is determined as

$$T0 = \mathbf{TEMP} + \mathbf{DTEMP} \tag{99}$$

where **DTEMP** is an instance parameter describing the temperature increase from **TEMP**, thus $T0$ is the given temperature. Whereas the temperature including the self heating effect is distinguished by T

$$T = T0 + \delta T \tag{100}$$

where δT is the temperature increase by the self-heating effect. The temperature dependence is included automatically in the surface potentials through β, which is the inverse of the thermal voltage. Additionally the bandgap, the intrinsic carrier concentration, the carrier mobility, and the carrier saturation velocity are also temperature dependent. The temperature dependence of the bandgap determines the temperature dependence of $V_{\rm th}$ [32] and is modeled as

$$E_{\rm g} = E_{\rm gnom} - \mathbf{BGTMP1} \cdot (T - \mathbf{TNOM}) - \mathbf{BGTMP2} \cdot (T - \mathbf{TNOM})^2 \tag{101}$$

$$E_{\rm gnom} = \mathbf{EG0} - 90.25 \cdot 10^{-6} \cdot \mathbf{TNOM} - 1.0 \cdot 10^{-7} \cdot \mathbf{TNOM}^2 \tag{102}$$

where T is the given temperature. The temperature dependence of the intrinsic carrier concentration is given by

$$n_{\rm i} = n_{\rm i0} \cdot T^{\frac{3}{2}} \cdot \exp\left(-\frac{E_{\rm g}}{2q}\beta\right) \tag{103}$$

The temperature dependence of the mobility and the temperature dependence of the saturation velocity have a major influence on the temperature dependence of the $I_{\rm ds}$-$V_{\rm ds}$ characteristics under the on-current condition. They are modeled as [26]:

$$\mu_{\rm PH}(\text{phonon}) = \frac{M_{\rm uephonon}}{(T/\mathbf{TNOM})^{\mathbf{MUETMP}} \cdot E_{\rm eff}^{\mathbf{MUEPH0}}} \tag{104}$$

$$V_{\rm max} = \frac{\mathbf{VMAX}}{1.8 + 0.4(T/\mathbf{TNOM}) + 0.1(T/\mathbf{TNOM})^2 - \mathbf{VTMP} \cdot (1 - T/\mathbf{TNOM})} \tag{105}$$

The temperature dependence of the gate current is modeled by modifying the bandgap specific for the gate current as

$$E_{\rm gp} = E_{\rm g0} + \mathbf{EGIG} + \mathbf{IGTEMP2}\left(\frac{1}{T} - \frac{1}{\mathbf{TNOM}}\right) + \mathbf{IGTEMP3}\left(\frac{1}{T^2} - \frac{1}{\mathbf{TNOM}^2}\right) \tag{106}$$

where $E_{\rm g0}$ is the bandgap at **TNOM**.

Junction Capacitance at Drain Side:

$$\mathbf{CJ} = \mathbf{CJ} \cdot (1 + \mathbf{TCJBD} \cdot (T - \mathbf{TNOM})) \tag{107}$$

$$\mathbf{CJSW} = \mathbf{CJSW} \cdot (1 + \mathbf{TCJBDSW} \cdot (T - \mathbf{TNOM})) \tag{108}$$

$$\mathbf{CJSWG} = \mathbf{CJSWG} \cdot (1 + \mathbf{TCJBDSWG} \cdot (T - \mathbf{TNOM})) \tag{109}$$

Junction Capacitance at Source Side:

$$\mathbf{CJ} = \mathbf{CJ} \cdot (1 + \mathbf{TCJBS} \cdot (T - \mathbf{TNOM})) \tag{110}$$

$$\mathbf{CJSW} = \mathbf{CJSW} \cdot (1 + \mathbf{TCJBSSW} \cdot (T - \mathbf{TNOM})) \tag{111}$$

$$\mathbf{CJSWG} = \mathbf{CJSWG} \cdot (1 + \mathbf{TCJBSSWG} \cdot (T - \mathbf{TNOM})) \tag{112}$$

Junction Current:

$$T_{\mathrm{tnom}} = \frac{T}{\mathbf{TNOM}} \tag{113}$$

$$j_{\mathrm{s}} = \mathbf{JS0} \exp\left\{\frac{(E_{\mathrm{g}}(T = \mathbf{TNOM}) \cdot \beta(T = \mathbf{TNOM}) - E_{\mathrm{g}}\beta + \mathbf{XTI} \cdot \log(T_{\mathrm{tnom}}))}{\mathbf{NJ}}\right\} \tag{114}$$

$$j_{\mathrm{ssw}} = \mathbf{JS0SW} \exp\left\{\frac{(E_{\mathrm{g}}(T = \mathbf{TNOM}) \cdot \beta(T = \mathbf{TNOM}) - E_{\mathrm{g}}\beta + \mathbf{XTI} \cdot \log(T_{\mathrm{tnom}}))}{\mathbf{NJSW}}\right\} \tag{115}$$

$$j_{\mathrm{s2}} = \mathbf{JS0} \exp\left\{\frac{(E_{\mathrm{g}}(T = \mathbf{TNOM}) \cdot \beta(T = \mathbf{TNOM}) - E_{\mathrm{g}}\beta + \mathbf{XTI2} \cdot \log(T_{\mathrm{tnom}}))}{\mathbf{NJ}}\right\} \tag{116}$$

$$j_{\mathrm{ssw2}} = \mathbf{JS0SW} \exp\left\{\frac{(E_{\mathrm{g}}(T = \mathbf{TNOM}) \cdot \beta(T = \mathbf{TNOM}) - E_{\mathrm{g}}\beta + \mathbf{XTI2} \cdot \log(T_{\mathrm{tnom}}))}{\mathbf{NJSW}}\right\} \tag{117}$$

$$\mathbf{CISB} = \mathbf{CISB} \cdot \exp\{(T_{\mathrm{tnom}} - 1)\mathbf{CTEMP}\} \tag{118}$$

$$\mathbf{VDIFFJ} = \mathbf{VDIFFJ} \cdot (T_{\mathrm{tnom}})^2 \tag{119}$$

In addition to the temperature dependence of the physical quantities considered, resistances include the temperature dependence, which is modeled with the given temperature to avoid complication in parameter extraction.

CORDRIFT=1: default

$$\mu_{\mathrm{drift0,temp}} = \frac{\mathbf{RDRMUE}}{(T/\mathbf{TNOM})^{\mathbf{RDRMUETMP}}} \tag{120}$$

$$V_{\mathrm{max_drift,temp}} = \frac{\mathbf{RDRVMAX}}{1.8 + 0.4(T/\mathbf{TNOM}) + 0.1(T/\mathbf{TNOM})^2 - \mathbf{RDRVTMP} \cdot (1 - T/\mathbf{TNOM})} \tag{121}$$

CORDRIFT=0: old model

$$R_{\mathrm{d0,temp}} = \mathbf{RDTEMP1} \cdot (T0 - \mathbf{TNOM}) + \mathbf{RDTEMP2} \cdot (T0^2 - \mathbf{TNOM}^2) \tag{122}$$

$$R_{\mathrm{dvd,temp}} = \mathbf{RDVDTEMP1} \cdot (T0 - \mathbf{TNOM}) + \mathbf{RDVDTEMP2} \cdot (T0^2 - \mathbf{TNOM}^2) \tag{123}$$

Additional temperature dependences are also included with the given temperature in case they are needed.

$$V_{\max} = \mathbf{VMAX} \cdot \left(1 + \mathbf{VMAXT1} \cdot (T0 - \mathbf{TNOM}) + \mathbf{VMAXT2} \cdot (T0^2 - \mathbf{TNOM}^2\right) \tag{124}$$

$$N_{\mathrm{invd}} = N_{\mathrm{invd}} \cdot \left(1 + \mathbf{NINVDT1} \cdot (T0 - \mathbf{TNOM}) + \mathbf{NINVDT2} \cdot (T0^2 - \mathbf{TNOM}^2\right) \tag{125}$$

where $T0$ in the above four equations can be replaced by T including the temperature increase due to the self-heating effect by selecting Flag **COTEMP** (see in section 23).

The HiSIM model parameters introduced in section 14 are summarized in Table 13.

Table 13: HiSIM model parameters introduced in section 14 of this manual. ∗ indicates minor parameters. # indicates an instance parameter.

Parameter	Description
EG0	bandgap
BGTMP1	temperature dependence of bandgap
BGTMP2	temperature dependence of bandgap
MUETMP	temperature dependence of phonon scattering
TNOM	temperature selected as nominal temperature value
#DTEMP	temperature increase from the given temperature
∗VTMP	temperature dependence of the saturation velocity
EGIG	bandgap of gate current
IGTEMP2	temperature dependence of gate current
IGTEMP3	temperature dependence of gate current
RDRMUE	field dependent mobility in the drift region for **CORDRIFT**=1
RDRMUETMP	temperature dependence of resistance for **CORDRIFT**=1
RDRVTMP	temperature dependence of resistance for **CORDRIFT**=1
RDRVMAX	saturaion velocity in the drift region for **CORDRIFT**=1
RDTEMP1	temperature dependence of resistance for **CORDRIFT**=0
RDTEMP2	temperature dependence of resistance for **CORDRIFT**=0
RDVDTEMP1	temperature dependence of resistance
RDVDTEMP2	temperature dependence of resistance
CJ	bottom junction capacitance per unit area at zero bias
CJSW	source/drain sidewall junction cap. grading coefficient per unit length at zero bias
CJSWG	source/drain sidewall junction capacitance per unit length at zero bias
TCJBD	temperature dependence of drain-side diode capacitance
TCJBDSW	temperature dependence of drain-side diode capacitance
TCJBDSWG	temperature dependence of drain-side diode capacitance
TCJBS	temperature dependence of source-side diode capacitance
TCJBSSW	temperature dependence of source-side diode capacitance
TCJBSSWG	temperature dependence of source-side diode capacitance
XTI	temperature coefficient for forward-current densities
XTI2	temperature coefficient for reverse-current densities
CTEMP	temperature coefficient of reverse currents
NINVDT1	temperature dependence of univerisal mobility model
NINVDT2	temperature dependence of univerisal mobility model
VMAXT1	temperature dependence of velocity
VMAXT2	temperature dependence of velocity

15 Resistances

Specific features of the LDMOS/HVMOS are caused by the highly resistive drift region, enabling the high-voltage application of MOSFETs.
Here the resistance model is described for the LDMOS case. For the symmetrical/asymmetrical HVMOS case, the resistance at the source side is modeled with the same equations for the drain side by fixing $V_{\rm ds}$ to zero.
The source and the drain resistances $R_{\rm s}$ and $R_{\rm d}$ are considered by voltage drops on each terminal as

$$V_{\rm gs,eff} = V_{\rm gs} - I_{\rm ds} \cdot R_{\rm s} \tag{126}$$

$$V_{\rm ds,eff} = V_{\rm ds} - I_{\rm ds} \cdot (R_{\rm s} + R_{\rm drift}) \tag{127}$$

$$V_{\rm bs,eff} = V_{\rm bs} - I_{\rm ds} \cdot R_{\rm s} \tag{128}$$

for the DC condition, where the effective voltages are referred as internal node potential $V_{\rm dp}$.
The source side resistance is written as

$$R_{\rm s} = \frac{\mathbf{RS}}{W_{\rm eff,LD} \cdot \mathbf{NF}} + \mathbf{NRS} \cdot \mathbf{RSH} \tag{129}$$

where **NRS** is an instance parameter describing the number of squares of the source diffusion, and **RSH** is its the sheet resistance of the square. The first term of the right hand side of Eq. (129) considers the resistance in the LDD region, and the second term is that in the diffusion region, which is layout dependent.
The specific feature of high-voltage MOSFETs is $R_{\rm drift}$, which sustains high breakdown voltage. HiSIM_HV 2.0.0 provides two $R_{\rm drift}$ options selected by Flag **CORDRIFT**. The resistance model of HiSIM_HV 1 is activated with **CORDRIFT**=0, and the new model added in HiSIM_HV 2 is selected by **CORDRIFT**=1. To switch off the resistance effect completely, the flag **CORDRIFT** together with that of **CORSRD** must be set to zero.
The $R_{\rm drift}$ selection is done in three functions as depicted in Fig. 15.

15.1 CORDRIFT=1: default

The model concept is schematically shown in Fig. 16, where $I_{\rm ds}$ is written in Eq. (27), and the current flowing in the drift region $I_{\rm ddp}$ is modeled

$$R_{\rm drift} = \frac{V_{\rm ddp}}{I_{\rm ddp}} + \mathbf{RSH} \cdot \mathbf{NRD} \tag{130}$$

$$I_{\rm ddp} = W_{\rm eff} \cdot X_{\rm ov} \cdot q \cdot N_{\rm drift} \cdot \mu_{\rm drift} \frac{V_{\rm ddp}}{L_{\rm drift} + \mathbf{RDRDL1}} \tag{131}$$

where

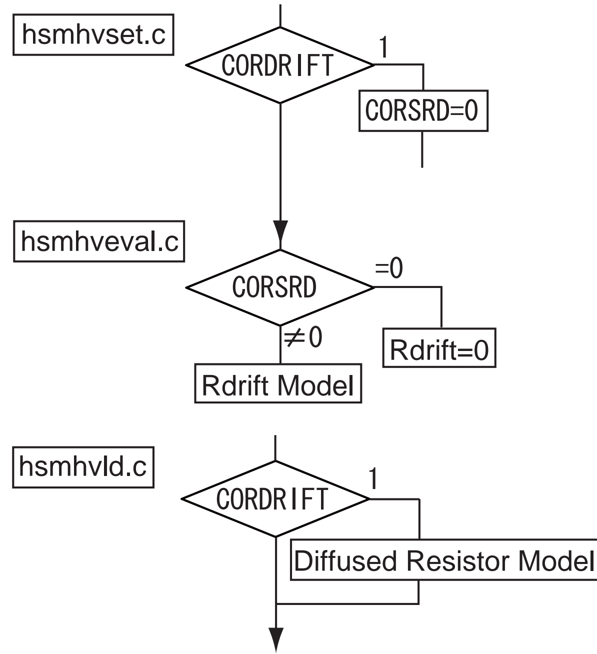

Fig. 15: Model selection done in three files.

$$L_{\rm drift} = L_{\rm drift1} + L_{\rm drift2} \tag{132}$$

$$\mu_{\rm drift} = \frac{\mu_{\rm drift0}}{\left[1 + \left(\frac{\mu_{\rm drift0}}{V_{\rm max_drift}} \cdot \frac{V_{\rm ddp}}{L_{\rm drift}}\right)^{\bf RDRBB}\right]^{\frac{1}{\bf RDRBB}}} \tag{133}$$

$$\mu_{\rm drift0} = \mu_{\rm drift0,temp} \left(1 + \frac{\bf RDRMUEL}{(L_{\rm gate} \cdot 10^6)^{\bf RDRMUELP}}\right) \tag{134}$$

$$V_{\rm max_drift} = V_{\rm max_drift,temp} \left(1 + \frac{\bf RDRVMAXL}{(L_{\rm gate} \cdot 10^6)^{\bf RDRVMAXLP}}\right) \left(1 + \frac{\bf RDRVMAXW}{(W_{\rm gate} \cdot 10^6)^{\bf RDRVMAXWP}}\right) \tag{135}$$

$$X_{\rm ov} = W_0 - \mathbf{RDRCX} \cdot \left(\frac{W_0}{\mathbf{RDRDJUNC}} W_{\rm dep} + \frac{W_0}{\mathbf{XLDLD}} W_{\rm junc} \right) \tag{136}$$

$$W_0 = \sqrt{\mathbf{XLDLD}^2 + \mathbf{RDRDJUNC}^2} \tag{137}$$

$$W_{\rm dep} = \sqrt{\frac{2\epsilon_{\rm Si} \left(-\phi_{\rm s,over}\right)}{q \cdot \mathbf{NOVER}}} \tag{138}$$

$$W_{\rm junc} = \sqrt{\frac{2\epsilon_{\rm Si} \left(V_{\rm dps} - V_{\rm bs} + V_{\rm bi}\right)}{q} \cdot \frac{N_{\rm sub}}{\mathbf{NOVER} \left(N_{\rm sub} + \mathbf{NOVER}\right)}} \tag{139}$$

$$N_{\rm drift} = \mathbf{NOVER} \left\{ 1 + \mathbf{RDRCAR} \left(\frac{V_{\rm ddp}}{L_{\rm drft} - \mathbf{RDRDL2}} \right) \left(1 - \frac{1}{1 + \frac{\mu_{\rm drift0}}{V_{\rm max_drift}} \cdot \frac{V_{\rm ddp}}{L_{\rm drift}}} \right) \right\} + \left(\mathbf{RDRQOVER} \frac{-Q_{\rm over}}{q} \right) \tag{140}$$

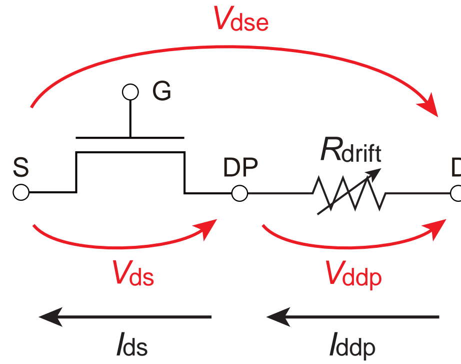

Fig. 16: Model concept.

The potential value of $V_{\rm ddp}$, the difference between the internal node DP and the drain node is calculated by circuit simulator.

15.2 CORDRIFT=0: old model provided in HiSIM_HV 1

The voltage drops are in principle calculated iteratively for applied voltages to keep consistency among all device performances. However, a simple analytical description is also provided. Thus, the parasitic source and drain resistances, $R_{\rm s}$ and $R_{\rm drift}$, can be considered by different optional approaches. Flag **CORSRD** is provided for the selection of one of the possible approaches. **CORSRD** = 0, 1, 2, 3 means "no resistance", "external", "analytical", "external + analytical", respectively. Options to be selected by Flag **CORSRD** are summarized in Fig. 17.

In the HiSIM_HV 1.0.2 version, the option **CORSRD=-1** was provided as an option by introducing an internal node additionally. To keep backward compatible for such case, **CORSRD**=1 must be selected and bias independent resistance parameters, **RS** and **RD**, can be used.

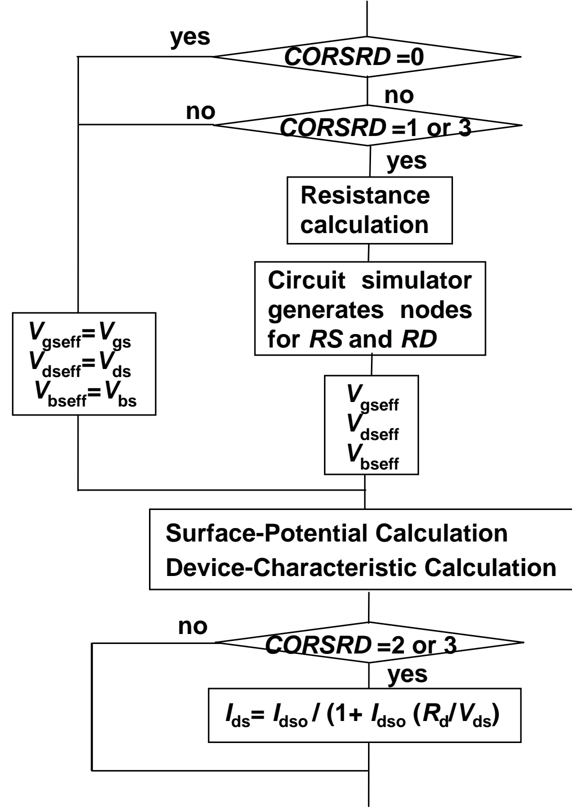

Fig. 17: Model options provided in HiSIM-LDMOS/HV for the resistance models, which are selected by Flag **CORSRD**.

CORSRD=2 considered only the resistance effect on the drain current as

$$I_{\rm ds} = \frac{I_{\rm ds0}}{1 + I_{\rm ds0}\frac{R_{\rm d}}{V_{\rm ds}}} \tag{141}$$

where $I_{\rm ds0}$ is the drain current without the resistance effect and

$$R_{\rm d} = \frac{1}{W_{\rm eff}}\left(R'_{\rm d} \cdot V_{\rm ds}^{\mathbf{RD21}} + V_{\rm bs} \cdot V_{\rm ds}^{\mathbf{RD22D}} \cdot \mathbf{RD22}\right) \tag{142}$$

$$RD23' \leq R'_{\rm d} \leq RD23'(1 + \mathbf{RD20}) \tag{143}$$

where

$$RD23' = \mathbf{RD23} \cdot \exp\left(-\mathbf{RD23L} \cdot (L_{\rm gate} \cdot 10^6)^{\mathbf{RD23LP}}\right)\left(1 + \frac{\mathbf{RD23S}}{(W_{\rm gate} \cdot 10^6 \cdot L_{\rm gate} \cdot 10^6)^{\mathbf{RD23SP}}}\right) \tag{144}$$

The $V_{\rm gs}$ dependence of $R'_{\rm d}$ is considered

$$R'_{\rm d} = \mathbf{RD24}\,(V_{\rm gs} - \mathbf{RD25}) \tag{145}$$

The resistance effect for the case **CORSRD**=1 is described here. However, in case if it is necessary, both

resistance models (internal-node approach and anlytical approach) can be applied with **CORSRD**=3.

$$R_{\rm drift} = (R_{\rm d} + V_{\rm ds} \cdot R_{\rm DVD}) \left(1 + \mathbf{RDVG11} - \frac{\mathbf{RDVG11}}{\mathbf{RDVG12}} \cdot V_{\rm gs}\right) \cdot (1 - V_{\rm bs} \cdot \mathbf{RDVB}) \tag{146}$$

$$\cdot \left(\frac{\mathbf{LDRIFT1} + \mathbf{LDRIFT2}}{\mathbf{DDRIFT} - W_{\rm dep}}\right) \tag{147}$$

and

$$R_{\rm d} = \frac{R_{\rm d0}}{W_{\rm eff,LD} \cdot \mathbf{NF}} \left(1 + \frac{\mathbf{RDS}}{(W_{\rm gate} \cdot 10^6 \cdot L_{\rm gate} \cdot 10^6)^{\mathbf{RDSP}}}\right) \tag{148}$$

$$R_{\rm d0} = (\mathbf{RD} + R_{\rm d0,temp})\, f_1 \cdot f_2 \tag{149}$$

$$R_{\rm DVD} = \frac{\mathbf{RDVD} + R_{\rm dvd,temp}}{W_{\rm eff}} \cdot \exp\left(-\mathbf{RDVDL} \cdot (L_{\rm gate} \cdot 10^6)^{\mathbf{RDVDLP}}\right) \cdot \left(1 + \frac{\mathbf{RDVDS}}{(W_{\rm gate} \cdot 10^6 \cdot L_{\rm gate} \cdot 10^6)^{\mathbf{RDVDSP}}}\right) \cdot f_1 \cdot f_2 \cdot f_3 \tag{150}$$

$$f_1(L_{\rm drift1}) = \frac{\mathbf{LDRIFT1}}{1\mu m} \cdot \mathbf{RDSLP1} + \mathbf{RDICT1} \tag{151}$$

$$f_2(L_{\rm drift2}) = \frac{\mathbf{LDRIFT2}}{1\mu m} \cdot \mathbf{RDSLP2} + \mathbf{RDICT2} \tag{152}$$

$$f_3(L_{\rm over})^* = 1 + \left(\mathbf{RDOV11} - \frac{\mathbf{RDOV11}}{\mathbf{RDOV12}}\right) \cdot \frac{\mathbf{LOVERLD}}{1\mu m} + (1 - \mathbf{RDOV13}) \cdot \frac{\mathbf{LOVERLD}}{1\mu m} \tag{153}$$

$$W_{\rm dep} = \sqrt{\frac{2\epsilon_{\rm Si}\{\mathbf{VBISUB} - (\mathbf{RDVDSUB} \cdot V_{\rm ds} + \mathbf{RDVSUB} \cdot V_{\rm sub,s})\}}{q}} \cdot \sqrt{\frac{\mathbf{NSUBSUB}}{\mathbf{NOVER} \cdot (\mathbf{NSUBSUB} + \mathbf{NOVER})}} \tag{154}$$

LDRIFT1 and **LDRIFT2** are model parameters denoting lengths of different parts of the drift region. The source resistance in the LDMOS case does not consider a drift region and has therefore no drift length parameters. It is expected that either the second term of Eq. (153) or the third term is selected. For HiSIM_HV1.0 versions, **RDOV13** must be fixed to unity to select the second term. To select the third term **RDOV11** must be zero.
In the present and previous versions Eq. (153) is written as

$$f_3(L_{\rm over})^* = 1 + \mathbf{RDOV11} - \frac{\mathbf{RDOV11}}{\mathbf{RDOV12}} \cdot \frac{\mathbf{LOVERLD}}{1\mu m} + (1 - \mathbf{RDOV13}) \cdot \frac{\mathbf{LOVERLD}}{1\mu m} \tag{155}$$

by mistake.

The final drift resistance $R_{\rm drift}$ is written as

$$R_{\rm drift} = R_{\rm drift} + \mathbf{RSH} \cdot \mathbf{NRD} \tag{156}$$

where **NRD** is an instance parameter describing the number of squares of the drain diffusion, and **RSH** is its the sheet resistance of the square. The first terms of the right hand side of the equation considers

the resistance in the drift region, and the second term is the that in the diffusion region, which are layout dependent.

The gate resistance becomes large as the gate width becomes large, which is the case for many RF circuits. The equation for the gate-resistance calculation is taken from the BSIM4 [33] description as

$$R_\mathrm{g} = \frac{\mathbf{RSHG} \cdot \left(\mathbf{XGW} + \frac{W_\mathrm{eff}}{3 \cdot \mathbf{NGCON}}\right)}{\mathbf{NGCON} \cdot (L_\mathrm{drawn} - \mathbf{XGL}) \cdot \mathbf{NF}} \tag{157}$$

where **RSHG** is the gate sheet resistance, and others are instance parameters dependent on the layout. The flag **CORG** is provided for the inclusion of gate resistance. **CORG** = 0,1 means "no", "external" gate resistance, respectively.
Model parameters for the same substrate resistance network as BSIM4 (**RBPB**, **RBPD**, **RBPS**) are included in the model parameter list, which are also treated as instance parameters.

Here summarizes the selection of the resistance model for **CORDRIFT** = 0:
CORSRD = 0 : no resistance
CORSRD = 1 : solved by circuit siumlator with external nodes
All model parameters included in Eq. (129)–Eq. (154) are used.
Model parameters are:
RS, **NRS**, **RSH**
RDVG11, **RDVG12**, **RDVB**, **RDS**, **RDSP**, **NRD**
RD, **RDVD**, **RDVDL**, **RDVDLP**, **RDVDS**, **RDVDSP**
RDSLP1, **RDICT1**, **RDSLP2**, **RDICT2**, **RDOV11**, **RDOV12**, **RDOV13**
RDVDSUB, **RDVSUB**, **VBISUB**, **DDRIFT**, **NSUBSUB**
CORSRD = 2 : solved with the analytical equations of Eq. (141)–Eq. (145)
Model parameters are:
RD21, **RD22**, **RD22D**, **RD23**, **RD23L**, **RD23LP**
RD23S, **RD23SP**, **RD24**, **RD25**, **RD20**
CORSRD = 3 : Both **CORSRD** = 1 and **CORSRD** = 2 are considered.

At the starting of the parameter extraction, following model parameters are suggested to set to zero:
RDVG11, **RDVB**, **RDVD**
RDTEMP1, **RDTEMP2**, **RDVDTEMP1**, **RDVDTEMP2**
The above condition refers to the bias independent resistance.
Table 14 summaizes the minimum resistance parameters to be determined.

Table 14: HiSIM_HV 1.2.0 resistance parameters introduced. If **RS** is not determined for the asymmetrical case, **RD** is taken.

	structure	source	drain
COSYM=0	**LDMOS**	**RS**(bias independent)	**RD**
COSYM=1	**symmetrical HVMOS**		**RD**
COSYM=1	**asymmetrical HVMOS**	**RS**	**RD**

The HiSIM model parameters introduced in section 15 are summarized in Table 15.

Table 15: HiSIM model parameters introduced in section 15 of this manual. # indicates instance parameters. ∗ indicates minor parameters.

RS	source-contact resistance of LDD region
RSH	source/drain sheet resistance of diffusion region
RSHG	gate sheet resistance
RBPB	substrate resistance network
RBPD	substrate resistance network
RBPS	substrate resistance network
RBDB	no more used
RBSB	no more used
#**NRS**	number of source squares
#**NRD**	number of drain squares
#**XGW**	distance from the gate contact to the channel edge
#**XGL**	offset of the gate length
#**NF**	number of fingers
#**NGCON**	number of gate contacts
CORDRIFT=1	
RDRDL1	effective L_{drift} of current in drift region
RDRDL2	pinch-off length in drift region
RDRCX	exude of current flow from X_{ov}
RDRCAR	high field injection in drift region
RDRDJUNC	junction depth at channel/drift region
RDRBB	high field mobility in drift region
RDRMUE	mobility in drift region
RDRVMAX	saturation velocity in drift region
RDRVMAXL	saturation velocity L_{gate} dependence
RDRVMAXLP	saturation velocity L_{gate} dependence
RDRVMAXW	saturation velocity W_{gate} dependence
RDRVMAXWP	saturation velocity W_{gate} dependence
RDRMUEL	mobility in drift region L_{gate} dependence
RDRMUELP	moblity in drift region L_{gate} dependence
RDRLOWVD1	modification of R_{drift} for small V_{ds}
RDRLOWVD2	modification of R_{drift} for small V_{ds}
RDRQOVER	inclusion of the overlap charge into R_{drift}
CORDRIFT=0	
RD	drain-contact resistance of LDD region
***RDVG11**	V_{gs} dependence of **RD** for **CORSRD**=1,3
***RDVG12**	V_{gs} dependence of **RD** for **CORSRD**=1,3
RDVD	V_{ds} dependence of **RD** for **CORSRD**=1,3
RDVB	V_{bs} dependence of **RD** for **CORSRD**=1,3
***RDS**	small size dependence of **RD** for **CORSRD**=1,3
***RDSP**	small size depenence of **RD** for **CORSRD**=1,3
***RDVDL**	L_{gate} dependence of **RD** for **CORSRD**=1,3
***RDVDLP**	L_{gate} dependence of **RD** for **CORSRD**=1,3
***RDVDS**	small size dependence of **RD** for **CORSRD**=1,3
***RDVDSP**	small size dependence of **RD** for **CORSRD**=1,3
RDOV11	L_{over} dependence of resistance for **CORSRD**=1,3
RDOV12	L_{over} dependence of resistance for **CORSRD**=1,3
RDOV13	alternative L_{over} dependence model for **CORSRD**=1,3
RDSLP1	**LDRIFT1** dependence of resistances for **CORSRD**=1,3
RDICT1	**LDRIFT1** dependence of resistances for **CORSRD**=1,3
RDSLP2	**LDRIFT2** dependence of resistances for **CORSRD**=1,3
RDICT2	**LDRIFT2** dependence of resistances for **CORSRD**=1,3
RD20	**RD23** boundary for **CORSRD**=2,3
RD21	V_{ds} dependence of **RD** for **CORSRD**=2,3
RD22	V_{bs} dependence of **RD** for **CORSRD**=2,3
RD22D	V_{bs} dependence of **RD** for **CORSRD**=2,3 with large V_{ds}

RD23	modification of **RD** for **CORSRD**=2,3
***RD23L**	L_{gate} dependence of **RD23** boundary for **CORSRD**=2,3
***RD23LP**	L_{gate} dependence of **RD23** boundary for **CORSRD**=2,3
***RD23S**	small size dependence of **RD23** for **CORSRD**=2,3
***RD23SP**	small size dependence of **RD23** for **CORSRD**=2,3
***RD24**	V_{gs} dependence of **RD** for **CORSRD**=2,3
***RD25**	V_{gs} dependence of **RD** for **CORSRD**=2,3
VBISUB	built-in potential at the drift/substrate junction
RDVDSUB	V_{ds} dependence of depletion width
RDVSUB	V_{sub} dependence of depletion width
DDRIFT	depth of the drift region
NSUBSUB	impurity concentration of the substrate required for V_{sub} dependence

16 Capacitances

16.1 Intrinsic Capacitances

The intrinsic capacitances are derivatives of the node charges determined as

$$\begin{aligned} C_{jk} &= \delta \frac{\partial Q_j}{\partial V_k} \\ \delta = -1 &\quad \text{for} \quad j \neq k \\ \delta = \;\; 1 &\quad \text{for} \quad j = k \end{aligned} \tag{158}$$

HiSIM uses analytical solutions for all 9 independent intrinsic capacitances, derived from the charges as explicit functions of the surface potentials. Therefore, there are no extra model parameters for the intrinsic capacitances except the width reduction parameter **XWDC** different from that of current **XWD**, namely $W_{\rm effc}$ for the total capacitance calculation instead of $W_{\rm eff}$, if it is necessary.
The lateral electric field along the channel induces a capacitance C_{Q_y} which significantly affects the gate capacitance in saturation [34]. The induced charge associated with C_{Q_y} is described with the surface potential values as

$$Q_y = \epsilon_{\rm Si} W_{\rm eff} \cdot \mathbf{NF} W_{\rm d} \left(\frac{\phi_{\rm S0} + V_{\rm ds} - \phi_{\rm S}(\Delta L)}{\mathbf{XQY}} \right) + \frac{\mathbf{XQY1}}{L_{\rm gate}^{\mathbf{XQY2}}} V_{\rm bs} \tag{159}$$

introducing **XQY**, a parameter determining the maximum field at the channel/drain junction independent of $L_{\rm gate}$. For **XQY**=0 the charge $Q_{\rm y}$ is fixed to zero.

16.2 Overlap Capacitances

The overlap capacitance includes three options as summarized in Fig. 18 for the drain side and Fig. 19 for the source side. If Flags **COOVLP**=**COOVLPS**=0, the overlap capacitances are treated to be constant. If **CGSO** and **CGDO** are determined, these values are taken. If they are not determined, the values are calculated with the overlap length and oxide capacitance.
If Flags **COOVLP**=**COOVLPS**=1, the bias dependent overlap capacitances are considered. Here two models are provided: One is the surface-potential-based model and the other describes with a simple $V_{\rm gs}$ dependence. In addition to the bias dependent capacitances, **CGSO** and **CGDO** can be also added, if they are determined.

The description is focussed on the drain side. For the source side the same calculation is performed with $V_{\rm ds}$=0.
i) Surface-Potential-Based Model
The surface potential $\phi_{\rm S}$ is calculated in the same manner as in the channel region, and only the polarity is inverted from the channel. The final overlap charge equation is written with the calculated $\phi_{\rm S}$

a) under the depletion and the accumulation conditions

$$Q_{\rm over} = W_{\rm eff} \cdot \mathbf{NF} \cdot \mathbf{LOVERLD} \left(\sqrt{\frac{2\epsilon_{\rm Si} q \mathbf{NOVER}}{\beta}} \sqrt{\beta(\phi_{\rm S} + V_{\rm ds}) - 1} \right) \tag{160}$$

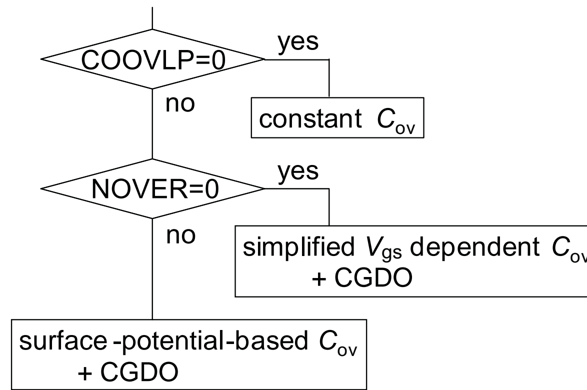

Fig. 18: Model options of the overlap capacitance at the drain side are summarized.

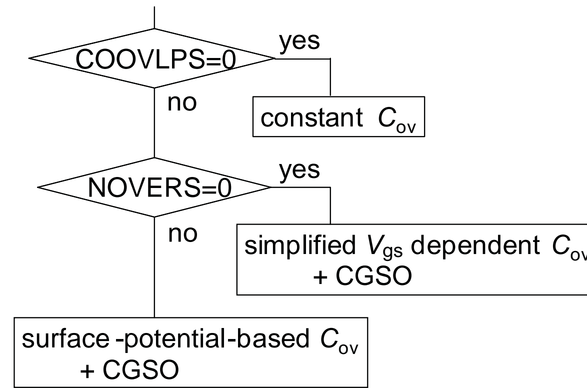

Fig. 19: Model options of the overlap capacitance at the soruce side are summarized.

b) under the inversion condition

$$Q_{\rm over} = W_{\rm eff} \cdot \mathbf{NF} \cdot \mathbf{LOVERLD} \cdot C_{\rm ox}(V_{\rm gs} - \mathbf{VFBOVER} - \phi_{\rm S}) \tag{161}$$

where **LOVERLD** is the length of the overlap region of the gate over drain, **NOVER** is the impurity concentration in the drift region, and **VFBOVER** is the flat-band voltage in the overlap region. This model is selected, if **NOVER** is not equal to zero.
The potential distribution occurs in the drain side of the drift region underneath the gate overlap before the strong inversion is created. This induces additional charge and the overlap capacitance at the same time. This effect is modeled as

$$Q_{\rm over,d} = Q_{\rm over,d} + W_{\rm eff} \cdot \mathbf{NF} \cdot \mathbf{QOVADD} \cdot \mathbf{LOVERLD} \cdot (V_{\rm dp} - V_{\rm ch}) \tag{162}$$

$$V_{\rm ch} = \phi_{\rm SL} - \phi_{\rm S0} \tag{163}$$

Three options are provided to calculate ϕ_s, which is selected by the flag **COQOVSM**:

COQOVSM=0: with an analytical equation excluding inversion charge

COQOVSM=1: with iterative procedure

COQOVSM=2: with an analytical equation including inversion charge

The potential value not only at the internal channel/drift junction but also that at the external node can be considered for the overlap capacitance calculation. The model parameter **CVDSOVER** has been introduced to determine the ratio of these two potential contributions as

$$C_{\text{ov}} = (1 - \mathbf{CVDSOVER}) \cdot C_{\text{ov}}(int) + \mathbf{CVDSOVER} \cdot C_{\text{ov}}(ext) \tag{164}$$

where $C_{\text{ov}}(int)$ is the overlap capacitance value calculated with the potential value at the channel/drift junction and $C_{\text{ov}}(ext)$ is that with the external potential value. Spikes observed in C_{gg} for $V_{\text{ds}} \neq 0$ are determined automatically by the resistance, which is extracted with $I - V$ characteristics. These spickes can be adjusted to measurements by **CVDSOVER** without influencing the calculated $I - V$ characteristics.

ii) Simplified Bias-Dependent Model

If **LOVERLD** > 0 and the flag **COOVLP** $= 1$, the overlap charge is modeled as

$$Q_{\text{god}} = W_{\text{eff}} \cdot \mathbf{NF} \cdot C_{\text{ox}} \left[(V_{\text{gs}} - V_{\text{ds}})\mathbf{LOVERLD} - \mathbf{OVSLP} \cdot (1.2 - (\phi_{\text{SL}} - V_{\text{ds}})) \cdot (\mathbf{OVMAG} + (V_{\text{gs}} - V_{\text{ds}})) \right] \tag{165}$$

The overlap capacitance Flags (**COOVLP** = **COOVLPS** = 0) calculates bias-independent overlap capacitances. User-defined values can be specified using the input parameters **CGDO** and **CGSO**. If these values are not specified, the overlap capacitances are calculated using

$$C_{\text{ov}} = -\frac{\epsilon_{\text{ox}}}{\mathbf{TOX}} \mathbf{LOVERLD} \cdot W_{\text{eff}} \cdot \mathbf{NF} \tag{166}$$

The gate-to-bulk overlap capacitance $C_{\text{gbo_loc}}$ is calculated only with a user-defined value **CGBO** using

$$C_{\text{gbo_loc}} = -\mathbf{CGBO} \cdot L_{\text{gate}} \tag{167}$$

independent of the model Flags **COOVLP** and **COOVLPS**.

16.3 Extrinsic Capacitances

The outer fringing capacitance is modeled as [36]

$$C_{\text{f}} = \frac{\epsilon_{\text{ox}}}{\pi/2} W_{\text{gate}} \cdot \mathbf{NF} \cdot \ln\left(1 + \frac{\mathbf{TPOLY}}{T_{\text{ox}}}\right) \tag{168}$$

where **TPOLY** is the gate-poly thickness. This capacitance is bias independent.

The HiSIM model parameters introduced in section 16 are summarized in Table 16.

Table 16: HiSIM model parameters introduced in section 16 of this manual.

Parameter	Description
XQY	distance from drain junction to maximum electric field point
***XQY1**	$V_{\rm bs}$ dependence of $Q_{\rm y}$
***XQY2**	$L_{\rm gate}$ dependence of $Q_{\rm y}$
LOVERLD	overlap length of the drift region
LOVERS	overlap length of the source region
LOVER	overlap length of the source region, if **LOVERS** is not determined.
VFBOVER	flat-band voltage in overlap region
***QOVADD**	additional overlap capacitance
***CVDSOVER**	modification of the $C_{\rm gg}$ spikes for $V_{\rm ds} \neq 0$
OVSLP	coefficient for overlap capacitance
OVMAG	coefficient for overlap capacitance
CGSO	gate-to-source overlap capacitance
CGDO	gate-to-drain overlap capacitance
CGBO	gate-to-bulk overlap capacitance
TPOLY	height of the gate poly-Si

17 Leakage Currents

17.1 Substrate Current

The substrate current is modeled as

$$I_{\rm sub} = X_{\rm sub1} \cdot P_{\rm sisubsat} \cdot I_{\rm ds} \cdot \exp\left(-\frac{X_{\rm sub2}}{P_{\rm sisubsat}}\right) \tag{169}$$

where

$$X_{\rm sub1} = \mathbf{SUB1} \cdot \left(1 + \frac{\mathbf{SUB1L}}{L_{\rm gate}^{\mathbf{SUB1LP}}}\right) \tag{170}$$

$$X_{\rm sub2} = \mathbf{SUB2} \cdot \left(1 + \frac{\mathbf{SUB2L}}{L_{\rm gate}}\right) \tag{171}$$

$$P_{\rm sisubsat} = \mathbf{SVDS} \cdot V_{\rm ds} + \phi_{\rm S0} - \frac{L_{\rm gate} \cdot P_{\rm sislsat}}{X_{\rm gate} + L_{\rm gate}} \tag{172}$$

$$X_{\rm gate} = \mathbf{SLG} \cdot \left(1 + \frac{\mathbf{SLGL}}{L_{\rm gate}^{\mathbf{SLGLP}}}\right) \tag{173}$$

$$P_{\rm sislsat} = V_{\rm g2} + \frac{q \cdot \epsilon_{\rm Si} \cdot N_{\rm sub}}{C_{\rm ox}^2} \cdot \left\{1 - \sqrt{1 + \frac{2C_{\rm ox}^2}{q \cdot \epsilon_{\rm Si} \cdot N_{\rm sub}} \cdot \left(V_{\rm g2} - \frac{1}{\beta} - X_{\rm vbs} \cdot V_{\rm bs}\right)}\right\} \tag{174}$$

$$X_{\rm vbs} = \mathbf{SVBS} \cdot \left(1 + \frac{\mathbf{SVBSL}}{L_{\rm gate}^{\mathbf{SVBSLP}}}\right) \tag{175}$$

$$V_{\rm g2} = \mathbf{SVGS} \cdot \left(1 + \frac{\mathbf{SVGSL}}{L_{\rm gate}^{\mathbf{SVGSLP}}}\right) \cdot \frac{W_{\rm gate}^{\mathbf{SVGSWP}}}{W_{\rm gate}^{\mathbf{SVGSWP}} + \mathbf{SVGSW}} \cdot V_{\rm gp} \tag{176}$$

17.1.1 Impact-Ionization Induced Bulk Potential Change

The impact ionization induces electron and hole pairs, which is the origin of the substrate current. However, not only the leakage current but also the charge distribtuion in the bulk is changed. This induced charge redistribution affects as the bulk potential change. This is modeled in a simple way as

$$\begin{aligned}\Delta I_{\rm ds} = \frac{2}{3}\sqrt{\frac{2\epsilon_{\rm Si} q N_{\rm sub}}{\beta}} \Big[& \left\{\beta(\phi_{\rm SL} - V_{\rm bs}) - 1\right\}^{\frac{3}{2}} \frac{3}{2} \frac{\beta \Delta V_{\rm bulk}}{\beta(\phi_{\rm SL} - V_{\rm bs}) - 1} \\ & - \left\{\beta(\phi_{\rm S0} - V_{\rm bs}) - 1\right\}^{\frac{3}{2}} \frac{3}{2} \frac{\beta \Delta V_{\rm bulk}}{\beta(\phi_{\rm S0} - V_{\rm bs}) - 1}\Big] \\ - \sqrt{\frac{2\epsilon_{\rm Si} q N_{\rm sub}}{\beta}} \Big[& \left\{\beta(\phi_{\rm SL} - V_{\rm bs}) - 1\right\}^{\frac{1}{2}} \frac{1}{2} \frac{\beta \Delta V_{\rm bulk}}{\beta(\phi_{\rm SL} - V_{\rm bs}) - 1} \\ & - \left\{\beta(\phi_{\rm S0} - V_{\rm bs}) - 1\right\}^{\frac{1}{2}} \frac{1}{2} \frac{\beta \Delta V_{\rm bulk}}{\beta(\phi_{\rm S0} - V_{\rm bs}) - 1}\Big]\end{aligned} \tag{177}$$

where

$$\Delta V_{\rm bulk} = IBPC1 \cdot (1 + \mathbf{IBPC2} \cdot \Delta V_{\rm th}) \cdot I_{\rm sub} \tag{178}$$

where

$$IBPC1 = \mathbf{IBPC1} \cdot \left(1 + \frac{\mathbf{IBPC1L}}{(L_{\rm gate} \cdot 10^6)^{\mathbf{IBPC1LP}}}\right) \tag{179}$$

and **IBPC1**, **IBPC1L**, **IBPC1LP** and **IBPC2** are model parameters.

Impact-Ionization in Drift Region

With increased $V_{\rm gs}$ the impact ionization occurs in the drift region, which shows exponential characteristics as a function of $V_{\rm gs}$. This type of impact-ionization induced current is modeled as

$$I_{\rm subLD} = I_{\rm ds} \cdot SUBLD1 \cdot E_{\rm y} \cdot L_{\rm drift} \cdot \exp\left(\frac{-\mathbf{SUBLD2}}{E_{\rm y} \cdot f(V_{\rm g}V_{\rm t})}\right) \tag{180}$$

$$E_{\rm y} = \frac{V_{\rm ddp} - \Delta V}{L_{\rm drift}} \tag{181}$$

$$f(V_{\rm g}V_{\rm t}) = \sqrt{Q_{\rm I}/q} \tag{182}$$

$$L_{\rm drift} = \mathbf{LDRIFT1} + \mathbf{LDRIFT2} \tag{183}$$

where ΔV is the potential change due to the stored generated carriers in the overlap region, and is modeled as

$$\Delta V = \mathbf{XPDV} \cdot T0 \cdot \mathbf{XLDLD} \cdot \exp\left(-\frac{a}{T0}\right) \tag{184}$$

$$T0 = V_{\rm ddp} - \mathbf{XPVDTH} \cdot (1 + \mathbf{XPVDTHG} \cdot V_{\rm gs}) \tag{185}$$

where a is unity with voltage dimension. This $I_{\rm subLD}$ is added to the conventional $I_{\rm sub}$. The potential change ΔV is the origin of the expansion effect. The parameter $SUBLD1$ provides the $L_{\rm gate}$ dependence

$$SUBLD1 = \mathbf{SUBLD1} \cdot \left(1 + \frac{\mathbf{SUBLD1L}}{(L_{\rm gate} \cdot 10^6)^{\mathbf{SUBLD1LP}}}\right) \tag{186}$$

17.2 Gate Current

All possible gate leakage currents are schematically shown in Fig. 20.

(i) Between Gate and Channel, $I_{\rm gate}$

As for the current between gate and channel, ($I_{\rm gate}$) the direct-tunneling mechanism is considered [38]. Since measured $I_{\rm gate}$ shows nearly linear $L_{\rm gate}$ dependence, the tunneling is assumed to occur along the whole channel length. Thus the final description implemented in HiSIM is [39, 40]

$$I_{\rm gate} = q \cdot \mathbf{GLEAK1} \cdot \frac{E^2}{E_{\rm gp}^{\frac{1}{2}}} \cdot \exp\left(-\frac{E_{\rm gp}^{\frac{3}{2}} \cdot \mathbf{GLEAK2}}{E}\right) \cdot \sqrt{\frac{Q_{\rm i}}{const0}} \cdot W_{\rm eff} \cdot \mathbf{NF} \cdot L_{\rm eff} \cdot \frac{\mathbf{GLEAK6}}{\mathbf{GLEAK6} + V_{\rm ds}} \cdot \frac{\mathbf{GLEAK7}}{\mathbf{GLEAK7} + W_{\rm eff} \cdot \mathbf{NF} \cdot L_{\rm eff}} \tag{187}$$

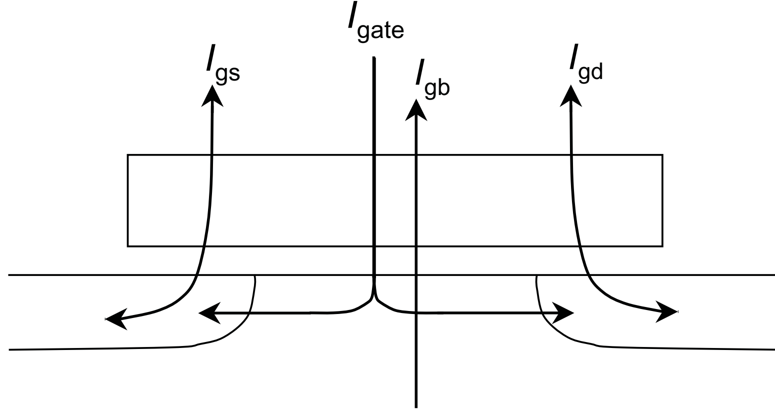

Fig. 20: Gate leakage currents considered.

where

$$E = \frac{\{V_{\mathrm{G}} - \mathbf{GLEAK3} \cdot \phi_{\mathrm{S}}(\Delta L)\}^2}{T_{\mathrm{ox}}} \cdot \left(1 + \frac{E_{\mathrm{y}}}{\mathbf{GLEAK5}}\right) \tag{188}$$

$$V_{\mathrm{G}} = V_{\mathrm{gs}} - \mathbf{VFBC} + \mathbf{GLEAK4} \cdot \Delta V_{\mathrm{th}} \cdot L_{\mathrm{eff}} \tag{189}$$

$$\Delta V_{\mathrm{th}} = \Delta V_{\mathrm{th,SC}} + \Delta V_{\mathrm{th,P}} + \Delta V_{\mathrm{th,W}} - \phi_{\mathrm{Spg}} \tag{190}$$

GLEAK1 – 7 are model parameters, and E_{gp} describes the temperture dependent bandgap for the gate current. The gate-channel current I_{gate} is partitioned into two terminal currents with one model parameter in the following manner.

$$I_{\mathrm{gate}} = I_{\mathrm{gate,s}} + I_{\mathrm{gate,d}} \tag{191}$$

where

$$I_{\mathrm{gate,s}} = (1 - P_{\mathrm{atition}} \cdot I_{\mathrm{gate}}) \tag{192}$$

$$I_{\mathrm{gate,d}} = P_{\mathrm{artition}} \cdot I_{\mathrm{gate}} \tag{193}$$

where analytical description of P_{artition} is obtained by integrating the following equation

$$I_{\mathrm{gate,d}} = \int_0^{L_{\mathrm{eff}}} \frac{y}{L_{\mathrm{eff}}} I_{\mathrm{gate}}(y) dy = P_{\mathrm{artition}} I_{\mathrm{gate}} \tag{194}$$

The straightforward simulation result is shown in Fig. 21.

(ii) Between Gate and Bulk, I_{gb}

The I_{gb} current under the accumulation condition is modeled as

$$I_{\mathrm{gb}} = \mathbf{GLKB1} \cdot E_{\mathrm{gb}}^2 \cdot \exp\left(-\frac{\mathbf{GLKB2}}{E_{\mathrm{gb}}}\right) W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot L_{\mathrm{eff}} \tag{195}$$

$$E_{\mathrm{gb}} = -\frac{V_{\mathrm{gs}} - \mathbf{VFBC} + \mathbf{GLKB3}}{T_{\mathrm{ox}}} \tag{196}$$

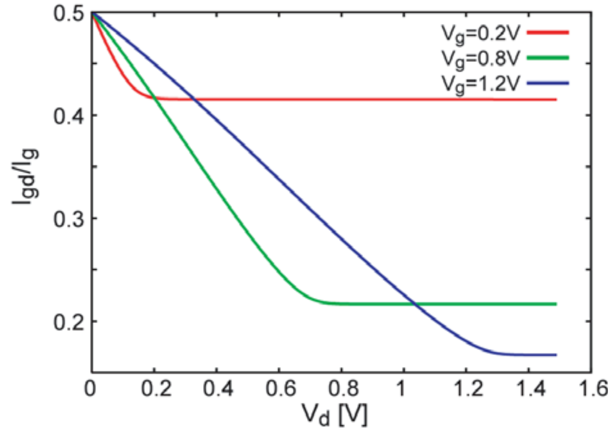

Fig. 21: Exact results of gate partitioning.

The Fowler-Nordheim tunneling mechanism is also considered

$$I_{\mathrm{FN}} = \frac{q \cdot \mathbf{FN1} \cdot E_{\mathrm{FN}}^2}{E_{\mathrm{g12}}} \cdot \exp\left(-\frac{\mathbf{FN2} \cdot E_{\mathrm{g32}}}{E_{\mathrm{FN}}}\right) \cdot W_{\mathrm{eff}} \cdot \mathbf{NF} \cdot L_{\mathrm{eff}} \tag{197}$$

where

$$E_{\mathrm{FN}} = -\frac{\mathbf{FVBS} \cdot V_{\mathrm{bs}} - (V_{\mathrm{gs}} - \Delta V_{\mathrm{th,SC}} - \Delta V_{\mathrm{th,P}}) - \mathbf{FN3}}{T_{\mathrm{OX}}} \tag{198}$$

$$E_{\mathrm{g32}} = E_{\mathrm{g}} \cdot E_{\mathrm{g12}} \tag{199}$$

$$E_{\mathrm{g12}} = \sqrt{E_{\mathrm{g}}} \tag{200}$$

Total substrate current is the sum of the two components as

$$I_{\mathrm{gb}} = I_{\mathrm{gb}} + I_{\mathrm{FN}} \tag{201}$$

(iii) Between Gate and Source/Drain, $I_{\mathrm{gs}}/I_{\mathrm{gd}}$

The tunneling current between the gate and the source/drain overlap region is modeled as

$$I_{\mathrm{gs}} = sign\mathbf{GLKSD1} \cdot E_{\mathrm{gs}}^2 \exp\left(T_{\mathrm{ox}}(-\mathbf{GLKSD2} \cdot V_{\mathrm{gs}} + \mathbf{GLKSD3})\right) W_{\mathrm{eff}} \cdot \mathbf{NF} \tag{202}$$

$$E_{\mathrm{gs}} = \frac{V_{\mathrm{gs}}}{T_{\mathrm{ox}}} \tag{203}$$

$$I_{\mathrm{gd}} = sign\mathbf{GLKSD1} \cdot E_{\mathrm{gd}}^2 \exp\left(T_{\mathrm{ox}}(\mathbf{GLKSD2} \cdot (-V_{\mathrm{gs}} + V_{\mathrm{ds}}) + \mathbf{GLKSD3})\right) W_{\mathrm{eff}} \cdot \mathbf{NF} \tag{204}$$

$$E_{\mathrm{gd}} = \frac{V_{\mathrm{gs}} - V_{\mathrm{ds}}}{T_{\mathrm{ox}}} \tag{205}$$

$$sign = +1 \quad \text{for} \quad E \leq 0$$
$$sign = -1 \quad \text{for} \quad E \geq 0$$

17.3 GIDL (Gate-Induced Drain Leakage)

The GIDL current is generated at the drain junction under the accumulation condition. The $V_{\rm ds}$ increase induces a very narrow potential well in the drain just under the gate, causing carrier generation. Therefore, the GIDL current is strongly dependent on $V_{\rm ds}$. At further reduced $V_{\rm gs}$ values the direct gate tunneling starts to dominate the $I_{\rm GIDL}$ measurements, resulting in $V_{\rm ds}$ independence. The $V_{\rm ds}$ dependent $I_{\rm GIDL}$ is modeled here. The generation mechanism is considered to be the direct tunneling between the above mentioned narrow potential well of length ΔY and the ordinary drain region.

$$I_{\rm GIDL} = \alpha I_{\rm ds} \Delta Y \tag{206}$$

The generation occurs only in this ΔY region at the drain. The final equation is

$$I_{\rm GIDL} = q \cdot \mathbf{GIDL1} \cdot \frac{E^2}{E_{\rm g}^{\frac{1}{2}}} \cdot \exp\left(-\mathbf{GIDL2} \cdot \frac{E_{\rm g}^{\frac{3}{2}}}{E}\right) \cdot W_{\rm eff} \cdot \mathbf{NF} \cdot A \tag{207}$$

where

$$E = \frac{\mathbf{GIDL3} \cdot (V_{\rm ds} + \mathbf{GIDL4}) - V'_{\rm G}}{T_{\rm ox}} \tag{208}$$

$$V'_{\rm G} = V_{\rm gs} + \Delta V_{\rm th} \cdot \mathbf{GIDL5} \tag{209}$$

and A is introduced after BSIM4 as

$$A = \left(\frac{V_{\rm db}^3}{V_{\rm db}^3 + 0.5}\right) \tag{210}$$

$$V_{\rm db} = V_{\rm ds} - V_{\rm bs} \tag{211}$$

Here $\Delta V_{\rm th}$ is defined as

$$\Delta V_{\rm th} = \Delta V_{\rm th,SC} + \Delta V_{\rm th,P} \tag{212}$$

The GISL current is calculated with the same equation as the GIDL current described above. The selection either $I_{\rm GIDL}$ or $I_{\rm GISL}$ is done by the polarity of the current flow.

The HiSIM model parameters introduced in section 17 are summarized in Table 17.

Table 17: HiSIM model parameters introduced in section 17 of this manual. ∗ indicates minor parameters.

SUB1	substrate current coefficient of magnitude
SUB1L	$L_{\rm gate}$ dependence **SUB1**
SUB1LP	$L_{\rm gate}$ dependence **SUB1**
SUB2	substrate current coefficient of exponential term
SUB2L	$L_{\rm gate}$ dependence of **SUB2**
SVDS	substrate current dependence on $V_{\rm ds}$
SLG	substrate current dependence on $L_{\rm gate}$
SLGL	substrate current dependence on $L_{\rm gate}$
SLGLP	substrate current dependence on $L_{\rm gate}$
SVBS	substrate current dependence on $V_{\rm bs}$
SVBSL	$L_{\rm gate}$ dependence of **SVBS**
SVBSLP	$L_{\rm gate}$ dependence of **SVBS**
SVGS	substrate current dependence on $V_{\rm gs}$
SVGSL	$L_{\rm gate}$ dependence of **SVGS**
SVGSLP	$L_{\rm gate}$ dependence of **SVGS**
SVGSW	$W_{\rm gate}$ dependence of **SVGS**
SVGSWP	$W_{\rm gate}$ dependence of **SVGS**
IBPC1	impact-ionization induced bulk potential change
IBPC1L	$L_{\rm gate}$ length dependence of impact-ionization induced bulk potential change
IBPC1LP	$L_{\rm gate}$ length dependence of impact-ionization induced bulk potential change
IBPC2	impact-ionization induced bulk potential change
SUBLD1	substrate current induced in $L_{\rm drift}$
SUBLD2	substrate current induced in $L_{\rm drift}$
XPDV	potential change for expansion effect
XPVDTH	potential change for expansion effect
XPVDTHG	potential change for expansion effect
GLEAK1	gate to channel current coefficient
GLEAK2	gate to channel current coefficient
GLEAK3	gate to channel current coefficient
GLEAK4	gate to channel current coefficient
∗**GLEAK5**	gate to channel current coefficient (short channel correction)
∗**GLEAK6**	gate to channel current coefficient ($V_{\rm ds}$ dependence correction)
∗**GLEAK7**	gate to channel current coefficient (gate length and width dependence correction)
∗**EGIG**	bandgap of gate leakage
∗**IGTEMP2**	temperature dependence of gate leakage
∗**IGTEMP3**	temperature dependence of gate leakage
GLKB1	gate to bulk current coefficient
GLKB2	gate to bulk current coefficient
GLKB3	flat-band shift for gate to bulk current
GLKSD1	gate to source/drain current coefficient
GLKSD2	gate to source/drain current coefficient
GLKSD3	gate to source/drain current coefficient
GLPART1	partitioning ratio of gate leakage current
FN1	coefficient of Fowler-Nordheim-current contribution
FN2	coefficient of Fowler-Nordheim-current contribution
FN3	coefficient of Fowler-Nordheim-current contribution
FVBS	$V_{\rm bs}$ dependence of Fowler-Nordheim current
GIDL1	magnitude of the GIDL
GIDL2	field dependence of the GIDL
GIDL3	$V_{\rm ds}$ dependence of the GIDL
∗**GIDL4**	threshold of $V_{\rm ds}$ dependence
∗**GIDL5**	correction of high-field contribution

18 Source/Bulk and Drain/Bulk Diode Models

18.1 Diode Current

The model equations for the source/bulk and drain/bulk diode currents are based on the concepts of BSIM3v3 [42], but include a number of modifications.

The two regions denoted (a) and (b) in the schematic diagram of Fig. 22, correspond to the forward-bias current saturation and the backward-bias region, respectively. These regions are distinguished in the modeling and are treated separately according to their origins.

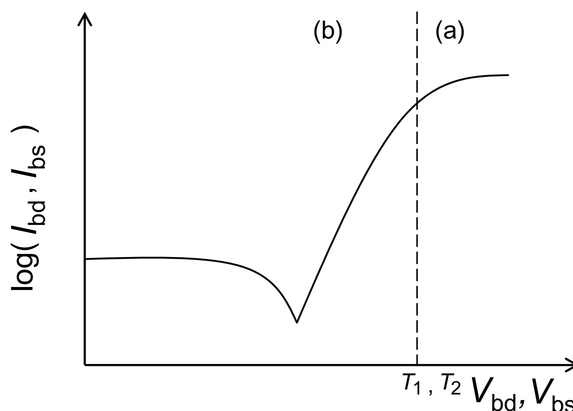

Fig. 22: The two $I_{\rm diode}$ currents ($I_{\rm bd}$ and $I_{\rm bs}$) are modeled separately in the two different operating regions (a) and (b).

The models for forward-biased current densities, describing the area and sidewall components of the source/drain regions, are given in Eqs. (213) and (214), respectively. The corresponding backward-biased current densities are given in Eqs. (215) and (216). These values include temperature dependence as described in section 14.

$$j_{\rm s} = \mathbf{JS0} \tag{213}$$

$$j_{\rm ssw} = \mathbf{JS0SW} \tag{214}$$

$$j_{\rm s2} = \mathbf{JS0} \tag{215}$$

$$j_{\rm ssw2} = \mathbf{JS0SW} \tag{216}$$

(i) Between Drain and Bulk

With these current densities and the area parameter AD and the perimeter parameter PD of the drain region, the forward and backward currents between drain and bulk are calculated as

$$I_{\rm sbd} = AD \cdot j_{\rm s} + PD \cdot j_{\rm ssw} \tag{217}$$

$$I_{\rm sbd2} = AD \cdot j_{\rm s2} + PD \cdot j_{\rm ssw2} \tag{218}$$

The resulting drain-bulk current equations in the 2 operating regions (a) and (b) are derived as follows.

a) $V_{\rm bd} \geq V_1$

$$\begin{aligned} I_{\rm bd} =& I_{\rm sbd}\left\{\exp\left(\frac{V_1}{N_{\rm vtm}}\right)-1\right\} + \frac{I_{\rm sbd}}{N_{\rm vtm}}\exp\left(\frac{V_1}{N_{\rm vtm}}\right)(V_{\rm bd}-V_1) \\ &+ I_{\rm sbd2}\cdot\mathbf{CISB}\left\{\exp\left(-\frac{V_{\rm bd}\mathbf{CVB}}{N_{\rm vtm}}\right)-1\right\} \\ &+ \mathbf{CISBK}\left\{\exp\left(-\frac{V_{\rm bd}\mathbf{CVB}}{N_{\rm vtm}}\right)-1\right\} \end{aligned} \tag{219}$$

b) $V_1 \geq V_{\rm bd}$

$$\begin{aligned} I_{\rm bd} =& I_{\rm sbd}\left\{\exp\left(\frac{V_{\rm bd}}{N_{\rm vtm}}\right)-1\right\} \\ &+ I_{\rm sbd2}\cdot\mathbf{CISB}\cdot\left\{\exp\left(-\frac{V_{\rm bd}\cdot\mathbf{CVB}}{N_{\rm vtm}}\right)-1\right\} \\ &+ \mathbf{CISBK}\cdot\left\{\exp\left(-\frac{V_{\rm bd}\cdot\mathbf{CVB}}{N_{\rm vtm}}\right)-1\right\} \end{aligned} \tag{220}$$

$$N_{\rm vtm} = \frac{\mathbf{NJ}}{\beta} \tag{221}$$

$$V_1 = N_{\rm vtm}\cdot\log\left\{\frac{\mathbf{VDIFFJ}}{I_{\rm sbd}}+1\right\} \tag{222}$$

$$I_{\rm bd} = I_{\rm bd} + \mathbf{DIVX}\cdot I_{\rm sbd2}\cdot V_{\rm bd} \tag{223}$$

(ii) Between Source and Bulk

The area parameter AS and the perimeter parameter PS of the source region are used to calculate the forward and backward currents between source and bulk.

$$I_{\rm sbs} = AS \cdot j_{\rm s} + PS \cdot j_{\rm ssw} \tag{224}$$

$$I_{\rm sbs2} = AS \cdot j_{\rm s2} + PS \cdot j_{\rm ssw2} \tag{225}$$

This leads to the following source-bulk current equations in the 2 operating regions (a) and (b).

a) $V_{\rm bs} \geq V_2$

$$\begin{aligned} I_{\rm bs} =& I_{\rm sbs}\left\{\exp\left(\frac{V_2}{N_{\rm vtm}}\right)-1\right\} + \frac{I_{\rm sbs}}{N_{\rm vtm}}\exp\left(\frac{V_2}{N_{\rm vtm}}\right)(V_{\rm bs}-V_2) \\ &+ I_{\rm sbs2}\cdot\mathbf{CISB}\left\{\exp\left(-\frac{V_{\rm bs}\mathbf{CVB}}{N_{\rm vtm}}\right)-1\right\} \\ &+ \mathbf{CISBK}\left\{\exp\left(-\frac{V_{\rm bs}\mathbf{CVB}}{N_{\rm vtm}}\right)-1\right\} \end{aligned} \tag{226}$$

b) $V_2 \geq V_{\rm bs}$

$$\begin{aligned} I_{\rm bs} =& I_{\rm sbs} \cdot \left\{ \exp\left(\frac{V_{\rm bs}}{N_{\rm vtm}}\right) - 1 \right\} \\ &+ I_{\rm sbs2} \cdot \mathbf{CISB} \cdot \left\{ \exp\left(-\frac{V_{\rm bs} \cdot \mathbf{CVB}}{N_{\rm vtm}}\right) - 1 \right\} \\ &+ \mathbf{CISBK} \cdot \left\{ \exp\left(-\frac{V_{\rm bs} \cdot \mathbf{CVB}}{N_{\rm vtm}}\right) - 1 \right\} \end{aligned} \tag{227}$$

$$V_2 = N_{\rm vtm} \cdot \log\left\{ \frac{\mathbf{VDIFFJ}}{I_{\rm sbs}} + 1 \right\} \tag{228}$$

$$I_{\rm bs} = I_{\rm bs} + \mathbf{DIVX} \cdot Isbs2 \cdot V_{\rm bs} \tag{229}$$

The hard-breakdown model of the diode will be implemented in a future version of HiSIM.

18.2 Diode Capacitance

The diode capacitances of the source/bulk junction $C_{\rm apbs}$ and of the drain/bulk junction $C_{\rm apbd}$ are given by the following equations. These equations have the same basis as those used in BSIM3v3 [42], but include a number of minor modifications.

The notations $\Theta = S,\ \ \theta = s$ (for source/bulk junction) and
$\Theta = D,\ \ \theta = d$ (for drain/bulk junction) apply.

$$c_{{\rm zb}\theta} = \mathbf{CJ} \cdot A\Theta \tag{230}$$

(I) $P\Theta > W_{\rm eff}$

$$c_{{\rm zb}\theta{\rm sw}} = \mathbf{CJSW}(P\Theta - W_{\rm eff} \cdot \mathbf{NF}) \tag{231}$$

$$c_{{\rm zb}\theta{\rm swg}} = \mathbf{CJSWG} \cdot W_{\rm eff} \cdot \mathbf{N} \tag{232}$$

(i) $V_{{\rm b}\theta} = 0$

$$Q_{{\rm b}\theta} = 0 \tag{233}$$

$$C_{{\rm apb}\theta} = c_{{\rm zb}\theta} + c_{{\rm zb}\theta{\rm sw}} + c_{{\rm zb}\theta{\rm swg}} \tag{234}$$

(ii) $V_{{\rm b}\theta} < 0$

a-1) $c_{{\rm zb}\theta} > 0$

$$arg = 1 - \frac{V_{{\rm b}\theta}}{\mathbf{PB}} \tag{235}$$

α) $\mathbf{MJ} = 0.5$

$$sarg = \frac{1}{\sqrt{arg}} \tag{236}$$

β) $\mathbf{MJ} \neq 0.5$

$$sarg = \exp(-\mathbf{MJ} \cdot \log(arg)) \tag{237}$$

$$Q_{{\rm b}\theta} = \frac{\mathbf{PB} \cdot c_{{\rm zb}\theta}(1 - arg \cdot sarg)}{1 - \mathbf{MJ}} \tag{238}$$

$$C_{{\rm apb}\theta} = c_{{\rm zb}\theta} \cdot sarg \tag{239}$$

a-2) $c_{\mathrm{zb}\theta} \leq 0$

$$Q_{\mathrm{b}\theta} = 0 \tag{240}$$

$$C_{\mathrm{apb}\theta} = 0 \tag{241}$$

b) $c_{\mathrm{zb}\theta\mathrm{sw}} > 0$

$$arg = 1 - \frac{V_{\mathrm{b}\theta}}{\mathbf{PBSW}} \tag{242}$$

α) $\mathbf{MJSW} = 0.5$

$$sarg = \frac{1}{\sqrt{arg}} \tag{243}$$

β) $\mathbf{MJSW} \neq 0.5$

$$sarg = \exp(-\mathbf{MJSW} \cdot \log(arg)) \tag{244}$$

$$Q_{\mathrm{b}\theta} += \frac{\mathbf{PBSW} \cdot c_{\mathrm{zb}\theta\mathrm{sw}}(1 - arg \cdot sarg)}{1.0 - \mathbf{MJSW}} \tag{245}$$

$$C_{\mathrm{apb}\theta} += c_{\mathrm{zb}\theta\mathrm{sw}} \cdot sarg \tag{246}$$

c) $c_{\mathrm{zb}\theta\mathrm{swg}} > 0$

$$arg = 1 - \frac{V_{\mathrm{b}\theta}}{\mathbf{PBSWG}} \tag{247}$$

α) $\mathbf{MJSWG} = 0.5$

$$sarg = \frac{1}{\sqrt{arg}} \tag{248}$$

β) $\mathbf{MJSWG} \neq 0.5$

$$sarg = \exp(-\mathbf{MJSWG} \cdot \log(arg)) \tag{249}$$

$$Q_{\mathrm{b}\theta} += \frac{\mathbf{PBSWG} \cdot c_{\mathrm{zb}\theta\mathrm{swg}}(1 - arg \cdot sarg)}{1 - \mathbf{MJSWG}} \tag{250}$$

$$C_{\mathrm{apb}\theta} += c_{\mathrm{zb}\theta\mathrm{swg}} \cdot sarg \tag{251}$$

(iii) $V_{\mathrm{b}\theta} > 0$

$$\begin{aligned} Q_{\mathrm{b}\theta} &= V_{\mathrm{b}\theta}(c_{\mathrm{zb}\theta} + c_{\mathrm{zb}\theta\mathrm{sw}} + c_{\mathrm{zb}\theta\mathrm{swg}}) \\ &+ V_{\mathrm{b}\theta}^2 \left(\frac{1}{2} \frac{c_{\mathrm{zb}\theta} \cdot \mathbf{MJ}}{\mathbf{PB}} + \frac{1}{2} \frac{c_{\mathrm{zb}\theta\mathrm{sw}} \cdot \mathbf{MJSW}}{\mathbf{PBSW}} + \frac{1}{2} \frac{c_{\mathrm{zb}\theta\mathrm{swg}} \cdot \mathbf{MJSWG}}{\mathbf{PBSWG}} \right) \end{aligned} \tag{252}$$

$$\begin{aligned} C_{\mathrm{apb}\theta} &= c_{\mathrm{zb}\theta} + c_{\mathrm{zb}\theta\mathrm{sw}} + c_{\mathrm{zb}\theta\mathrm{swg}} \\ &+ V_{\mathrm{b}\theta} \left(\frac{c_{\mathrm{zb}\theta} \cdot \mathbf{MJ}}{\mathbf{PB}} + \frac{c_{\mathrm{zb}\theta\mathrm{sw}} \cdot \mathbf{MJSW}}{\mathbf{PBSW}} + \frac{c_{\mathrm{zb}\theta\mathrm{swg}} \cdot \mathbf{MJSWG}}{\mathbf{PBSWG}} \right) \end{aligned} \tag{253}$$

(II) $P\Theta \leq W_{\mathrm{eff}}$

$$c_{\mathrm{zb}\theta\mathrm{swg}} = \mathbf{CJSWG} \cdot P\Theta \tag{254}$$

(i) $V_{\mathrm{b}\theta} = 0$

$$Q_{\mathrm{b}\theta} = 0 \tag{255}$$

$$C_{\mathrm{apb}\theta} = c_{\mathrm{zb}\theta} + c_{\mathrm{zb}\theta\mathrm{swg}} \tag{256}$$

(ii) $V_{\mathrm{b}\theta} < 0$

a-1) $c_{\mathrm{zb}\theta} > 0$

$$arg = 1 - \frac{V_{\mathrm{b}\theta}}{\mathbf{PB}} \tag{257}$$

α) $\mathbf{MJ} = 0.5$

$$sarg = \frac{1}{\sqrt{arg}} \tag{258}$$

β) $\mathbf{MJ} \neq 0.5$

$$sarg = \exp(-\mathbf{MJ} \cdot \log(arg)) \tag{259}$$

$$Q_{\mathrm{b}\theta} = \frac{\mathbf{PB} \cdot c_{\mathrm{zb}\theta}(1 - arg \cdot sarg)}{1 - \mathbf{MJ}} \tag{260}$$

$$C_{\mathrm{apb}\theta} = c_{\mathrm{zb}\theta} \cdot sarg \tag{261}$$

a-2) $c_{\mathrm{zb}\theta} \leq 0$

$$Q_{\mathrm{b}\theta} = 0 \tag{262}$$

$$C_{\mathrm{apb}\theta} = 0 \tag{263}$$

b) $c_{\mathrm{zb}\theta\mathrm{swg}} > 0$

$$arg = 1 - \frac{V_{\mathrm{b}\theta}}{\mathbf{PBSWG}} \tag{264}$$

α) $\mathbf{MJSWG} = 0.5$

$$sarg = \frac{1}{\sqrt{arg}} \tag{265}$$

β) $\mathbf{MJSWG} \neq 0.5$

$$sarg = \exp(-\mathbf{MJSWG} \cdot \log(arg)) \tag{266}$$

$$Q_{\mathrm{b}\theta} += \mathbf{PBSWG} \cdot c_{\mathrm{zb}\theta\mathrm{swg}} \cdot \frac{1 - arg \cdot sarg}{1 - \mathbf{MJSWG}} \tag{267}$$

$$C_{\mathrm{apb}\theta} += c_{\mathrm{zb}\theta\mathrm{swg}} \cdot sarg \tag{268}$$

(iii) $V_{\mathrm{b}\theta} > 0$

$$Q_{\mathrm{b}\theta} = V_{\mathrm{b}\theta} \cdot (c_{\mathrm{zb}\theta} + c_{\mathrm{zb}\theta\mathrm{swg}}) + V_{\mathrm{b}\theta}^2 \left(\frac{1}{2} \frac{c_{\mathrm{zb}\theta} \cdot \mathbf{MJ}}{\mathbf{PB}} + \frac{1}{2} \frac{c_{\mathrm{zb}\theta\mathrm{swg}} \cdot \mathbf{MJSWG}}{\mathbf{PBSWG}} \right) \tag{269}$$

$$C_{\mathrm{apb}\theta} = c_{\mathrm{zb}\theta} + c_{\mathrm{zb}\theta\mathrm{swg}} + V_{\mathrm{b}\theta} \left(\frac{c_{\mathrm{zb}\theta} \cdot \mathbf{MJ}}{\mathbf{PB}} + \frac{c_{\mathrm{zb}\theta\mathrm{swg}} \cdot \mathbf{MJSWG}}{\mathbf{PBSWG}} \right) \tag{270}$$

The HiSIM model parameters introduced in section 18 are summarized in Table 18.

Table 18: HiSIM model parameters introduced in section 18 of this manual. # indicates instance parameters.

Parameter	Description
JS0	saturation current density
JS0SW	sidewall saturation current density
NJ	emission coefficient
NJSW	sidewall emission coefficient
DIVX	reverse current coefficient
CISB	reverse biased saturation current
CVB	bias dependence coefficient of **CISB**
CISBK	reverse biased saturation current (at low temperature)
CVBK	bias dependence coefficient of **CISB** (at low temperature)
MJ	bottom junction capacitance grading coefficient
MJSW	source/drain sidewall junction capacitance grading coefficient
MJSWG	source/drain gate sidewall junction capacitance grading coefficient
PB	bottom junction build-in potential
PBSW	source/drain sidewall junction build-in potential
PBSWG	source/drain gate sidewall junction build-in potential
VDIFFJ	diode threshold voltage between source/drain and substrate
#**AD**	junction area of the drain contact
#**PD**	junction periphery of the drain contact
#**AS**	junction area of the source contact
#**PS**	junction periphery of the source contact

19 Noise Models

19.1 $1/f$ Noise Model

The $1/f$ noise is caused by both the carrier fluctuation and the mobility fluctuation. The final description for the drift-diffusion model is [43]

$$S_{I_{\rm ds}} = \frac{I_{\rm ds}^2 \mathbf{NFTRP}}{\beta f (L_{\rm eff} - \Delta L) W_{\rm eff} \cdot \mathbf{NF}} \left[\frac{1}{(N_0 + N^*)(N_L + N^*)} + \frac{2\mu E_y \mathbf{NFALP}}{N_L - N_0} \ln \left(\frac{N_L + N^*}{N_0 + N^*} \right) + (\mu E_y \mathbf{NFALP})^2 \right] \tag{271}$$

where the parameters **NFALP** and **NFTRP** represent the contribution of the mobility fluctuation and the ratio of trap density to attenuation coefficient, respectively. N_0 and N_L are carrier densities at source side and drain side or pinch-off point, respectively, as calculated in HiSIM. N^* is written as

$$N^* = \frac{C_{\rm ox} + C_{\rm dep} + \mathbf{CIT}}{q\beta} \tag{272}$$

where $C_{\rm dep}$ is the depletion capacitance calculated with $\phi_{\rm S}$. **CIT** is the capacitance caused by the interface-trapped carriers and is normally fixed to be zero.

$$N_{\rm flick} = S_{I_{\rm ds}} \cdot f^{\mathbf{FALPH}} \tag{273}$$

is calculated in HiSIM, where **FALPH** has been introduced to model the deviation from the exact $1/f$ characteristic.

19.2 Thermal Noise Model

Van der Ziel derived the equation for the spectral density of the thermal drain-noise current at temperature T by integrating the transconductance along the channel direction y based on the Nyquist theorem [44]

$$S_{\rm id} = \frac{4kT}{L_{\rm eff}^2} \int g_{\rm ds}(y) dy = 4kT g_{\rm ds0} \gamma \tag{274}$$

Here k, $I_{\rm ds}$, $g_{\rm ds}(y)$, $g_{\rm ds0}$, γ are Boltzmann's constant, drain current, position-dependent channel conductance, channel conductance at $V_{\rm ds} = 0$, and drain-noise coefficient, respectively. In HiSIM the integration is performed with the surface potential $\phi_{\rm s}$ instead of the channel position as [45, 46]

$$S_{\rm id} = \frac{4kT}{L_{\rm eff}^2 I_{\rm ds}} \int g_{\rm ds}^2(\phi_{\rm s}) d\phi_{\rm s} \tag{275}$$

$$g_{\rm ds}(\phi_{\rm s}) = \frac{W_{\rm eff} \cdot \mathbf{NF}}{L_{\rm eff}} \beta \frac{d(\mu(\phi_{\rm s}) f(\phi_{\rm s}))}{d\phi_{\rm s}} \tag{276}$$

Here $f(\phi_{\rm s})$ is a characteristic function of HiSIM related to the carrier concentration [47]. The final equations for $S_{\rm id}$ in our compact-modeling approach, obtained after solving the integral of Eq. (275), become functions of the self-consistent surface potentials as well as the surface-potential derivatives at source and drain.

$$S_{\rm id} = 4kT \frac{W_{\rm eff} \cdot \mathbf{NF} C_{\rm ox} \, VgVt \, \mu}{(L_{\rm eff} - \Delta L)} \frac{(1 + 3\eta + 6\eta^2)\mu_{\rm d}^2 + (3 + 4\eta + 3\eta^2)\mu_{\rm d}\mu_{\rm s} + (6 + 3\eta + \eta^2)\mu_{\rm s}}{15(1+\eta)\mu_{\rm av}^2} \tag{277}$$

where μ_{s}, μ_{d} and μ_{av} are mobilities at the source side, the drain side, and averaged, respectively.

$$\eta = 1 - \frac{(\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}) + \chi(\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}})}{V_{\mathrm{g}}V_{\mathrm{t}}} \tag{278}$$

$$\chi = 2\frac{cnst0}{C_{\mathrm{ox}}}\left[\left[\frac{2}{3}\frac{1}{\beta}\frac{\{\beta(\phi_{\mathrm{SL}} - V_{\mathrm{bs}}) - 1\}^{\frac{3}{2}} - \{\beta(\phi_{\mathrm{S0}} - V_{\mathrm{bs}}) - 1\}^{\frac{3}{2}}}{\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}}\right] - \sqrt{\beta(\phi_{\mathrm{S0}} - V_{\mathrm{bs}}) - 1}\right] \tag{279}$$

$VgVt$ is equal to the carrier density at the source side divided by the oxide capacitance.
Thus no additional model parameters are required for the thermal noise model.

$$N_{\mathrm{thrml}} = S_{\mathrm{id}}/4kT \tag{280}$$

is calculated in HiSIM.

19.3 Induced Gate Noise Model

No additional model parameters are required for the induced gate noise model.

$$N_{\mathrm{igate}} = S_{\mathrm{igate}}/f^2 \tag{281}$$

is calculated in HiSIM. Explicit model equation were presented at SISPAD in 2006 [48].

19.4 Coupling Noise Model

No additional model parameters are required for the coupling noise model.

$$N_{\mathrm{cross}} = \frac{S_{\mathrm{igid}}}{\sqrt{S_{\mathrm{igate}} \cdot S_{\mathrm{id}}}} \tag{282}$$

is calculated in HiSIM. Explicit model equation were presented at SISPAD in 2006 [48].

The HiSIM model parameters introduced in section 19 are summarized in Table 19.

Table 19: HiSIM model parameters introduced in section 19 of this manual. $*$ indicates a minor parameter.

NFTRP	ratio of trap density to attenuation coefficient
NFALP	contribution of the mobility fluctuation
$*$**CIT**	capacitance caused by the interface trapped carriers
FALPH	power of f describing deviation of $1/f$

20 Non-Quasi-Static (NQS) Model

20.1 Carrier Formation

To consider the carrier transit delay in HiSIM, the carrier formation is modeled as [49, 50, 51]

$$q(t_{\rm i}) = \frac{q(t_{\rm i-1}) + \frac{\Delta t}{\tau} Q(t_{\rm i})}{1 + \frac{\Delta t}{\tau}} \tag{283}$$

where $q(t_{\rm i})$ and $Q(t_{\rm i})$ represent the non-quasi-static and the quasi-static carrier density at time $t_{\rm i}$, respectively, and $\Delta t = t_{\rm i} - t_{\rm i-1}$ is valid. The delay is determined by the carrier transit delay τ and the time interval in the circuit simulation Δt.

20.2 Delay Mechanisms

Up to weak inversion:

$$\tau_{\rm diff} = \mathbf{DLY1} \tag{284}$$

At strong inversion:

$$\tau_{\rm cond} = \mathbf{DLY2} \cdot \frac{Q_{\rm i}}{I_{\rm ds}} \tag{285}$$

$$\frac{1}{\tau} = \frac{1}{\tau_{\rm diff}} + \frac{1}{\tau_{\rm cond}} \tag{286}$$

For the formation of bulk carriers:

$$\tau_{\rm B} = \mathbf{DLY3} \cdot C_{\rm ox} \tag{287}$$

where **DLY3** is a constant coefficient and $C_{\rm ox}$ is the oxide capacitance. From the HiSIM_HV 1.1.0 version this NQS model is implemented in the newwork form as shown in Fig. 23.

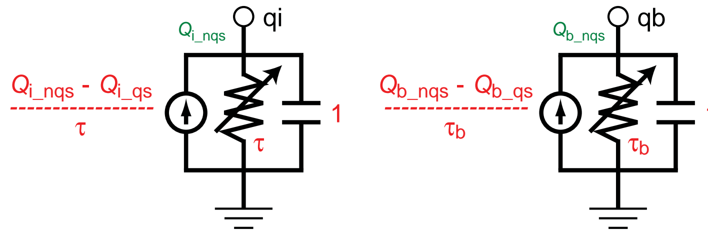

Fig. 23: NQS model implementation into circuit simulator.

20.3 Time-Domain Analysis

The total drain/source/bulk terminal currents are derived from the superposition of the transport current and the charging current. The transport current is a function of the instantaneous terminal voltages and is approximated by the steady-state solution. The source/drain/bulk charging currents are the time derivatives of the associated non-quasi-static charges, $q_{\rm S}$, $q_{\rm D}$, and $q_{\rm B}$, respectively.

For LDMOS/HVMOS, carrier transit delay effect in the drift region is included as the *RC* delay. The resistance *R* and the capacitance *C* contributing the delay are taken calculated in HiSIM_HV. If the resistance in the drift region is large, the delay becomes automatically large.

20.4 AC Analysis

The load file is rewritten from the HiSIM_HV 1.1.0 version so that the internal node is seen explicitly. Thus, the calculation procesure becomes different from the older versions, however, the formulae used for the calculation are the same.

The HiSIM model parameters introduced in section 20 are summarized in Table 20.

Table 20: HiSIM model parameters introduced in section 20 of this manual.

DLY1	coefficient for delay due to diffusion of carriers
DLY2	coefficient for delay due to conduction of carriers
DLY3	coefficient for RC delay of bulk carriers
DLYDFT	coefficient for carrier transit delay: inactivated
DLYOV	coefficient for RC delay of carriers: inactivated

21 Self-Heating Effect Model

The self-heating effect is modeled with the thermal network shown in Fig. 24. The flag **COSELFHEAT** must be equal to one and **RTH0** must not be equal to zero to activate the model. The temperature node must not be zero, if the self-heating effect is switched on. The SHE should be switched on/off only with the model flag **COSELFHEAT**. The temperature node is automatically generated in circuit simulator for each device as other bias nodes. Fisrt, the model core (HiSIMhv.eval) is called to evaluate device characteristics without heating. Then, the temperature is updated considering the self-heating effect by creating the temperature node. The model core is called again to update the device characteristics with the calculated temperature T. Under the DC condition the temperature increase is calculated analytically as

$$T = T + R_{\rm th} \cdot I_{\rm ds} \cdot V_{\rm ds} \tag{288}$$

where $R_{\rm th}$ as well as $C_{\rm th}$ are a function of $W_{\rm eff}$ as

$$R_{\rm th} = \frac{R_{\rm th0}}{W_{\rm eff}} \cdot \left(\frac{1}{\mathbf{NF}^{\mathbf{RTH0NF}}}\right)\left(1 + \frac{\mathbf{RTH0W}}{(W_{\rm gate} \cdot 10^6)^{\mathbf{RTH0WP}}}\right) \tag{289}$$

$$R_{\rm th0} = \mathbf{RTH0} + \mathbf{RTHTEMP1} \cdot (T0 - \mathbf{TNOM}) + \mathbf{RTHTEMP2} \cdot (T0^2 - \mathbf{TNOM}^2) \tag{290}$$

$$C_{\rm th} = \mathbf{CTH0} \cdot W_{\rm eff} \tag{291}$$

The model parameter **RTH0** is fitted to measured DC data, and the model parameter **CTH0** is introduced for AC fitting.

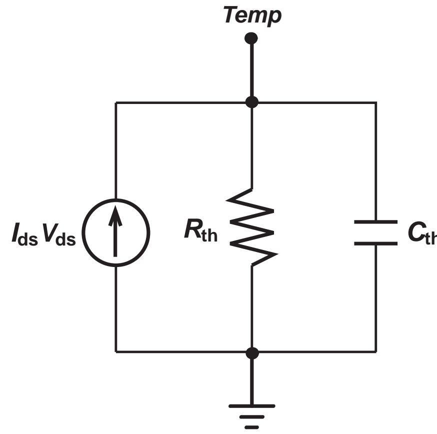

Fig. 24: Thermal Network applied for the self-heating effect.

The thermal dissipation is modeled as [54]

$$T = T + R_{\rm th} \cdot I_{\rm ds} \cdot V'_{\rm ds} \tag{292}$$

$$V'_{\rm ds} = V_{\rm dsi} + POW_{\rm ratio}(V_{\rm ds} - V_{\rm dsi}) \tag{293}$$

$$POW_{\rm ratio} = \mathbf{POWRAT} + \mathbf{PRATTEMP1} \cdot (T0 - \mathbf{TNOM}) + \mathbf{PRATTEMP2} \cdot (T0^2 - \mathbf{TNOM}^2) \tag{294}$$

where **POWRAT** is a model parameter. The external node potential is represented by $V_{\rm ds}$ and the internal node potential within the drift region at the channel/drift junction is by $V_{\rm dsi}$, which is calculated during the SPICE simulation.
A limiter for the temperature increase due to the self-heating effect **SHEMAX** is introduced to avoid drastic artifical temperature increase during circuit simulations.

The HiSIM model parameters introduced in section 21 are summarized in Table 21.

Table 21: HiSIM model parameters introduced in section 21 of this manual.

RTH0	thermal resistance
RTHTEMP1	temperature dependence of thermal resistance
RTHTEMP2	temperature dependence of thermal resistance
CTH0	thermal capacitance
RTH0W	width dependence of thermal resistance
RTH0WP	width dependence of thermal resistance
RTH0NF	number of finger dependence of thermal resistance
RTH0R	thermal dissipation: inactivated
POWRAT	thermal dissipation
PRATTEMP1	tenperture dependence of thermal dissipation
PRATTEMP2	tenperture dependence of thermal dissipation
SHEMAX	maximum temperature increase

22 DFM Model

To support design for manufacturability (DFM) HiSIM introduces an option for considering the variation of device parameters.
Accurate prediction of device performance for a wide range of the substrate-impurity-concentration variations is secured by introducing an impurity concentration dependent mobility due to the phonon scattering as

$$M_{\rm uephonon} = \mathbf{MUEPH1}\,[\mathbf{MPHDFM}\{\ln(\mathbf{NSUBCDFM}) - \ln(N_{\rm subc})\} + 1]$$

$$\mathbf{NSUBP} = \mathbf{NSUBP} + (N_{\rm SUBCDFM} - N_{\rm subc}) \tag{295}$$

$$\mathbf{NEXT} = \mathbf{NEXT} + (\mathbf{NSUBCDFM} - N_{\rm subc}) \tag{296}$$

where **NSUBCDFM** is an instance parameter and **MPHDFM** is a model parameter describing the mobility reduction due to the increase of the substrate impurity concentration. This model is activated if the model flag **CODFM** = 1, and NSUBCDFM is also given.

The HiSIM model parameters introduced in section 22 are summarized in Table 22.

Table 22: HiSIM model parameters introduced in section 22 of this manual. # indicates an instance parameter.

#**NSUBCDFM**	substrate impurity concentration
MPHDFM	mobility dependence of $N_{\rm subc}$ due to $\mu_{\rm phonon}$

23 Exclusion of Modeled Effects and Model Flags

1. To exclude specific modeled effects, following parameter settings should be chosen:

Effect	Setting
Short-Channel Effect	**SC1** = **SC2** = **SC3** = 0
Reverse-Short-Channel Effect	**LP** = 0
Quantum-Mechanical Effect	**QME1** = **QME3** = 0
Poly-Depletion Effect	**PGD1** = **PGD2** = 0
Channel-Length Modulation	**CLM1** = **CLM2** = **CLM3** = 0
Narrow-Channel Effect	**WFC** = **MUEPHW** = **WL1** = 0
Small-Size Effect	**WL2** = 0

Following flags are prepared to select required model options.

2. Selection for asymmetrical (LDMOS) or HV-MOS structure is done:

    COSYM = 0: LDMOS (default)

    COSYM = 1: symmetrical/asymmetrical HV-MOS

3. Contact resistances R_{s} and R_{d} are included:

    CORSRD = 0: no

    CORSRD = 1 & **RS/RD** $\neq 0$: yes, as internal resistance nodes

    CORSRD = 2 & **RD** $\neq 0$: yes, analytical description

    CORSRD = 3 & **RD** $\neq 0$: yes, both internal nodes and analytical description (default)

    CORSRD = -1 & **RS/RD** $\neq 0$: yes, as external resistance nodes

4. Overlap charges/capacitances are added to intrinsic ones:

    COADOV = 0: no

    COADOV = 1: yes (default)

5. Bias dependent overlap capacitance model is selected at drain side:

    COOVLP = 0: constant overlap capacitance

    COOVLP = 1: yes (default) including constant values as option

6. Bias dependent overlap capacitance model is selected at source side:

    COOVLPS = 0: constant overlap capacitance (default)

    COOVLPS = 1: yes including constant values as option

7. Method for calculating potential in overlap region is selected:

    COQOVSM = 0: analytical equation excluding inversion charge

    COQOVSM = 1: iterative solution (default)

    COQOVSM = 2: analytical equation including inversion charge

8. Self-Heating Effect is considered:

    COSELFHEAT = 0: no (default)

    COSELFHEAT = 1: yes

9. Substrate current I_{sub} is calculated:

COISUB = 0: no (default)

COISUB = 1: yes

10. Gate current $I_{\rm gate}$ is calculated:

COIIGS = 0: no (default)

COIIGS = 1: yes

11. GIDL current $I_{\rm GIDL}$ is calculated:

COGIDL = 0: no (default)

COGIDL = 1: yes

12. STI leakage current $I_{\rm ds,STI}$ is calculated:

COISTI = 0: no (default)

COISTI = 1: yes

13. Non-quasi-static mode is invoked:

CONQS = 0: no (default)

CONQS = 1: yes

14. Gate-contact resistance is included:

CORG = 0: no (default)

CORG = 1: yes

15. Substrate resistance network is invoked:

CORBNET = 0: no (default)

CORBNET = 1: yes

16. $1/f$ noise is calculated:

COFLICK = 0: no (default)

COFLICK = 1: yes

17. Thermal noise is calculated:

COTHRML = 0: no (default)

COTHRML = 1: yes

18. Induced gate and cross correlation noise are calculated:

COIGN = 0 ‖ **COTHRML** = 0: no (default)

COIGN = 1 & **COTHRML** = 1: yes

19. Previous $\phi_{\rm S}$ is used for the iteration:

COPPRV = 0: no

COPPRV = 1: yes (default)

20. Parameter variations for the DFM support is considered:

CODFM = 0: no (default)

CODFM = 1: yes

21. Previous Ids is used for calculating source/drain resistance effect ($R_{\rm s}$ and/or $R_{\rm d} \neq 0$): This flag is inactivated.

COIPRV = 0:

COIPRV = 1:

22. Selection for temperature dependence of models:

	$R_{\mathrm{d0,temp}}$	$R_{\mathrm{dvd,temp}}$	V_{max}	N_{invd}	
COTEMP = 0:	T	$T0$	$T0$	$T0$	:default & backward compatible
COTEMP = 1:	$T0$	$T0$	$T0$	$T0$	
COTEMP = 2:	T	T	T	T	
COTEMP = 3:	T	T	$T0$	$T0$	

where T includes the temperature increase by the self-heating effect and $T0$ is without.

23. Selection for the 5th node:

    COSUBNODE = 0: the 5th node is the thermal node.

    COSUBNODE = 1: the 5th node is the V_{sub} node.

24. Selection for R_{drift} model:

    CORDRIFT = 0: old model provided for earlier versions of HiSIM_HV 1.

    CORDRIFT = 1: new model (default).

25. Selection for output message whether model parameter is within recommendend range:

    COERRREP = 0: no message is given.

    COERRREP = 1: range check result is given (default).

24 List of Instance Parameters

Partly the same instance-parameter names and their definitions as in the BSIM3/4 models are adopted for the convenience of HiSIM users. The HiSIM Research Group wishes to acknowledge the UC Berkeley BSIM Research Group for the introduction of these instance parameters.

L	gate length (L_{gate}) default: $\mathbf{L} = 2\mu m$
W	gate width (W_{gate}) default: $\mathbf{W} = 2\mu m$
	** Diode **
AD	area of drain junction
AS	area of source junction
PD	perimeter of drain junction
PS	perimeter of source junction
	** Source/Drain Resistance **
NRS	number of source squares
NRD	number of drain squares
	** Gate Resistance **
XGW	distance from the gate contact to the channel edge
XGL	offset of the gate length
NF	number of gate fingers
M	multiplication factor
NGCON	number of gate contacts
	** Substrate Network **
RBPB	substrate resistance network
RBPD	substrate resistance network
RBPS	substrate resistance network
RBDB	no more used
RBSB	no more used
	** Length of Diffusion **
SA	length of diffusion between gate and STI
SB	length of diffusion between gate and STI
SD	length of diffusion between gate and gate
	** Temperature **
DTEMP	device temperature change
	** Design for Manufacturability **
NSUBCDFM	substrate impurity concentration
	** Substrate Current **
SUBLD1	substrate current induced in L_{drift} (inactivated)
SUBLD2	substrate current induced in L_{drift} (inactivated)
	** Resistance **
LDRIFT1	lenght of lightly doped drift region (default: 0)
LDRIFT2	length of heavily doped drift region (defailt: 1 μm)
LDRIFT1S	lenght of lightly doped drift region in source side (default: 0)
LDRIFT2S	length of heavily doped drift region in source side (defailt: 1 μm)
	** Overlap **
LOVER	lenght of overlap region in source side for LDMOS
LOVERLD	length of overlap region in drain side
LOVERS	lenght of overlap region in source side for HVMOS
COSELFHEAT	falg to switch on the self-heating effect
COSUBNODE	flag for selection of the 5th node

NPEXT	maximum concentration of pocket tail
FALPH	power of f describing deviation of $1/f$
RS	source-contact resistance of LDD region
RD	drain-contact resistance of LDD region
RD22	$V_{\rm bs}$ dependence of **RD** for **CORSRD**=2,3
RD23	modification of **RD** for **CORSRD**=2,3
RD24	$V_{\rm gs}$ dependence of **RD** for **CORSRD**=2,3
RDVG11	$V_{\rm gs}$ dependence of **RD** for **CORSRD**=1,3
RDICT1	**LDRFIT1** dependence of resistance for **CORSRD**=1,3
RDOV13	alternative $L_{\rm over}$ depepdence model for **CORSRD**
RDSLP1	**LDRFIT1** dependence of resistance for **CORSRD**=1,3
RDVB	$V_{\rm bs}$ dependence of **RD** for **CORSRD**=1,3
RDVD	$V_{\rm ds}$ dependence of **RD** for **CORSRD**=1,3
RTH0	thermal resistance
VOVER	velocity overshoot effect
CGBO	gate-to-bulk overlap capacitance
CVDSOVER	modification of the $C_{\rm gg}$ spikes for $V_{\rm ds} \neq 0$
POWRAT	thermal dissipation

25 Default Parameters and Limits of the Parameter Values

The maximum and minimum limits of the model parameter are recommended values. These values may be violated in some specific cases. "default" in remarks means that the default value is preferable.

parameter	unit	min	max	default	remarks
TOX	[m]			7n	
XL	[m]			0	
XW	[m]			0	
XLD	[m]	0	50n	0	
XWD	[m]	-100n	300n	0	
XWDLD	[m]			0	given if $\neq$ **XWD**
XWDC	[m]	-10n	100n	0	given if $\neq$ **XWD**
TPOLY	[m]			200×10^{-9}	
DDRIFT	[m]			0	
LL	[$m^{\mathbf{LLN+1}}$]			0	
LLD	[m]			0	
LLN	[—]			0	
WL	[$m^{\mathbf{WLN+1}}$]			0	
WLD	[m]			0	
WLN	[—]			0	
NSUBC	[cm^{-3}]	1×10^{16}	1×10^{19}	3×10^{17}	
NSUBP	[cm^{-3}]	1×10^{16}	1×10^{19}	1×10^{18}	
DDRIFT	[m]			1.0×10^{-6}	
NSUBSUB	[cm^{-3}]			1.0×10^{15}	required for $V_{\rm sub,s}$ dependence
LP	[m]	0	300n	15n	**LP** $\geq$1nm, **LP**=0 for nopockt
∗**NPEXT**	[cm^{-3}]	1×10^{16}	1×10^{18}	5×10^{17}	
∗**LPEXT**	[m]	1×10^{-50}	1×10^{-5}	1×10^{-50}	
VFBC	[V]	-1.2	-0.4	-1.0	reset within the range
VBI	[V]	1.0	1.2	1.1	
KAPPA	[—]			3.9	
EG0	[eV]	1.0	1.3	1.1785	
BGTMP1	[$eV\,K^{-1}$]	50μ	1000μ	90.25μ	default
BGTMP2	[$eV\,K^{-2}$]	-1μ	1μ	0.1μ	
TNOM	[°C]	22	32	27	
VMAX	[$cm\,s^{-1}$]	1MEG	20MEG	10MEG	
VMAXT1	[$cm\,(sK)^{-1}$]			0	
VMAXT2	[$cm\,(sK^2)^{-1}$]			0	
VOVER	[$m^{\mathbf{VOVERP}}$]	0	4.0	0.3	
VOVERP	[—]	0	2.0	0.3	
∗**VTMP**	[—]	-2.0	1.0	0	
QME1	[Vm]	0	1n	0	
QME2	[V]	1.0	3.0	2.0	
QME3	[m]	0	500p	0	
PGD1	[V]	0	30m	0	
PGD2	[V]	0	1.5	1.0	
∗**PGD4**	[—]	0	3.0	0	

parameter	unit	min	max	default	remarks
PARL2	[m]	0	50n	10n	
SC1	[—]	0	10	0	
SC2	[V^{-1}]	0	1	0	
∗**SC3**	[V^{-1}m]	0	200n	0	
∗∗**SC4**	[1/V]	0		0	
SCP1	[—]	0	10	0	
SCP2	[V^{-1}]	0	1	0	
∗**SCP3**	[V^{-1}m]	0	200n	0	
∗**SCP21**	[V]	0	5.0	0	
∗**SCP22**	[V^4]	0	0	0	reset to zero
∗**BS1**	[V^2]	0	50m	0	
∗**BS2**	[V]	0.5	1.0	0.9	
∗**PTL**	[$V^{\mathbf{PTP}-1}m^{\mathbf{PTLP}}$]	0		0	
∗**PTLP**	[—]			1.0	
∗**PTP**	[—]	3.0	4.0	3.5	
∗**PT2**	[V^{-1}]	0		0	
∗**PT4**	[V^{-2}]	0		0	
∗**PT4P**	[—]	0		1	
∗**GDL**	[$m^{\mathbf{GDLP}}$]	0	220m	0	
∗**GDLP**	[—]			0	
∗**GDLD**	[m]			0	
MUECB0	[$cm^2V^{-1}s^{-1}$]	100	100K	1K	
MUECB1	[$cm^2V^{-1}s^{-1}$]	5	10k	100	
MUEPH0	[—]	0.25	0.35	0.3	default
MUEPH1	[$cm^2V^{-1}s^{-1}$	2K	30K	20K(nMOS),9K(pMOS)	
@	$(V\,cm^{-1})^{\mathbf{MUEPH0}}$]				
MUETMP	[—]	0.5	2.5	1.5	
∗**MUEPHL**	[$\mu m^{\mathbf{MUEDLP}}$]			0	
∗**MUEPLP**	[—]			1.0	
MUESR0	[—]	1.8	2.2	2.0	default
MUESR1	[$cm^2V^{-1}s^{-1}$	1×10^{14}	1×10^{16}	6×10^{14}	
@	$(V\,cm^{-1})^{\mathbf{MUESR0}}$]				
∗**MUESRL**	[$\mu m^{\mathbf{MUESLP}}$]			0	
∗**MUESLP**	[—]			1.0	
NDEP	[—]	0	1.0	1.0	
∗**NDEPL**	[$\mu m^{\mathbf{NDEPLP}}$]			0	
∗**NDEPLP**	[—]			1.0	
NINV	[—]	0	1.0	0.5	
NINVD	[1/V]	0		0.0	
NINVDW	[$\mu m^{\mathbf{NINVDWP}}$]	0		0.0	
NINVDWP	[—]	0		1.0	
NINVDT1	[1/K]	0		0.0	
NINVDT2	[$1/K^2$]	0		0.0	
BB	[—]			2.0(nMOS),1.0(pMOS)	default

parameter	unit	min	max	default	remarks
WFC	[F m^{-1}]	-5.0×10^{-15}	1×10^{-6}	0	
∗**WVTH0**	[V·μm]			0	
∗**NSUBCW**	[μm$^{\mathbf{NSUBCWP}}$]			0	
∗**NSUBCWP**	[—]			1	
∗**NSUBP0**	[cm^{-3}]			0	
∗**NSUBWP**				1.0	
∗**MUEPHW**	[μm$^{\mathbf{MUEPHW}}$]			0	
∗**MUEPWP**	[—]			1.0	
∗**MUESRW**	[μm$^{\mathbf{MUESRW}}$]			0	
∗**MUESWP**	[—]			1.0	
∗**VTHSTI**	[V]			0	
VDSTI	[—]			0	
SCSTI1	[—]			0	
SCSTI2	[V^{-1}]			0	
NSTI	[cm^{-3}]	1×10^{16}	1×10^{19}	5×10^{17}	
WSTI	[m]			0	
WSTIL	[μm$^{\mathbf{WSTILP}}$]			0	
WSTILP	[—]			1.0	
WSTIW	[μm$^{\mathbf{WSTIWP}}$]			0	
WSTIWP	[—]			1.0	
WL1	[μm$^{\mathbf{2WL1P+1}}$]			0	
WL1P	[—]			1.0	
NSUBPSTI1	[m]			0	
NSUBPSTI2	[—]			0	
NSUBPSTI3	[—]			1.0	
MUESTI1	[m]			0	
MUESTI2	[—]			0	
MUESTI3	[—]			1.0	
WL2	[Vμm$^{\mathbf{2WL2P}}$]			0	
WL2P	[—]			1.0	
∗**MUEPHS**	[μm$^{\mathbf{2MUEPSP}}$]			0	
∗**MUEPSP**	[—]			1.0	
∗**VOVERS**	[—]			0	
∗**VOVERSP**	[—]			0	
CLM1	[—]	10m	1.0	50m	
CLM2	[—]	1.0	4.0	2.0	
CLM3	[—]	0.5	5.0	1.0	
CLM5	[—]	0	2.0	1.0	
CLM6	[μm$^{-\mathbf{CLM5}}$]	0	20.0	0	

parameter	unit	min	max	default	remarks
SUB1	[V^{-1}]			10	
SUB1L	[$m^{\mathbf{2WL1P+1}}$]			2.5×10^{-3}	
SUB1LP	[—]			1.0	
SUB2	[V]			25.0	
SUB2L	[m]	0	1.0	2×10^{-6}	
SVDS	[—]			0.8	
SLG	[m]			3×10^{-8}	
SLGL	[$m^{\mathbf{SLGLP}}$]			0	
SLGLP	[—]			1.0	
SVBS	[—]			0.5	
SVBSL	[$m^{\mathbf{SVBSLP}}$]			0	
SVBSLP	[—]			1.0	
SVGS	[—]			0.8	
SVGSL	[$m^{\mathbf{SVGSLP}}$]			0	
SVGSLP	[—]			1.0	
SVGSW	[$m^{\mathbf{SVGSWP}}$]			0	
SVGSWP	[—]			1.0	
IBPC1	[VA^{-1}]	0	1.0×10^{12}	0	
IBPC1L	[]				
IBPC1LP	[]				
IBPC2	[V^{-1}]	0	1.0×10^{12}	0	
SUBLD1	[V^{-1}]			0	
SUBLD1L	[]				
SUBLD1LP	[]				
SUBLD2	[mV^{-1}]			0	
XPDV	[]	0		0	
XPVDTH	[]	0		0	
XPVDTHG	[]	-1	1	0	
MPHDFM	[—]	-3	3	-0.3	
SAREF	[m]			1.0×10^{-6}	
SBREF	[m]			1.0×10^{-6}	

parameter	unit	min	max	default	remarks
GLEAK1	$[\mathrm{V}^{-3/2}\mathrm{s}^{-1}]$			50	
GLEAK2	$[\mathrm{V}^{-1/2}\mathrm{cm}^{-1}]$			10MEG	
GLEAK3	[—]			60×10^{-3}	
GLEAK4	$[\mathrm{m}^{-1}]$			4.0	
∗**GLEAK5**	$[\mathrm{V\,m}^{-1}]$			7.5×10^{3}	
∗**GLEAK6**	[V]			250×10^{-3}	
∗**GLEAK7**	$[\mathrm{m}^{2}]$			1×10^{-6}	
∗**EGIG**	[V]			0.0	
∗**IGTEMP2**	[V K]			0	
∗**IGTEMP3**	$[\mathrm{V\,K}^{2}]$			0	
GLKSD1	$[\mathrm{A\,m\,V}^{-2}]$			1f	
GLKSD2	$[\mathrm{V}^{-1}\mathrm{m}^{-1}]$			1×10^{3}	
GLKSD3	$[\mathrm{m}^{-1}]$			-1×10^{3}	
GLKB1	$[\mathrm{A\,V}^{-2}\,\mathrm{m}^{-2}]$			5×10^{-16}	
GLKB2	$[\mathrm{m\,V}^{-1}]$			1.0	
GLKB3	[V]			0	
GLPART1	[-]	0	1.0	0.5	
FN1	$[V^{-1.5}\cdot\ \mathrm{m}^{2}]$			50	
FN2	$[V^{-0.5}\cdot\ \mathrm{m}^{-1}]$			170×10^{-6}	
FN3	[V]			0	
FVBS	[—]			12×10^{-3}	
GIDL1	$[\mathrm{V}^{-3/2}\mathrm{s}^{-1}\mathrm{m}]$			2.0	
GIDL2	$[\mathrm{V}^{-0.5}\mathrm{m}^{-1}]$			3×10^{7}	
GIDL3	[—]			0.9	
∗**GIDL4**	[V]			0	
∗**GIDL5**	[—]			0.2	
VBSMIN	[V]				no more required
VGSMIN	[V]			-100(nMOS),100(pMOS)	fixed
VZADD0	[V]			10m	fixed
PZADD0	[V]			5m	fixed
DDLTMAX	[—]	1	10	10	
DDLTSLP	$[\mu\mathrm{m}^{-1}]$	0	20	0	
DDLTICT	[—]	-3	20	10	

parameter	unit	min	max	default	remarks
JS0	[A m^{-2}]			0.5×10^{-6}	
JS0SW	[A m^{-1}]			0	
NJ	[—]			1.0	
NJSW	[—]			1.0	
XTI	[—]			2.0	
XTI2	[—]			0	
DIVX	[V^{-1}]			0	
CTEMP	[—]			0	
CISB	[—]			0	
CISBK	[A]			0	
CVB	[—]	-0.1	0.2	0	
CJ	[F m^{-2}]			5×10^{-4}	
CJSW	[F m^{-1}]			5×10^{-10}	
CJSWG	[F m^{-1}]			5×10^{-10}	
MJ	[—]			0.5	
MJSW	[—]			0.33	
MJSWG	[—]			0.33	
PB	[V]			1.0	
PBSW	[V]			1.0	
PBSWG	[V]			1.0	
VDIFFJ	[V]			0.6×10^{-3}	
TCJBD	[K^{-1}]			0	
TCJBDSW	[K^{-1}]			0	
TCJBDSWG	[K^{-1}]			0	
TCJBS	[K^{-1}]			0	
TCJBSSW	[K^{-1}]			0	
TCJBSSWG	[K^{-1}]			0	
NFALP	[cm s]			1×10^{-19}	
NFTRP	[V^{-1}]			10G	
∗**CIT**	[F cm^{-2}]			0	
FALPH	[sm^{3}]			1.0	
DLY1	[s]			100×10^{-12}	
DLY2	[m^{2}]			0.7	
DLY3	[Ωm^{2}]			0.8×10^{-6}	
XQY	[m]	10n	50n	0	
XQY1	[F·μm$^{\mathbf{XQY2}-1}$]	0		0	
XQY2	[—]	0		2	
OVSLP	[mV^{-1}]			2.1×10^{-7}	
OVMAG	[V]			0.6	
CGSO	[F m^{-1}]	0	100nm $\times C_{\rm ox}$		to be set by user
CGDO	[F m^{-1}]	0	100nm $\times C_{\rm ox}$		to be set by user
CGBO	[F m^{-1}]	0		0	

parameter	unit	min	max	default	remarks
RS	[Ωm]	0	10m	0	
RD	[Ωm]	0	100m	0	
RSH	[V A^{-1}square]	0	500	0	
RSHG	[V A^{-1}square]	0	100	0	
GBMIN	[—]			1×10^{-12}	for circuit simulation
GDSLEAK	[—]			0	for circuit simulation
RBPB	[Ω]			50	instance parameter
RBPD	[Ω]			50	instance parameter
RBPS	[Ω]			50	instance parameter
RBDB	[Ω]			50	instance parameter
RBSB	[Ω]			50	instance parameter
RTH0	[Kcm/W]	0	10	0.1	
RTHTEMP1	[Kcm/W/K]	-1	1	0	
RTHTEMP2	[Kcm/W/K^2]	-1	1	0	
CTH0	[Ws/(Kcm)]			1×10^{-7}	
RTH0W	[μm$^{\mathbf{RTH0WP}}$]	-100	100	0	
RTH0WP	[—]	-10	10	1	
RTH0NF	[—]	-5	5	0	
RTH0R	[—]				inactivated
POWRAT	[—]	0	1.0	1.0	
PRATTEMP1	[1/K]	-1	1	0	
PRATTEMP2	[1/K^2]	-1	1	0	
SHEMAX	[K]	300	600	500	
XLDLD	[m]	0		1×10^{-6}	reset to **XLDLD** ≥ 0
LOVERLD	[m]	0		1.0×10^{-6}	
LOVERS	[m]	0		30nm	
LOVER	[m]	0		30n	
NOVER	[cm^{-3}]			3×10^{16}	
NOVERS	[cm^{-3}]			1.0×10^{17}	
VFBOVER	[V]	-1	1	0.5	
DLYDFT	[m^2/(Vs)]			5.0×10^{-2}	inactivated
DLYOV	[s/F]			0	inactivated
QOVADD	[F/m^2]			0	
CVDSOVER	[—]	0	1.0	0	modify $C_{\rm gg}$ spikes
LDRIFT1	[m]	0		1.0×10^{-6}	
LDRIFT1S	[m]	0		0.0	
LDRIFT2	[m]	0		1.0 ×10^{-6}	
LDRIFT2S	[m]	0		1.0 ×10^{-6}	
LDRIFT	[m]	0		1.0 ×10^{-6}	taken as **LDRIFT2**
****CORDRIFT**=1**					
RDRDL1	[m]			0	
RDRDL2	[m]			0	
RDRCX	[—]	0	1	0	reset within the range
RDRCAR	[mV^{-1}]	0	50n	1×10^{-8}	
RDRDJUNC	[m]			1.0×10^{-6}	
RDRBB	[—]			1.0	
RDRMUE	[$m^2(V \cdot s)^{-1}$]	100	3K	1K	
RDRMUEL	[μm$^{\mathbf{RDRMUELP}}$]			0	
RDRMUELP	[—]			1	

parameter	unit	min	max	default	remarks
RDRMUETMP	[—]	0.0	2.0	0	
RDRVMAX	[cm s^{-1}]	1MEG	100MEG	30MEG	
RDRVMAXL	[$\mu m^{\mathbf{RDRVMAXLP}}$]			0	
RDRVMAXLP	[—]			1	
RDRVMAXW	[$\mu m^{\mathbf{RDRVMAXWP}}$]			0	
RDRVMAXWP	[—]			1	
RDRVTMP	[—]	-2.0	1.0	0	
RDRQOVER	[—]	0	1×10^{7}	1×10^{5}	
****CORDRIFT=0****					
RDVG11	[]	0	$V_{\rm ds,max}/30$	0	**CORSRD**=1,3
RDVG12	[V^{-1}]	0	$V_{\rm ds,max}$	100	**CORSRD**=1,3
RDVG11	[]	0	$V_{\rm ds,max}/30$	0	**CORSRD**=1,3
RDVG12	[V^{-1}]	0	$V_{\rm ds,max}$	100	**CORSRD**=1,3
RDVD	[Ω/V]	0	2.0	7.0×10^{-2}	**CORSRD**=1,3
RDVB	[V^{-1}]	0	2.0	0	**CORSRD**=1,3
RDS	[$\mu m^{\mathbf{RDSP}}$]	-100	100	0	**CORSRD**=1,3
RDSP	[—]	-10	10	1	**CORSRD**=1,3
RDVDL	[$\mu m^{-\mathbf{RDVDLP}}$]	-100	100	0	**CORSRD**=1,3
RDVDLP	[—]	-10	10	1	**CORSRD**=1,3
RDVDS	[$\mu m^{\mathbf{RDVDSP}}$]	-100	100	0	**CORSRD**=1,3
RDVDSP	[—]	-10	10	1	**CORSRD**=1,3
RD20	[—]	0	30	0	**CORSRD**=2,3
RD21	[—]	0	1.0	1.0	**CORSRD**=2,3
RD22	[Ω m/$V^{\mathbf{RD22D}+1}$]	-5.0	0	0	**CORSRD**=2,3
RD22D	[—]	0	2.0	0	**CORSRD**=2,3
RD23	[Ω m/$V^{\mathbf{RD21}}$]	0	2.0	5m	**CORSRD**=2,3
RD23L	[$\mu m^{-\mathbf{RD23LP}}$]	-100	100	0	**CORSRD**=2,3
RD23LP	[—]	-10	10	1	**CORSRD**=2,3
RD23S	[$\mu m^{\mathbf{RD23SP}+1}$]	-100	100	0	**CORSRD**=2,3
RD23SP	[—]	-10	10	1	**CORSRD**=2,3
RD24	[Ωm/$V^{\mathbf{RD21}+1}$]	0	0.1	0	**CORSRD**=2,3
RD25	[V]	0	$V_{\rm gs,max}$	0	**CORSRD**=2,3
RDOV11	[—]	0	10	0	**CORSRD**=1,3
RDOV12	[—]	0	2	1.0	**CORSRD**=1,3
RDOV13	[—]	0	1.0	1.0	**CORSRD**=1,3
RDSLP1	[—]	-10	10	0	**CORSRD**=1,3
RDICT1	[—]	-10	10	1.0	**CORSRD**=1,3
RDSLP2	[—]	-10	10	1	**CORSRD**=1,3
RDICT2	[—]	-10	10	0	**CORSRD**=1,3
RDTEMP1	[Ωm/K]	-1.0×10^{-3}	2.0×10^{-2}	0	
RDTEMP2	[Ωm/K^2]	-1.0×10^{-5}	1.0×10^{-5}	0	
RDVDTEMP1	[Ωm/(VK)]	-1.0×10^{-3}	1.0×10^{-2}	0	
RDVDTEMP2	[Ωm/$(VK)^2$]	-1.0×10^{-5}	1.0×10^{-5}	0	
RDVDSUB	[—]			0.3	
RDVSUB	[—]			1.0	
VBISUB	[—]			0.7	

26 Overview of the Parameter-Extraction Procedure

26.1 General MOSFET Part

In HiSIM, device characteristics are strongly dependent on basic device parameter values, such as the impurity concentration and the oxide thickness. Therefore, the parameter-value extraction has to be repeated with measured characteristics of different devices in a specific sequence until extracted parameter values reproduce all device characteristics consistently and reliably. To achieve reliable results, it is recommended to start with initial parameter values according to the recommendations listed in the table below. Since some of the model parameters such as $T_{\rm ox}$ are difficult to extract, they are expected to be determined directly by dedicated measurements. Threshold voltage measurements allow to derive a rough extraction for the model parameters referred to as "basic device parameters". The parameters identified with the symbol "*" in the Model Parameter Table are initially fixed to zero.

Determined by dedicated measurements (not changed during extraction procedure) are used	Default values listed in the section 25 initially for the groups of parameters listed below
TOX	basic device parameters (not listed on left side) gate leakage GIDL source/bulk and drain/bulk diodes noise subthreshold swing non-quasi-static model overlap capacitances

The sequence of device selection for the parameter extraction is recommended in 4 steps

1. Long-Channel Devices
2. Short-Channel Devices
3. Long-Narrow Devices
4. Short-Narrow Devices

Prior to the extracttion, a rough extraction with measured $V_{\rm th} - L_{\rm gate}$ characteristics is recommended to get rough idea about parameter values. These parameters are usually important giving strong influence on accuracy of the total parameter extraction. The parameter extraction of the general MOSFET part is summarized in the following Table.

26.2 HiSIM_HV Specific Part

Model parameters are categorized into two parts: (1) general MOSFET related parameters and (2) the HiSIM_HV specific parameters. The HiSIM_HV specific model parameters are extracted after the extraction of the intrinsic MOSFET part. Recommended extraction procedure is to perform first (1) and then (2). Thus the parameter extraction is done in the following sequence:

1. rougth extraction of the MOSFET parameters with measured $V_{\rm th} - L_{\rm gate}$
2. fine extraction with measured subthreshold in $I_{\rm ds} - V_{\rm gs}$
3. extraction of mobility parameters with $I_{\rm ds} - V_{\rm gs}$ and $I_{\rm ds} - V_{\rm ds}$

Table 23: Summary of the 7 steps of HiSIM's Parameter Extraction Procedure.

Step	Description	Parameters
Step 1: Initial preparation and rough extraction		
1-1.	Initialize all parameters to their default values	
1-2.	Use the measured gate-oxide thickness for TOX	TOX
1-3.	Rough extraction with $V_{\rm th}$-dependence on $L_{\rm gate}$ $[V_{\rm th} - V_{\rm gs}]$	**NSUBC**, **VFB**, **SC1**, **SC2**, **SC3**, **NSUBP**, **LP**, **SCP1**, **SCP2**, **SCP3**, **NPEXT**, **LPEXT**
1-4.	Quantum and poly-depletion effects $[C_{\rm gg} - V_{\rm gs}]$	**QME1**, **QME2**, **QME3**, **PGD1**, **PGD2**
Step 2: Extraction with long and wide transistors		
2-1.	Fitting of sub-threshold characteristics $[I_{\rm ds} - V_{\rm gs}]$	**NSUBC**, **VFB**, **MUECB0**, **MUECB1**
2-2.	Determination of mobility parameters for low $V_{\rm ds}$ $[I_{\rm ds} - V_{\rm gs}]$	**MUEPH0**, **MUEPH1**, **MUESR0**, **MUESR1**
2-3.	Determination of mobility parameters for high $V_{\rm ds}$ $[I_{\rm ds} - V_{\rm gs}]$	**NINV**, **NDEP**
Step 3: Extraction with medium/short length and large width transistors		
3-1.	Pocket-parameter extraction with medium length transistors $[I_{\rm ds} - V_{\rm gs}]$	**NSUBP**, **LP**, **SCP1**, **SCP2**, **SCP3**, **NPEXT**, **LPEXT**
3-2.	Short-channel-parameter extraction with short-length transistors $[V_{\rm th} - L_{\rm gate}]$	**SC1**, **SC2**, **SC3**, **PARL2**, **XLD**
3-3.	Mobility-parameter refinement for low $V_{\rm d}$ $[I_{\rm ds} - V_{\rm gs}]$	**MUEPHL**, **MUEPLP**, **MUESRL**, **MUESLP**
3-4.	Velocity parameter extraction for high $V_{\rm d}$ $[I_{\rm ds} - V_{\rm gs}]$	**VMAX**, **VOVER**, **VOVERP**
3-5.	Parameters for channel-length modulation $[I_{\rm ds} - V_{\rm ds}]$	**CLM1**, **CLM2**, **CLM3**
3-6.	Source/drain resistances $[I_{\rm ds} - V_{\rm ds}]$	**RS**, **RD**, **RSH**, **NRS**, **NRD**
Step 4: Extraction of the width dependencies for long transistors		
4-1.	Fitting of sub-threshold width dependencies $[I_{\rm ds} - V_{\rm gs}]$	**NSUBC**, **NSUBCW**, **NSUBCWP**, **WFC**, **XWD**, **WVTH0**
4-2.	Fitting of mobility width dependencies $[I_{\rm ds} - V_{\rm gs}]$	**MUEPHW**, **MUEPWP**, **MUESRW**, **MUESWP**
Step 5: Extraction of the width dependencies for short transistors		
5-1.	Fitting of sub-threshold dependencies $[I_{\rm ds} - V_{\rm gs}]$	**NSUBP0**, **NSUBWP**
Step 6: Extraction of small-geometry effects		
6-1.	Effective channel-length corrections	**WL2**, **WL2P**
6-2.	Mobility and velocity $[I_{\rm ds} - V_{\rm ds}]$	**MUEPHS**, **MUEPSP**, **VOVERS**, **VOVERSP**
Step 7: Extraction of temperature dependence with long-channel transistors		
7-1.	Sub-threshold dependencies $[I_{\rm ds} - V_{\rm gs}]$	**BGTMP1**, **BGTMP2**, **EG0**
7-2.	Mobility and maximum carrier-velocity dependencies $[I_{\rm ds} - V_{\rm gs}]$	**MUETMP**, **VTMP**

4. extraction of resistance parameters with $I_{\rm ds} - V_{\rm gs}$ and $I_{\rm ds} - V_{\rm ds}$
5. fine extraction of resistance with channel-conductance and trans-conductance
6. capacitacne extraction

Agreement of the extraction results after the 3rd step is not sufficient especially in high $V_{\rm gs}$ region and low $V_{\rm ds}$ region. The 4th resistance-extraction step is focused on the resion where the quasi-saturation effect is obvious. It is recommended to repeat the extraction steps from 3rd to 5th to achieve better fitting. The steps from 1st to 3rd are the same as the conventional extraction procedure.
The extraction of the resistance parameters are done after the model selection as summarized in Fig. 25.

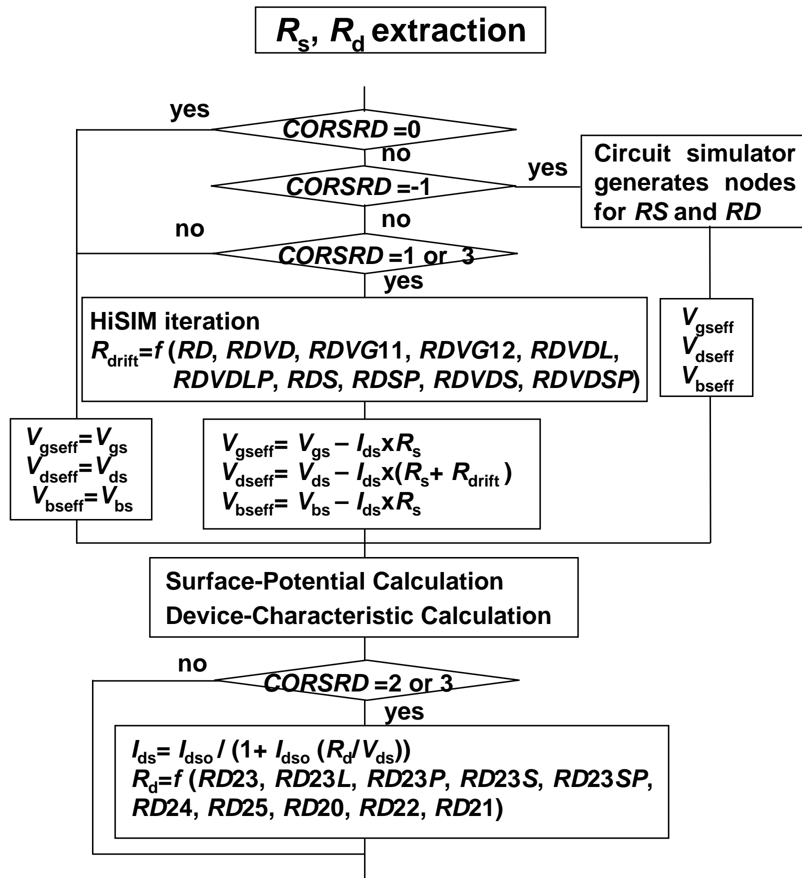

Fig. 25: Parameter extraction flow for resistance parameters. For the new resistance model (**CORDIRIFT**=1) the flag **CORSRD** is no more valid but only one extraction procedure is followed, namely the "HiSIM iteration" part with the new model equations.

If the self-heating effect is activatied, all device characteristics are changed drastically. Retunning of model parameters are required. These model parameters are mostly related to the mobility and resistance models. The temperature dependent parameters are extracted without the self-heating effect with temperature dependent measurements. These values are usually not necessary to be modified after activating the self-heating effect.

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